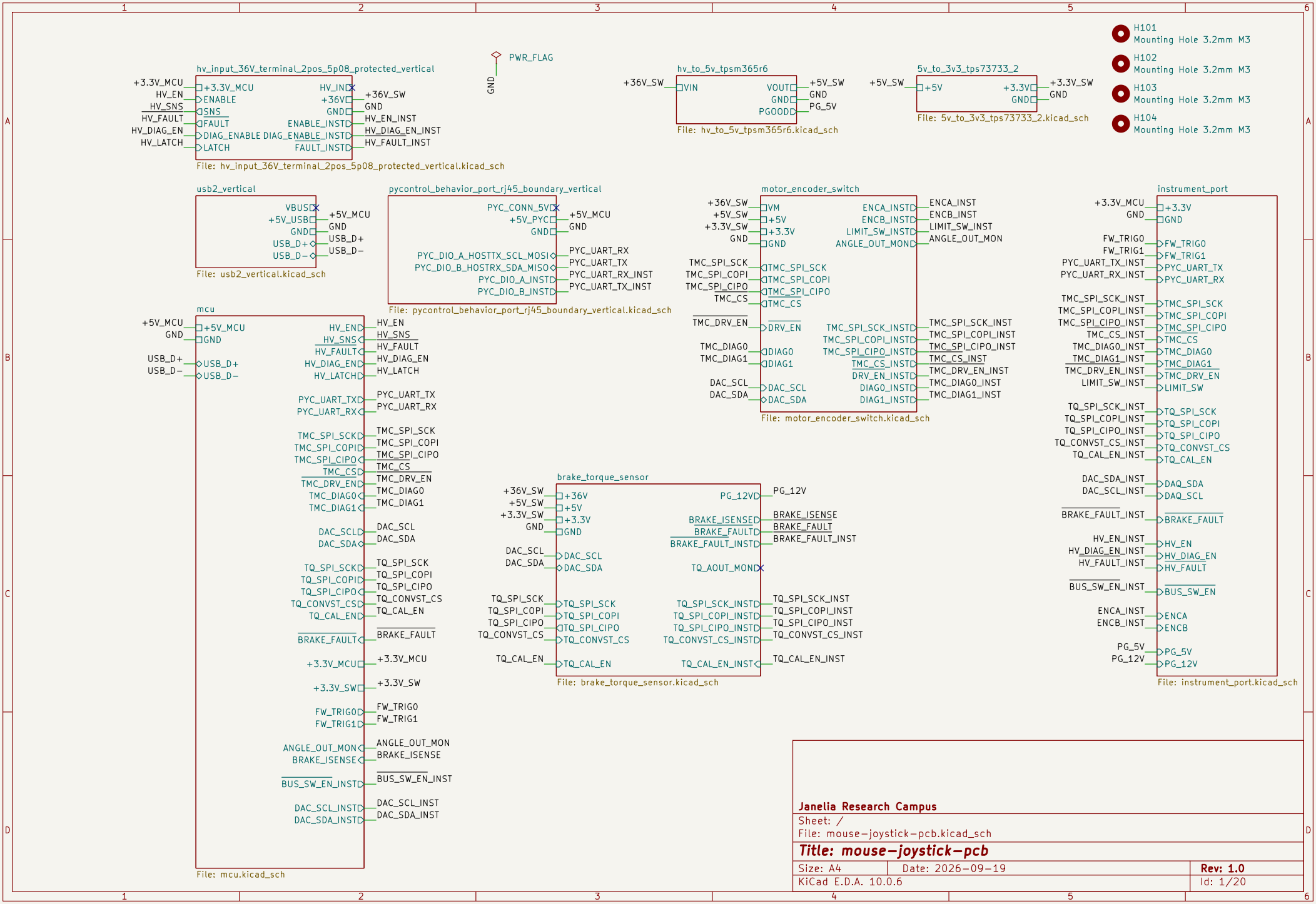
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HV_EN
HV_SNS
HV_FAULT
HV_DIAG_EN
HV_LATCH
+3.3V_MCU
ENABLE
SNS
FAULT
DIAG_ENABLE
LATCH
HV_IN
+36V
GND
ENABLE_INST
DIAG_ENABLE_INST
FAULT_INST
+36V_SW
GND
HV_EN_INST
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HV_FAULT_INST
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PWR_FLAG
GND
hv_to_5v_tpsm365r6
+36V_SW
VIN
VOUT
GND
PGOOD
+5V_SW
GND
PG_5V
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+5V_SW
+5V
+3.3V
GND
+3.3V_SW
GND
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H101
Mounting Hole 3.2mm M3
H102
Mounting Hole 3.2mm M3
H103
Mounting Hole 3.2mm M3
H104
Mounting Hole 3.2mm M3
usb2_vertical
VBUS
+5V_USB
GND
USB_D+
USB_D−
+5V_MCU
GND
USB_D+
USB_D−
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PYC_CONN_5V
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GND
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PYC_DIO_B_HOSTRX_SDA_MISO
PYC_DIO_A_INST
PYC_DIO_B_INST
+5V_MCU
GND
PYC_UART_RX
PYC_UART_TX
PYC_UART_RX_INST
PYC_UART_TX_INST
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motor_encoder_switch
+36V_SW
+5V_SW
+3.3V_SW
GND
TMC_SPI_SCK
TMC_SPI_COPI
TMC_SPI_CIPO
TMC_CS
TMC_DRV_EN
TMC_DIAG0
TMC_DIAG1
DAC_SCL
DAC_SDA
VM
+5V
+3.3V
GND
DRV_EN
DIAG0
DIAG1
DAC_SCL
DAC_SDA
ENCA_INST
ENCB_INST
LIMIT_SW_INST
ANGLE_OUT_MOND
TMC_SPI_SCK_INST
TMC_SPI_COPI_INST
TMC_SPI_CIPO_INST
TMC_CS_INST
DRV_EN_INST
DIAG0_INST
DIAG1_INST
ENCA_INST
ENCB_INST
LIMIT_SW_INST
ANGLE_OUT_MON
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FW_TRIG1
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PYC_UART_RX_INST
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TMC_SPI_COPI_INST
TMC_SPI_CIPO_INST
TMC_CS_INST
TMC_DIAG0_INST
TMC_DIAG1_INST
TMC_DRV_EN_INST
LIMIT_SW_INST
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TQ_SPI_COPI_INST
TQ_SPI_CIPO_INST
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TQ_CAL_EN_INST
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DAC_SCL_INST
BRAKE_FAULT_INST
HV_EN_INST
HV_DIAG_EN_INST
HV_FAULT_INST
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ENCA_INST
ENCB_INST
PG_5V
PG_12V
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GND
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PYC_UART_RX
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TMC_SPI_CIPO
TMC_CS
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TMC_DIAG1
TMC_DRV_EN
LIMIT_SW
TQ_SPI_SCK
TQ_SPI_COPI
TQ_SPI_CIPO
TQ_CONVST_CS
TQ_CAL_EN
DAQ_SDA
DAQ_SCL
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HV_DIAG_EN
HV_FAULT
BUS_SW_EN
ENCA
ENCB
PG_5V
PG_12V
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USB_D−
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HV_SNS
HV_FAULT
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TMC_SPI_SCK
TMC_SPI_COPI
TMC_SPI_CIPO
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TMC_DIAG0
TMC_DIAG1
DAC_SCL
DAC_SDA
TQ_SPI_SCK
TQ_SPI_COPI
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TQ_CONVST_CS
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BRAKE_FAULT
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+3.3V_SW
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FW_TRIG1
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BRAKE_ISENSE
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DAC_SCL_INST
DAC_SDA_INST
+5V_MCU
GND
USB_D+
USB_D−
HV_EN
HV_SNS
HV_FAULT
HV_DIAG_EN
HV_LATCH
PYC_UART_TX
PYC_UART_RX
TMC_SPI_SCK
TMC_SPI_COPI
TMC_SPI_CIPO
TMC_CS
TMC_DRV_EN
TMC_DIAG0
TMC_DIAG1
DAC_SCL
DAC_SDA
TQ_SPI_SCK
TQ_SPI_COPI
TQ_SPI_CIPO
TQ_CONVST_CS
TQ_CAL_EN
BRAKE_FAULT
+3.3V_MCU
+3.3V_SW
FW_TRIG0
FW_TRIG1
ANGLE_OUT_MON
BRAKE_ISENSE
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+5V_SW
+3.3V_SW
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DAC_SCL
DAC_SDA
TQ_SPI_SCK
TQ_SPI_COPI
TQ_SPI_CIPO
TQ_CONVST_CS
TQ_CAL_EN
+36V
+5V
+3.3V
GND
DAC_SCL
DAC_SDA
TQ_SPI_SCK
TQ_SPI_COPI
TQ_SPI_CIPO
TQ_CONVST_CS
TQ_CAL_EN
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BRAKE_ISENSE
BRAKE_FAULT
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TQ_SPI_COPI_INST
TQ_SPI_CIPO_INST
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PG_12V
BRAKE_ISENSE
BRAKE_FAULT
BRAKE_FAULT_INST
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Janelia Research Campus
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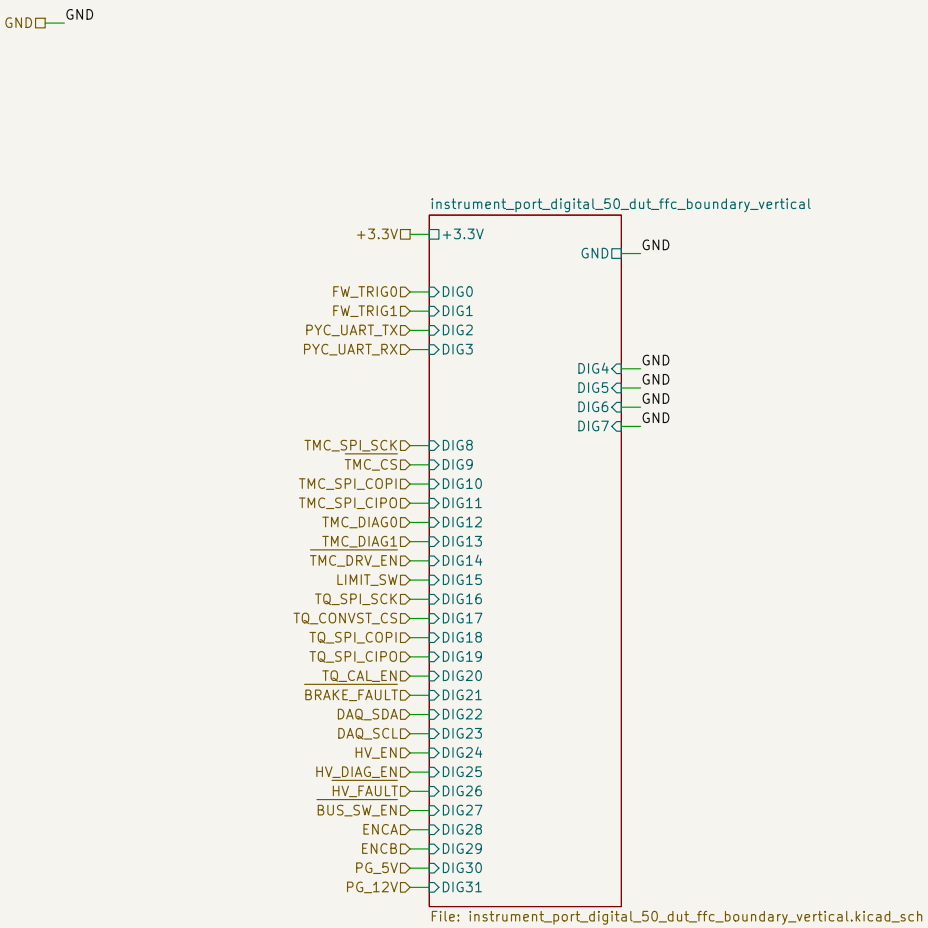
Date: 2026−09−19
Rev: 1.0
KiCad E.D.A. 10.0.6
Id: 1/20



Janelia Research Campus		
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Title: mouse-joystick-pcb		
Size: A4	Date: 2026-09-19	**Rev: 1.0**
KiCad E.D.A. 10.0.6		Id: 14/20

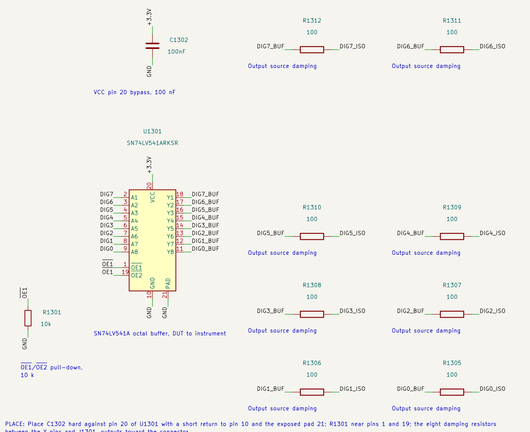
InstrumentPort-Digital-50 DUT boundary | four SN74LV541A octets, 100 ohm damping, enabled by hardware

DUT-side InstrumentPort-Digital-50 with integrated read-only buffering, on a VERTICAL, top-entry 50-contact ZIF connector: Hirose FH12-50S-0.5SVA(54). OW-CONN-FH12-50S-0-5SVA-54, LCSC C597991, 0.5mm pitch, symbol Conn_01x50, footprint orb_weaver_connectors:Hirose_FH12-50S-0.5SVA_1x50-4MP_P0.5mm_Vertical: the four mechanical lands are unnumbered pads and carry no net.

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Octet DIG0 to DIG7: U1301

U1301 buffers DIG0 to DIG7 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18): R1305 to R1312 (100 ohm) damp each output into its connector contact.
C1302 bypasses VCC (pin 20): R1301 holds both enables (pins 1 and 19) low.

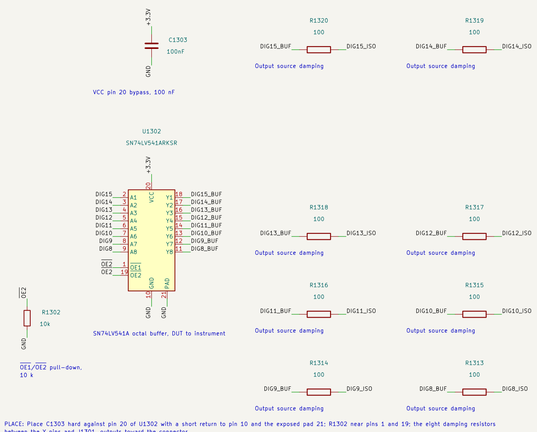


PLACE: Place C1302 hard against pin 20 of U1301 with a short return to pin 10 and the exposed pad 21; R1301 near pins 1 and 19; the eight damping resistors between the Y pins and J1301, outputs toward the connector.

ROUTE: The DIG0 to DIG7 inputs are this block's ports and escape toward the board on vias; keep the Y runs short to the resistors and the resistor-to-contact runs paired with the connector's ground contacts.

2. Octet DIG8 to DIG15: U1302

U1302 buffers DIG8 to DIG15 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18): R1313 to R1320 (100 ohm) damp each output into its connector contact.
C1303 bypasses VCC (pin 20): R1302 holds both enables (pins 1 and 19) low.

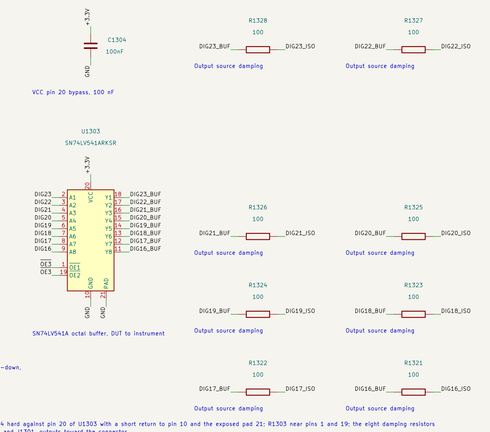


PLACE: Place C1303 hard against pin 20 of U1302 with a short return to pin 10 and the exposed pad 21; R1302 near pins 1 and 19; the eight damping resistors between the Y pins and J1301, outputs toward the connector.

ROUTE: The DIG8 to DIG15 inputs are this block's ports and escape toward the board on vias; keep the Y runs short to the resistors and the resistor-to-contact runs paired with the connector's ground contacts.

3. Octet DIG16 to DIG23: U1303

U1303 buffers DIG16 to DIG23 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18): R1321 to R1328 (100 ohm) damp each output into its connector contact.
C1304 bypasses VCC (pin 20): R1303 holds both enables (pins 1 and 19) low.



PLACE: Place C1304 hard against pin 20 of U1303 with a short return to pin 10 and the exposed pad 21; R1303 near pins 1 and 19; the eight damping resistors between the Y pins and J1301, outputs toward the connector.

ROUTE: The DIG16 to DIG23 inputs are this block's ports and escape toward the board on vias; keep the Y runs short to the resistors and the resistor-to-contact runs paired with the connector's ground contacts.

4. Octet DIG24 to DIG31: U1304

U1304 buffers DIG24 to DIG31 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18): R1329 to R1336 (100 ohm) damp each output into its connector contact.
C1305 bypasses VCC (pin 20): R1304 holds both enables (pins 1 and 19) low.

PLACE: Place C1305 hard against pin 20 of U1304 with a short return to pin 10 and the exposed pad 21; R1304 near pins 1 and 19; the eight damping resistors between the Y pins and J1301, outputs toward the connector.

ROUTE: The DIG24 to DIG31 inputs are this block's ports and escape toward the board on vias; keep the Y runs short to the resistors and the resistor-to-contact runs paired with the connector's ground contacts.

5. Rail-entry bulk bypass

C1301 (4.7 uF) holds the +3.3V rail where it enters the block; the per-package 100 nF bypasses are in the octet groups.

PLACE: Place C1301 at the supply entry of the block, not at any one package.

ROUTE: +3.3V carries PWR_3V3_LOCAL from the entry to the four VCC pins; GND is PWR_RETURN_LOCAL.

6. FFC receptacle

J1301 carries the 32 damped outputs (DIGn_ISO) on the contract's DUT contacts and the 18 grounds on one GND: the four mechanical lands carry no net.

50-contact FFC receptacle, top entry

PLACE: Vertical, top-entry receptacle at the board edge, latch away from the buffers; verify pin 1 and the contact face on the real part.

ROUTE: Pair each DIGn_ISO with its neighbouring ground contact and tie all 18 grounds into one GND copper under the connector; land pattern dual-row staggered at 1.0 mm within each row.

OPERATION

DUT side of the InstrumentPort-Digital-50 profile (board-interfaces docs/instrument-port-digital.md, draft v0.1). Direction is a hardware property. DUT to instrument only: DIGn enters U1301 to U1304 (DIG0 to 7, 8 to 15, 16 to 23, 24 to 31, each octet one package, A8 down to A1), leaves on Y8 to Y1 through 100 ohm damping (R1305 to R1336) onto J1301. The cable carries no supply, reference, enable or stimulus.

Pin mapping is the contract's DUT table and is not mirrored: channel n lands on contact 2 + n + floor(n/2) + floor(n/16). DIG0 on contact 2, DIG31 on contact 49, the 18 grounds on 1, 4, 7, ... 47, 50 with the 25/26 double ground at the bank boundary. The mirror lives on instrument_port_digital_50_adapter_ffc_boundary_vertical; mirroring both ends cancels, and ERC and DRC cannot see it.

Enabled by hardware default, no disable at all; both active-low enables of each package share one net held low by its 10 k pull-down (R1301 to R1304: at most about 0.1 V from the two inputs' leakage against the 0.99 V VIL), so observation works with the MCU in reset or unprogrammed. The contract permits this since 2026-09-15: do not re-add a control as a fix.

Supply: the always-on 3.3 V rail on VCC (pins 20): SN74LV541A runs 2 to 5.5 V, drives +/-8 mA at 3.3 V, inputs tolerate 0 to 5.5 V with Ioff <= 5 uA unpowered, VIH 2.31 V, VIL 0.99 V, edges <= 100 ns/V, not a Schmitt input. C1302 to C1305 (100 nF) bypass each pin 20; C1301 (4.7 uF, X5R 0402, well below nameplate at 3.3 V bias) is the one rail-entry bulk, not a fifth per-package bypass.

The 100 ohm damping bounds a hard short of one output to GND at 33 mA, inside the +/-35 mA per-output absolute maximum, and damps edges into the cable: it is not short-circuit protection. Input bias is board-specific and not in this block: every unused DIGn must be tied at the board. Attach and remove the FFC with target power off; J1301 is rated 20 mating cycles, so break the link at the instrument end.

DESIGN CONTRACT

DUT-side InstrumentPort-Digital-50 with integrated read-only buffering, on a VERTICAL, top-entry 50-contact ZIF connector: Hirose FH12-50S-0.5SVA(54). OW-CONN-FH12-50S-0-5SVA-54, LCSC C597991, 0.5mm pitch, symbol Conn_01x50, footprint orb_weaver_connectors:Hirose_FH12-50S-0.5SVA_1x50-4MP_P0.5mm_Vertical: the four mechanical lands are unnumbered pads and carry no net. Thirty-two channels through four SN74LV541ARKSR octal buffers (OW-MISC-SN74LV541ARKSR: C7364695, symbol orb_weaver_misc:SN74LV541ARKSR, footprint orb_weaver_smt:Texas_RKS0020A_VQFN-20-1EP_2.5x4.5mm_P0.5mm_EP1x3mm, exposed pad 21 to GND), grouped DIG0-7 / DIG8-15 / DIG16-23 / DIG24-31 to match the 13-contact octet windows. The 541 is flow-through: input pin p pairs with output pin 20-p. A1(2) to Y1(18) through A8(9) to Y8(11). DIRECTION IS A HARDWARE PROPERTY: DUT to instrument only. The cable carries no supply, no voltage reference, no enable and no stimulus, and nothing in this block may be driven by the instrument. PIN MAPPING IS THE CONTRACT'S DUT TABLE AND IS NOT MIRRORED: channel n lands on pin 2 + n + floor(n/2) + floor(n/16), so DIG0 is pin 2 and DIG31 is pin 49, with all 18 grounds on pins 1, 4, 7, 10, 13, 16, 19, 22, 25, 26, 29, 32, 35, 38, 41, 44, 47 and 50. THE MIRROR LIVES ON THE ADAPTER, NOT HERE. instrument_port_digital_50_adapter_ffc_boundary_vertical is pre-mirrored to 51-n so that the expected reversing assembly - same-side Type A FFC with a vertical FH12 at both ends, connectors rotated 180 degrees - delivers DIGn to DIGn. Mirroring both ends cancels and channels arrive as DIG31-n. The ground pattern is palindromic under 51-n, so a mirrored map lands every ground identically and every net stays driven and terminated: ERC, DRC and design_block_tools.py check are ALL BLIND to this error, and only a pin-by-pin netlist comparison or continuity on the real cable catches it. Per-output source damping is 100 ohms, OW-PASS-0402WSF1000TCE. That value is chosen as the smallest standard one that bounds a hard short to ground inside the LV541A's +/-35mA output absolute maximum even crediting the driver with zero impedance (3.3V/100R = 33mA): 68R gives 49mA, 47R gives 70mA, and the legacy 33R gives 100mA. It is NOT short-circuit protection and does not cover every fault. DEFAULT-ENABLED BY HARDWARE, AND THERE IS NO DISABLE AT ALL: both active-low OE inputs of each package share one net held low by a single 10k pull-down - R1301 through R1304. one per package - so observation works with the MCU held in reset, unprogrammed or unable to boot, and the port cannot be muted without desoldering. There is no manual jumper, no firmware link and no OE port. The swelling contract was relaxed on 2026-09-15 from requiring manual disabling to permitting none, so this reasoning and the retained future option are in klcad-libs/docs/digital-instrument-port-design-blocks.md under. No disable control, and why'. DO NOT re-add a control as an oversight fix. Shared 10k is verified against aggregate leakage: 2 x 5uA max gives 0.1V against a 0.99V VIL. If a noise investigation ever needs a mute, detaching the FFC bounds the cable's contribution but NOT the buffers', which keep switching into their board-side traces and damping resistors: lift the 100R resistors on the suspect channels instead. SUPPLY FROM THE BOARD'S ALWAYS-ON 3.3V RAIL. Independent of firmware, HV_EN and every switched domain: a buffer on a switched rail cannot observe the domain it is powering down with. DECOUPLING is one 100nF per package, C1302 through C1305, hard against pin 20 with a short return, plus one 4.7uF rail-entry bulk. C1301 / OW-CAP-4U7-0402-X5R-16V. at the supply entry. C1301 is NOT a fifth per-IC bypass - do not 'fix' its distance to any package. Simultaneous-switching budget: 32 x 50pF x 3.3V = 5.3nC per all-channel edge, about 1mV of droop against the combined local reservoir; Expect meaningfully less than 4.7uF at 3.3V bias - a 4.7uF X5R in an 0402 derates hard - so treat the nameplate value as nominal, not measured. INPUT BIAS IS BOARD-SPECIFIC AND IS NOT IN THIS BLOCK: there is no universal pull-down, because SPI selects, open-drain buses and switched-domain taps each need different bias, and pulls that must read HIGH on a switched net reference the switched rail, never the always-on one. Every unused input must be explicitly tied at the board. LV541A at 3.3V needs VIH >= 2.31V and VIL <= 0.99V with transitions <= 100 ns/V: It is 0-5.5V input tolerant with 2pF typical input capacitance and Ioff <= 5uA at VCC=0. It is NOT Schmitt-triggered and NOT a comparator: do not route a raw analog node through it for a timing witness, and do not treat a clean legacy LVC125A capture as LV541A qualification. OE would disable outputs only - it never removes input loading or makes a floating input acceptable, which is part of why no mute was fitted. Requires straight-ended 0.50 +/-0.05mm FFC with gold contacts, at least 2mm exposed contact and 3mm reinforcement; retention-eared cable is NOT qualified for this connector. Rated 20 mating cycles, so prefer breaking the link at the instrument end, and attach or remove the cable with target power off unless the actual assembly is hot-plug qualified. Profile is InstrumentPort-Digital-50 draft v0.1. UNQUALIFIED: no measured rate, delay, skew, loading or power-state limit has been established. Marker/beacon channel indices are NOT frozen, with DIG0/DIG1 the current recommendation over the earlier DIG14/DIG15. Pairs with instrument_port_digital_50_adapter_ffc_boundary_vertical: the analyzer-specific channel map belongs to ia5032_connector_boundary, not here. GROUNDED INPUTS ARE THE BOARD'S COPPER: the inputs are this block's ports, so a board that grounds unused DIGn channels draws one 0.20 mm track per grounded LV541A pad column straight into that package's thermal pad on F.Cu, before autorouting: freerouting will not run a track along a row of same-net 0.5 mm-pitch pads and left those groups unrouted on every camera-board run (layout conventions 11a). Since 2026-09-29 every DIGn also ends at its own escape via above the pad row, so a board may instead tie an unused channel to ground at that via; either way the grounding copper is the board's, never the block's. FLOOR COPPER IS DECLARED: the 0.10 mm gaps between the 32 damping resistors and the LV541A pins (2026-09-26) and between each DIGn escape stub and the escape via beside it (2026-09-29) are wrapped in BLOCK_FLOOR rule areas, so a consuming board sees no clearance findings from this block under the shared rules: a board wanting 0.20 mm inside the block re-routes the block, not the rule (layout conventions 12).

INTERFACES

+3.3V — +3.3V

Always-on 3.3 V buffer supply (VCC pins 20); never reaches the cable.

GND — GND

18 connector grounds, buffer GND pins and pads, bypass and OE pull-down return.

DIG0 — DIG0

Observation input 0 into U1301 A8 (pin 9); leaves on contact 2.

DIG1 — DIG1

Observation input 1 into U1301 A7 (pin 8); leaves on contact 3.

DIG2 — DIG2

Observation input 2 into U1301 A6 (pin 7); leaves on contact 5.

DIG3 — DIG3

Observation input 3 into U1301 A5 (pin 6); leaves on contact 6.

DIG4 — DIG4

Observation input 4 into U1301 A4 (pin 5); leaves on contact 8.

DIG5 — DIG5

Observation input 5 into U1301 A3 (pin 4); leaves on contact 9.

DIG6 — DIG6

Observation input 6 into U1301 A2 (pin 3); leaves on contact 11.

DIG7 — DIG7

Observation input 7 into U1301 A1 (pin 2); leaves on contact 12.

DIG8 — DIG8

Observation input 8 into U1302 A8 (pin 9); leaves on contact 14.

DIG9 — DIG9

Observation input 9 into U1302 A7 (pin 8); leaves on contact 15.

DIG10 — DIG10

Observation input 10 into U1302 A6 (pin 7); leaves on contact 17.

DIG11 — DIG11

Observation input 11 into U1302 A5 (pin 6); leaves on contact 18.

DIG12 — DIG12

Observation input 12 into U1302 A4 (pin 5); leaves on contact 20.

DIG13 — DIG13

Observation input 13 into U1302 A3 (pin 4); leaves on contact 21.

DIG14 — DIG14

Observation input 14 into U1302 A2 (pin 3); leaves on contact 23.

DIG15 — DIG15

Observation input 15 into U1302 A1 (pin 2); leaves on contact 24.

DIG16 — DIG16

Observation input 16 into U1303 A8 (pin 9); leaves on contact 27.

DIG17 — DIG17

Observation input 17 into U1303 A7 (pin 8); leaves on contact 28.

DIG18 — DIG18

Observation input 18 into U1303 A6 (pin 7); leaves on contact 30.

DIG19 — DIG19

Observation input 19 into U1303 A5 (pin 6); leaves on contact 31.

DIG20 — DIG20

Observation input 20 into U1303 A4 (pin 5); leaves on contact 33.

DIG21 — DIG21

Observation input 21 into U1303 A3 (pin 4); leaves on contact 34.

DIG22 — DIG22

Observation input 22 into U1303 A2 (pin 3); leaves on contact 36.

DIG23 — DIG23

Observation input 23 into U1303 A1 (pin 2); leaves on contact 37.

DIG24 — DIG24

Observation input 24 into U1304 A8 (pin 9); leaves on contact 39.

DIG25 — DIG25

Observation input 25 into U1304 A7 (pin 8); leaves on contact 40.

DIG26 — DIG26

Observation input 26 into U1304 A6 (pin 7); leaves on contact 42.

DIG27 — DIG27

Observation input 27 into U1304 A5 (pin 6); leaves on contact 43.

DIG28 — DIG28

Observation input 28 into U1304 A4 (pin 5); leaves on contact 45.

DIG29 — DIG29

Observation input 29 into U1304 A3 (pin 4); leaves on contact 46.

DIG30 — DIG30

Observation input 30 into U1304 A2 (pin 3); leaves on contact 48.

DIG31 — DIG31

Observation input 31 into U1304 A1 (pin 2); leaves on contact 49.

Circuit and PCB layout guidance
Migrated from the saved library sheet: circuit and PCB unchanged
Orb Weaver

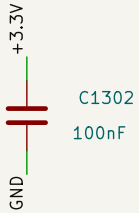
Sheet: /instrument_port/instrument_port_digital_50_dut_ffc_boundary_vertical/
File: instrument_port_digital_50_dut_ffc_boundary_vertical.kicad_sch

Title: InstrumentPort-Digital-50 DUT boundary, vertical

Size: A1	Date: 2026-10-04	Rev: Source migration 1
KiCad E.D.A. 10.0.6		id: 15/20

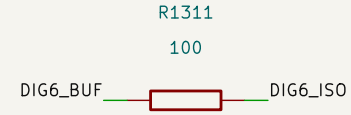
1. Octet DIG0 to DIG7: U1301

U1301 buffers DIG0 to DIG7 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18); R1305 to R1312 (100 ohm) damp each output into its connector contact.
C1302 bypasses VCC (pin 20); R1301 holds both enables (pins 1 and 19) low.



VCC pin 20 bypass, 100 nF

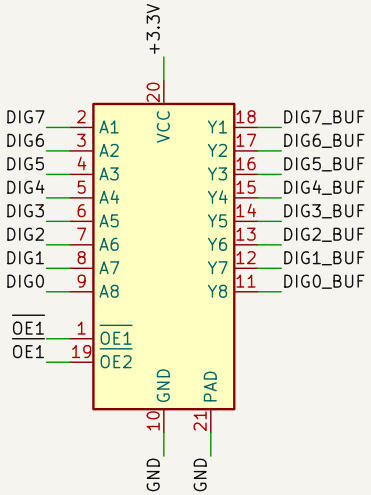
Output source damping



Output source damping

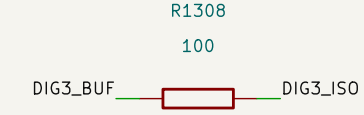
U1301

SN74LV541ARKSR

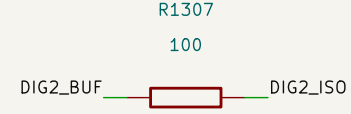


Output source damping

Output source damping

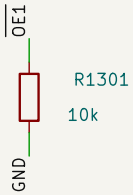


Output source damping

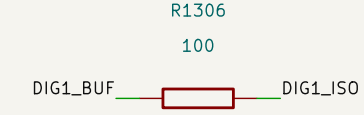


Output source damping

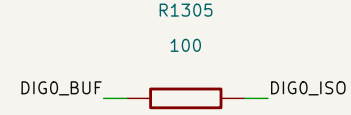
SN74LV541A octal buffer, DUT to instrument



OE1 OE1 pull-down,
10 k



Output source damping



Output source damping

PLACE: Place C1302 hard against pin 20 of U1301 with a short return to pin 10 and the exposed pad 21; R1301 near pins 1 and 19; the eight damping resistors between the Y pins and J1301, outputs toward the connector.

ROUTE: The DIG0 to DIG7 inputs are this block's ports and escape toward the board on vias; keep the Y runs short to the resistors and the resistor-to-contact runs paired with the connector's ground contacts.

2. Octet DIG8 to D

U1302 buffers DIG8 to
C1303 bypasses VCC (p

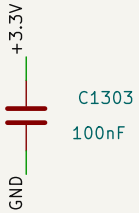
OE1/OE2 pull-dow
10 k

PLACE: Place C1303 ha
between the Y pins and

ROUTE: The DIG8 to DIG
with the connector's gro

2. Octet DIG8 to DIG15: U1302

U1302 buffers DIG8 to DIG15 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18); R1313 to R1320 (100 ohm) damp each output into its connector contact.
C1303 bypasses VCC (pin 20); R1302 holds both enables (pins 1 and 19) low.



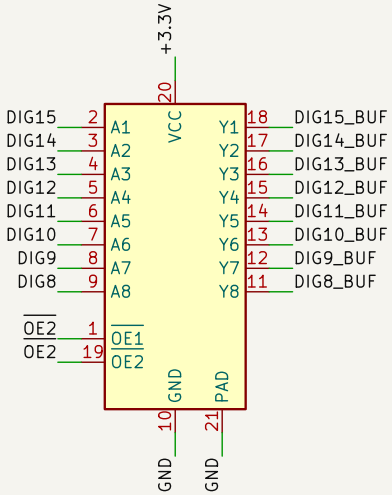
VCC pin 20 bypass, 100 nF

Output source damping

Output source damping

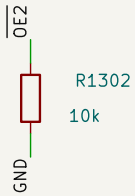
U1302

SN74LV541ARKSR



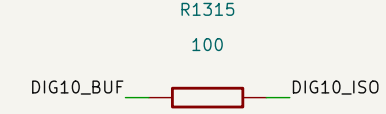
Output source damping

Output source damping



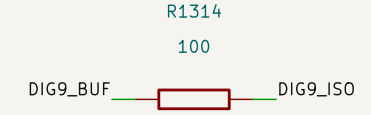
SN74LV541A octal buffer, DUT to instrument

Output source damping



Output source damping

OE1/OE2 pull-down,
10 k



Output source damping

Output source damping

PLACE: Place C1303 hard against pin 20 of U1302 with a short return to pin 10 and the exposed pad 21; R1302 near pins 1 and 19; the eight damping resistors between the Y pins and J1301, outputs toward the connector.

ROUTE: The DIG8 to DIG15 inputs are this block's ports and escape toward the board on vias; keep the Y runs short to the resistors and the resistor-to-contact runs paired with the connector's ground contacts.

3. Octet DIG16 to

U1303 buffers DIG16 to
C1304 bypasses VCC (p

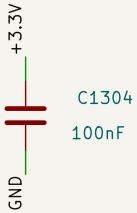
OE1/OE2 pull-dow
10 k

PLACE: Place C1304 ha
between the Y pins and

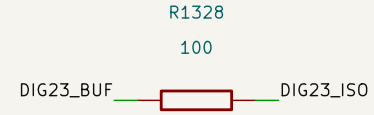
ROUTE: The DIG16 to DI
with the connector's gr

3. Octet DIG16 to DIG23: U1303

U1303 buffers DIG16 to DIG23 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18); R1321 to R1328 (100 ohm) damp each output into its connector contact. C1304 bypasses VCC (pin 20); R1303 holds both enables (pins 1 and 19) low.



VCC pin 20 bypass, 100 nF

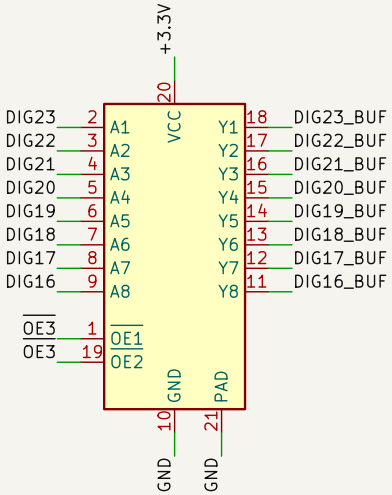


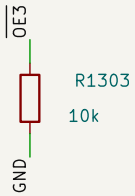
Output source damping

Output source damping

U1303

SN74LV541ARKSR



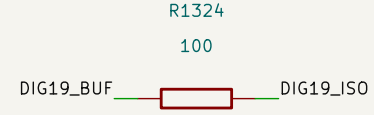


$\overline{OE1}$/$\overline{OE2}$ pull-down, 10 k

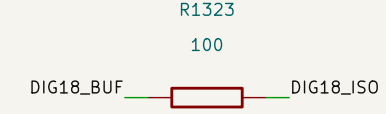
SN74LV541A octal buffer, DUT to instrument

Output source damping

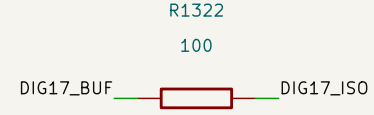
Output source damping



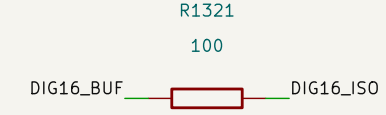
Output source damping



Output source damping



Output source damping



Output source damping

PLACE: Place C1304 hard against pin 20 of U1303 with a short return to pin 10 and the exposed pad 21; R1303 near pins 1 and 19; the eight damping resistors between the Y pins and J1301, outputs toward the connector.

ROUTE: The DIG16 to DIG23 inputs are this block's ports and escape toward the board on vias; keep the Y runs short to the resistors and the resistor-to-contact runs paired with the connector's ground contacts.

INTERFACES

+3.3V +3.3V

Always-on 3.3 V buffer

GND GND

18 connector grounds,

DIG0 DIG0

Observation input 0 into

DIG1 DIG1

Observation input 1 into

DIG2 DIG2

Observation input 2 into

DIG3 DIG3

Observation input 3 into

DIG4 DIG4

Observation input 4 into

DIG5 DIG5

Observation input 5 into

DIG6 DIG6

Observation input 6 into

DIG7 DIG7

Observation input 7 into

DIG8 DIG8

Observation input 8 into

DIG9 DIG9

Observation input 9 into

DIG10 DIG10

Observation input 10 in

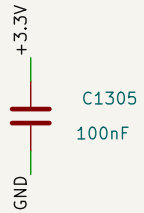
DIG11 DIG11

Observation input 11 in

DIG12 DIG12

4. Octet DIG24 to DIG31: U1304

U1304 buffers DIG24 to DIG31 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18); R1329 to R1336 (100 ohm) damp each output into its connector contact.
C1305 bypasses VCC (pin 20); R1304 holds both enables (pins 1 and 19) low.



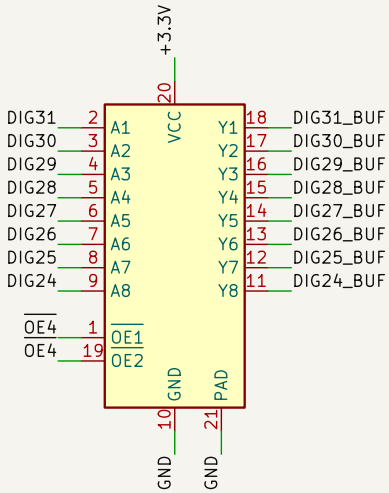
VCC pin 20 bypass, 100 nF

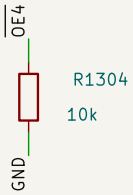
Output source damping

Output source damping

U1304

SN74LV541ARKSR





SN74LV541A octal buffer, DUT to instrument

$\overline{OE1}$/$\overline{OE2}$ pull-down, 10 k

Output source damping

Output source damping

Output source damping

Output source damping

Output source damping

Output source damping

PLACE: Place C1305 hard against pin 20 of U1304 with a short return to pin 10 and the exposed pad 21; R1304 near pins 1 and 19; the eight damping resistors between the Y pins and J1301, outputs toward the connector.

ROUTE: The DIG24 to DIG31 inputs are this block's ports and escape toward the board on vias; keep the Y runs short to the resistors and the resistor-to-contact runs paired with the connector's ground contacts.

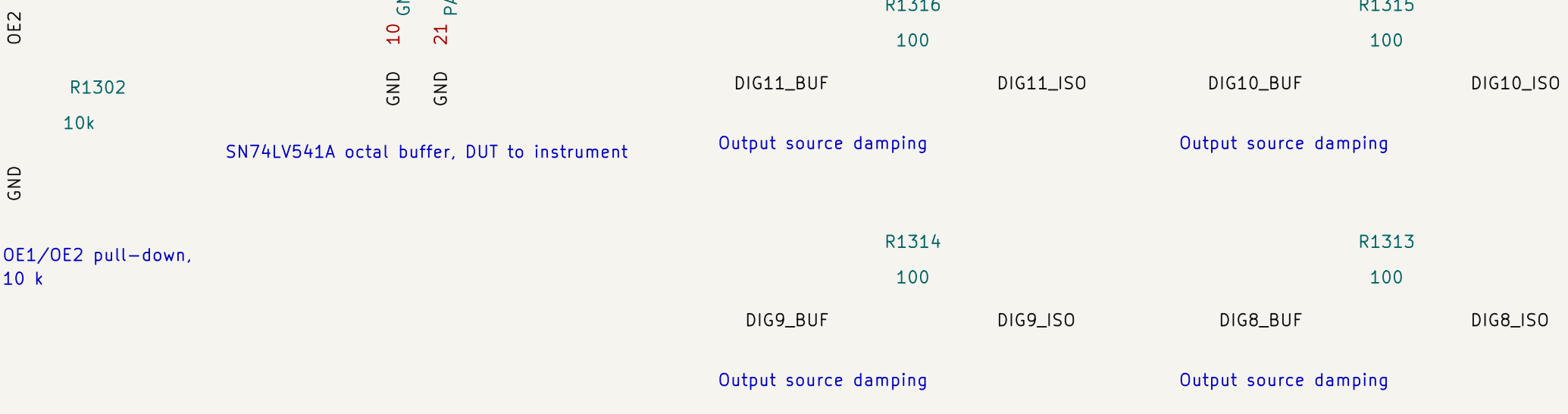
5. Rail-entry bulk b

C1301 (4.7 uF) holds the

+3.3V rail-entry bul
4.7 uF

PLACE: Place C1301 at th

ROUTE: +3.3V carries PW

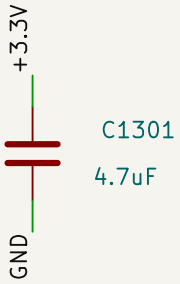


PLACE: Place C1303 hard against pin 20 of U1302 with a short return to pin 10 and the exposed pad 21; R1302 near pins 1 and 19; the eight damping resistors between the Y pins and J1301, outputs toward the connector.

ROUTE: The DIG8 to DIG15 inputs are this block's ports and escape toward the board on vias; keep the Y runs short to the resistors and the resistor-to-contact runs paired with the connector's ground contacts.

5. Rail-entry bulk bypass

C1301 (4.7 uF) holds the +3.3V rail where it enters the block; the per-package 100 nF bypasses are in the octet groups.



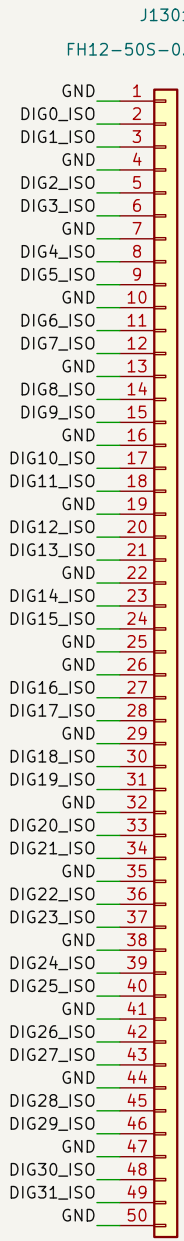
+3.3V rail-entry bulk,
4.7 uF

PLACE: Place C1301 at the supply entry of the block, not at any one package.

ROUTE: +3.3V carries PWR_3V3_LOCAL from the entry to the four VCC pins; GND is PWR_RETURN_LOCAL.

6. FFC receptacle

J1301 carries the 32 damped outputs (DIGn_ISO) on the contract's DUT contacts and the 18 grounds on one GND; the four mechanical lands carry no net.



50-contact FFC receptacle, top entry

PLACE: Vertical, top-entry receptacle at the board edge, latch away from the buffers; verify pin 1 and the contact face on the real part.

ROUTE: Pair each DIGn_ISO with its neighbouring ground contact and tie all 18 grounds into one GND copper under the connector; land pattern dual-row staggered at 1.0 mm within each row.

Observation input 13 into U1

DIG14 DIG14

Observation input 14 into U1

DIG15 DIG15

Observation input 15 into U1

DIG16 DIG16

Observation input 16 into U1

DIG17 DIG17

Observation input 17 into U1

DIG18 DIG18

Observation input 18 into U1

DIG19 DIG19

Observation input 19 into U1

DIG20 DIG20

Observation input 20 into U1

DIG21 DIG21

Observation input 21 into U1

DIG22 DIG22

Observation input 22 into U1

DIG23 DIG23

Observation input 23 into U1

DIG24 DIG24

Observation input 24 into U1

DIG25 DIG25

Observation input 25 into U1

DIG26 DIG26

Observation input 26 into U1

DIG27 DIG27

Observation input 27 into U1

INTERFACES

+3.3V — +3.3V

Always-on 3.3 V buffer supply (VCC pins 20); never reaches the cable.

GND — GND

18 connector grounds, buffer GND pins and pads, bypass and OE pull-down return.

DIG0 — DIG0

Observation input 0 into U1301 A8 (pin 9); leaves on contact 2.

DIG1 — DIG1

Observation input 1 into U1301 A7 (pin 8); leaves on contact 3.

DIG2 — DIG2

Observation input 2 into U1301 A6 (pin 7); leaves on contact 5.

DIG3 — DIG3

Observation input 3 into U1301 A5 (pin 6); leaves on contact 6.

DIG4 — DIG4

Observation input 4 into U1301 A4 (pin 5); leaves on contact 8.

DIG5 — DIG5

Observation input 5 into U1301 A3 (pin 4); leaves on contact 9.

DIG6 — DIG6

Observation input 6 into U1301 A2 (pin 3); leaves on contact 11.

DIG7 — DIG7

Observation input 7 into U1301 A1 (pin 2); leaves on contact 12.

DIG8 — DIG8

Observation input 8 into U1302 A8 (pin 9); leaves on contact 14.

DIG9 — DIG9

Observation input 9 into U1302 A7 (pin 8); leaves on contact 15.

DIG10 — DIG10

Observation input 10 into U1302 A6 (pin 7); leaves on contact 17.

DIG11 — DIG11

Observation input 11 into U1302 A5 (pin 6); leaves on contact 18.

DIG12 — DIG12

Observation input 12 into U1302 A4 (pin 5); leaves on contact 20.

DIG13 — DIG13

Observation input 13 into U1302 A3 (pin 4); leaves on contact 21.

DIG14 — DIG14

Observation input 14 into U1302 A2 (pin 3); leaves on contact 23.

DIG15 — DIG15

Observation input 15 into U1302 A1 (pin 2); leaves on contact 24.

DIG16 DIG16

Observation input 16 into U1303 A8 (pin 9); leaves on contact 27.

DIG17 DIG17

Observation input 17 into U1303 A7 (pin 8); leaves on contact 28.

DIG18 DIG18

Observation input 18 into U1303 A6 (pin 7); leaves on contact 30.

DIG19 DIG19

Observation input 19 into U1303 A5 (pin 6); leaves on contact 31.

DIG20 DIG20

Observation input 20 into U1303 A4 (pin 5); leaves on contact 33.

DIG21 DIG21

Observation input 21 into U1303 A3 (pin 4); leaves on contact 34.

DIG22 DIG22

Observation input 22 into U1303 A2 (pin 3); leaves on contact 36.

DIG23 DIG23

Observation input 23 into U1303 A1 (pin 2); leaves on contact 37.

DIG24 DIG24

Observation input 24 into U1304 A8 (pin 9); leaves on contact 39.

DIG25 DIG25

Observation input 25 into U1304 A7 (pin 8); leaves on contact 40.

DIG26 DIG26

Observation input 26 into U1304 A6 (pin 7); leaves on contact 42.

DIG27 DIG27

Observation input 27 into U1304 A5 (pin 6); leaves on contact 43.

DIG28 DIG28

Observation input 28 into U1304 A4 (pin 5); leaves on contact 45.

DIG29 DIG29

Observation input 29 into U1304 A3 (pin 4); leaves on contact 46.

DIG30 DIG30

Observation input 30 into U1304 A2 (pin 3); leaves on contact 48.

DIG31 DIG31

Observation input 31 into U1304 A1 (pin 2); leaves on contact 49.

OPERATION

DUT side of the InstrumentPort-Digital-50 profile (board-interfaces docs/instrument-port-digital.md, draft v0.1). Direction is a hardware property, DUT to instrument only: DIGn enters U1301 to U1304 (DIG0 to 7, 8 to 15, 16 to 23, 24 to 31, each octet one package, A8 down to A1), leaves on Y8 to Y1 through 100 ohm damping (R1305 to R1336) onto J1301. The cable carries no supply, reference, enable or stimulus.

Pin mapping is the contract's DUT table and is not mirrored: channel n lands on contact 2 + n + floor(n/2) + floor(n/16), DIG0 on contact 2, DIG31 on contact 49, the 18 grounds on 1, 4, 7, ... 47, 50 with the 25/26 double ground at the bank boundary. The mirror lives on instrument_port_digital_50_adapter_ffc_boundary_vertical; mirroring both ends cancels, and ERC and DRC cannot see it.

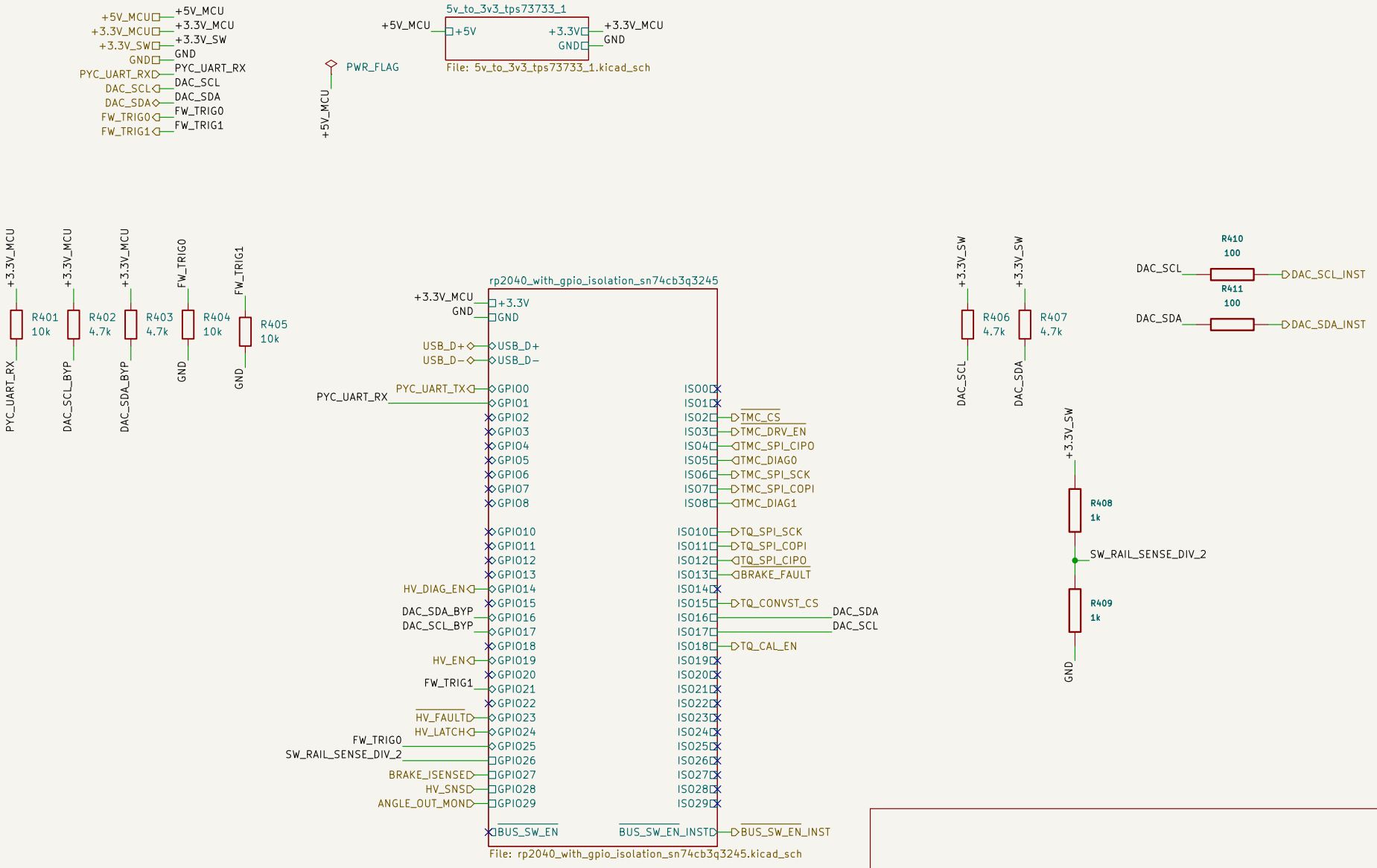
Enabled by hardware default, no disable at all: both active-low enables of each package share one net held low by its 10 k pull-down (R1301 to R1304; at most about 0.1 V from the two inputs' leakage against the 0.99 V VIL), so observation works with the MCU in reset or unprogrammed. The contract permits this since 2026-09-15; do not re-add a control as a fix.

Supply: the always-on 3.3 V rail on VCC (pins 20); SN74LV541A runs 2 to 5.5 V, drives +/-8 mA at 3.3 V, inputs tolerate 0 to 5.5 V with Ioff <= 5 uA unpowered, VIH 2.31 V, VIL 0.99 V, edges <= 100 ns/V, not a Schmitt input. C1302 to C1305 (100 nF) bypass each pin 20; C1301 (4.7 uF, X5R 0402, well below nameplate at 3.3 V bias) is the one rail-entry bulk, not a fifth per-package bypass.

The 100 ohm damping bounds a hard short of one output to GND at 33 mA, inside the +/-35 mA per-output absolute maximum, and damps edges into the cable; it is not short-circuit protection. Input bias is board-specific and not in this block: every unused DIGn must be tied at the board. Attach and remove the FFC with target power off; J1301 is rated 20 mating cycles, so break the link at the instrument end.

DESIGN CONTRACT

DUT-side InstrumentPort-Digital-50 with integrated read-only buffering, on a VERTICAL, top-entry 50-contact ZIF connector: Hirose FH12-50S-0.5SVA(54), OW-CONN-FH12-50S-0-5SVA-54, LCSC C597991, 0.5mm pitch, symbol Conn_01x50, footprint orb_weaver_connectors:Hirose_FH12-50S-0.5SVA_1x50-4MP_P0.5mm_Vertical; the four mechanical lands are unnumbered pads and carry no net. Thirty-two channels through four SN74LV541ARKSR octal buffers (OW-MISC-SN74LV541ARKSR, C7364695, symbol orb_weaver_misc:SN74LV541ARKSR, footprint orb_weaver_smd:Texas_RKS0020A_VQFN-20-1EP_2.5x4.5mm_P0.5mm_EP1x3mm, exposed pad 21 to GND), grouped DIG0-7 / DIG8-15 / DIG16-23 / DIG24-31 to match the 13-contact octet windows. The 541 is flow-through: input pin p pairs with output pin 20-p, A1(2) to Y1(18) through A8(9) to Y8(11). DIRECTION IS A HARDWARE PROPERTY: DUT to instrument only. The cable carries no supply, no voltage reference, no enable and no stimulus, and nothing in this block may be driven by the instrument. PIN MAPPING IS THE CONTRACT'S DUT TABLE AND IS NOT MIRRORED: channel n lands on pin 2 + n + floor(n/2) + floor(n/16), so DIG0 is pin 2 and DIG31 is pin 49, with all 18 grounds on pins 1, 4, 7, 10, 13, 16, 19, 22, 25, 26, 29, 32, 35, 38, 41, 44, 47 and 50. THE MIRROR LIVES ON THE ADAPTER, NOT HERE. instrument_port_digital_50_adapter_ffc_boundary_vertical is pre-mirrored to 51-n so that the expected reversing assembly - same-side Type A FFC with a vertical FH12 at both ends, connectors rotated 180 degrees - delivers DIGn to DIGn. Mirroring both ends cancels and channels arrive as DIG31-n. The ground pattern is palindromic under 51-n, so a mirrored map lands every ground identically and every net stays driven and terminated: ERC, DRC and design_block_tools.py check are ALL BLIND to this error, and only a pin-by-pin netlist comparison or continuity on the real cable catches it. Per-output source damping is 100 ohms, OW-PASS-0402WGF1000TCE. That value is chosen as the smallest standard one that bounds a hard short to ground inside the LV541A's +/-35mA output absolute maximum even crediting the driver with zero impedance (3.3V/100R = 33mA); 68R gives 49mA, 47R gives 70mA, and the legacy 33R gives 100mA. It is NOT short-circuit protection and does not cover every fault. DEFAULT-ENABLED BY HARDWARE, AND THERE IS NO DISABLE AT ALL: both active-low OE inputs of each package share one net held low by a single 10k pull-down - R1301 through R1304, one per package - so observation works with the MCU held in reset, unprogrammed or unable to boot, and the port cannot be muted without desoldering. There is no manual jumper, no firmware link and no OE port. The owning contract was relaxed on 2026-09-15 from requiring manual disabling to permitting none, so this conforms; the reasoning and the retained future option are in kicad-libs/docs/digital-instrument-port-design-blocks.md under 'No disable control, and why'. DO NOT re-add a control as an oversight fix. Shared 10k is verified against aggregate leakage: 2 x 5uA max gives 0.1V against a 0.99V VIL. If a noise investigation ever needs a mute, detaching the FFC bounds the cable's contribution but NOT the buffers', which keep switching into their board-side traces and damping resistors; lift the 100R resistors on the suspect channels instead. SUPPLY FROM THE BOARD'S ALWAYS-ON 3.3V RAIL, independent of firmware, HV_EN and every switched domain; a buffer on a switched rail cannot observe the domain it is powering down with. DECOUPLING is one 100nF per package, C1302 through C1305, hard against each pin 20 with a short return, plus one 4.7uF rail-entry bulk, C1301 / OW-CAP-4U7-0402-X5R-16V, at the supply entry. C1301 is NOT a fifth per-IC bypass - do not 'fix' its distance to any package. Simultaneous-switching budget: 32 x 50pF x 3.3V = 5.3nC per all-channel edge, about 1mV of droop against the combined local reservoir. Expect meaningfully less than 4.7uF at 3.3V bias - a 4.7uF X5R in an 0402 derates hard - so treat the nameplate value as nominal, not measured. INPUT BIAS IS BOARD-SPECIFIC AND IS NOT IN THIS BLOCK: there is no universal pull-down, because SPI selects, open-drain buses and switched-domain taps each need different bias, and pulls that must read HIGH on a switched net reference the switched rail, never the always-on one. Every unused input must be explicitly tied at the board. LV541A at 3.3V needs VIH >= 2.31V and VIL <= 0.99V with transitions <= 100 ns/V; it is 0-5.5V input tolerant with 2pF typical input capacitance and Ioff <= 5uA at VCC=0. It is NOT Schmitt-triggered and NOT a comparator: do not route a raw analog node through it for a timing witness, and do not treat a clean legacy LVC125A capture as LV541A qualification. OE would disable outputs only - it never removes input loading or makes a floating input acceptable, which is part of why no mute was fitted. Requires straight-ended 0.30 +/-0.05mm FFC with gold contacts, at least 2mm exposed contact and 3mm reinforcement; retention-eared cable is NOT qualified for this connector. Rated 20 mating cycles, so prefer breaking the link at the instrument end, and attach or remove the cable with target power off unless the actual assembly is hot-plug qualified. Profile is InstrumentPort-Digital-50 draft v0.1, UNQUALIFIED: no measured rate, delay, skew, loading or power-state limit has been established. Marker/beacon channel indices are NOT frozen, with DIG0/DIG1 the current recommendation over the earlier DIG14/DIG15. Pairs with instrument_port_digital_50_adapter_ffc_boundary_vertical; the analyzer-specific channel map belongs to la5032_connector_boundary, not here. GROUNDED INPUTS ARE THE BOARD'S COPPER: the inputs are this block's ports, so a board that grounds unused DIGn channels draws one 0.20 mm track per grounded LV541A pad column straight into that package's thermal pad on F.Cu, before autorouting; Freerouting will not run a track along a row of same-net 0.5 mm-pitch pads and left those groups unrouted on every camera-board run (layout conventions 11a). Since 2026-09-29 every DIGn also ends at its own escape via above the pad row, so a board may instead tie an unused channel to ground at that via; either way the grounding copper is the board's, never the block's. FLOOR COPPER IS DECLARED: the 0.10 mm gaps between the 32 damping resistors and the LV541A pins (2026-09-26) and between each DIGn escape stub and the escape via beside it (2026-09-29) are wrapped in BLOCK_FLOOR rule areas, so a consuming board sees no clearance findings from this block under the shared rules; a board wanting 0.20 mm inside the block re-routes the block, not the rule (layout conventions 12).



Janelia Research Campus		
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RP2040 core with GPIO isolation | flash, 12 MHz crystal, BOOTSEL and RUN, four SN74CB3Q3245 bus switches

RP2040 controller core and its GPIO isolation in one block: the full rp2040 core — W25Q128JVPIQ QSPI flash, 12 MHz ABM8 crystal, decoupling, BOOTSEL and RUN switches — plus four SN74CB3Q3245RGYR 8-channel bidirectional FET bus switches, with all 29 MCU-to-switch connections made inside the block so that routing is placed once instead of re-drawn per board.

Matching net labels are connected. Group order explains function: PCB placement priorities are stated below.

1. Controller core

U601: QSPI to U602, IOVDD through R601/R602. GPIO0–29 to the switches' B side; GPIO9 as the enable. +3.3V: C603 (1 uF) bulk at VREG_IN and seven 100 nF for the nine +3.3V supply pins: C605 at IOVDD 1, C614 at IOVDD 10, C609 at IOVDD 22, C607 at IOVDD 33, and C610, C611 and C613 at the corner of IOVDD 42, ADC_AVDD 43, VREG_IN 44, USB_VDD 48 and IOVDD 49, where the routed PCB flies the pairing. +1.1V: C606 at DVDD 23, C608 at VREG_VOUT 45, C604 (1 uF) beside DVDD 50.

Controller core: GPIO9 is the switch enable
C605: IOVDD pin 1 bypass; 100 nF. C607: IOVDD pin 33 bypass; 100 nF. C609: IOVDD pin 22 bypass; 100 nF. C610: Corner bypass, pins 42–44, 48, 49; 100 nF. C614: IOVDD pin 10 bypass; 100 nF; one per IOVDD pins 1, 10, 22, 33, 42, 49
C606: +1.1V bulk beside DVDD pin 50; 1 uF. C606: DVDD pin 23 bypass; 100 nF; one per DVDD pins 23, 50
C608: VREG_VOUT pin 45 bypass; 100 nF
C611, C613: Corner bypass, pins 42–44, 48, 49; 100 nF
R605: QSPI_SS pull-up; 10 k
C608 VREG_VOUT pin 45 bypass; 100 nF

PLACE: Exposed pad to GND copper with vias; GPIO escapes toward the switches.

PLACE: Each capacitor hard against its pin with the shortest return to the GND pad (57); the corner pins 42 to 44, 48 and 49 share C610, C611 and C613.

ROUTE: Switched signals lower on the A side; raw GPIO ports are the same B-side traces.

ROUTE: +1.1V stays inside the block; the switches' VCC pins have their own capacitors.

2. Clock

Y601 (12 MHz) between XIN and XOUTB with 15 pF loads; R603 (1 k) in the XOUT leg.

12 MHz crystal
C601, C602: Crystal load capacitors (15 pF, C0G)

Crystal drive limit; 1 k, XOUT

PLACE: All four at pins 20 and 21 over a local ground; nothing else beside the crystal.

ROUTE: Short traces, no vias. GND fill around; keep switching lines away.

3. QSPI flash

U602 (W25Q128JVPIQ) on QSPI_SCLK, SD0–SD3 and QSPI_SS; C612 decouples pin 8.

QSPI boot flash, 16 MB
C612: U602 VCC pin 8 bypass, 100 nF

PLACE: Next to pins 51–56. C612 at pin 8, pad 9 to GND.

ROUTE: Six short QSPI lines of similar length; up to 133 MHz.

4. USB

R601/R602 (27 ohm) between the pads (D+, D–) and the USB_D+/USB_D– ports.

USB_DP series, 27 R

USB_DM series, 27 R

PLACE: At pins 46 and 47; the ports leave outside them.

ROUTE: USB_HS class, routed as a pair; no stubs.

5. BOOTSEL and RUN

R605 pulls QSPI_SS up. SW601 grounds USB_BOOT via R606; SW602 grounds RUN. C615 filters it.

BOOTSEL switch, grounds USB_BOOT

RUN switch, grounds RUN pin 26
C615: RUN pin 26 filter, 100 nF

BOOTSEL series, 1 k, QSPI_SS to USB_BOOT

PLACE: SW602 beside SW601 on one edge (hold BOOTSEL, tap RUN); C615 hard against pin 26.

ROUTE: RUN is DC with an internal pull-up; length is free, noise is not.

6. Bus switch enable

R607 (7.87 k) holds BUS_SW_EN high at reset; R604 (1 k) makes BUS_SW_EN_INST.

BUS_SW_EN pull-up; bus isolated at reset

BUS_SW_EN instrument tap, 1 k

PLACE: R607 near pin 12; R604 toward the instrument escape.

ROUTE: One net to all four pin 19 inputs.

7. Bus switches U603 and U604

U603 and U604 pass GPIO0–7 and GPIO8, GPIO10–15 to the ISO ports (B side MCU; A side switched): C616 (U603) and C617 (U604) decouple pin 20. U604's channel 2 spare (B2 pin 17 to GND, A2 pin 3 open).

FET bus switch, GPIO0–7 to ISO0–7
C616: U603 VCC pin 20 bypass; 100 nF

FET bus switch, GPIO8,10–15 to ISO8,10–15
C617: U604 VCC pin 20 bypass; 100 nF

PLACE: C616 and C617 at pin 20 with short returns to pin 10 and the EPAD.

ROUTE: B side to the MCU, A side to the ISO port vias; EPADs to GND.

8. Bus switches U605 and U606

U605 and U606 pass GPIO16–23 and GPIO24–29 to the ISO ports (B side MCU; A side switched): C618 (U605) and C619 (U606) decouple pin 20. U606 channels 7 and 8 spare (B7/B8 pins 12/11 to GND. A7/A8 pins R/F open).

FET bus switch, GPIO16–23 to ISO16–23
C618: U605 VCC pin 20 bypass; 100 nF

FET bus switch, GPIO24–29 to ISO24–29
C619: U606 VCC pin 20 bypass; 100 nF

PLACE: C618 and C619 at pin 20 with short returns to pin 10 and the EPAD.

ROUTE: B side to the MCU, A side to the ISO port vias; EPADs to GND.

OPERATION

Bit parts: GPIO0–8 and GPIO15–29 are the raw pads, ISO0–8 and ISO10–29 the same pads behind one switch channel each; BUS_SW_EN and its tap BUS_SW_EN_INST leave for observation only; GPIO9 (pin 12) is the enable and has no GPIO or ISO port. Per Index, GPIOn and ISOn are one node when enabled; wire one or the other, by the far end's power domain.

The ISO side is a bare pass gate: no level shift, buffer or protection. Switch I/O is rated to 5.5 V but the MCU pad behind it is limited to IOVDD + 0.3 V; pulls on the switched side reference the switched rail, never +3.3V. Unused ports get no-connect flags on the placing sheet.

Enable: GPIO9 drives BUS_SW_EN (active low) to the four OE pins: R607 (7.87 k) keeps the bus isolated from power-on; R604 (1 k) makes the instrument tap. Lan 14 ns, tpls 13 ns max at 3.3 V. Firmware: isolate, drop the rail: raise, confirm, connect.

Supply: always-on +3.3V for IOVDD, USB_VDD, ADC_AVDD, VREG_IN, the flash and the switches' VCC (2.3–3.6 V); the regulator makes +1.1V for DVDD. Each switch draws 1 mA typ, 2 mA max on or off (about ¼ mA typ, 8 mA max total). Isolation rests on the enable, not on 1uff.

Core: Y601 12 MHz with C601/C602 (15 pF) and R603 (1 k); W25Q128 on QSPI; BOOTSEL grounds USB_BOOT (R606 1 k to QSPI_SS, R605 10 k up); RUN grounds pin 26 (C615, internal pull-up only), does not reset the flash, releases GPIO to high-Z, SWD is not exposed. Two instances need separate sheets.

DESIGN CONTRACT

RP2040 controller core and its GPIO isolation in one block: the full rp2040 core (W25Q128JVPIQ QSPI flash, 12 MHz ABM8 crystal, decoupling, BOOTSEL and RUN switches) plus four SN74CB3Q3245RGYR 8-channel bidirectional FET bus switches, with all 29 MCU-to-switch connections made inside the block so that routing is placed once instead of re-drawn per board. Derived from rp2040, which remains canonical for an MCU with no isolation and is the upstream for the core half. Fix core circuitry there first, then refresh here. The switch half has no upstream; fix here. This block replaces the retired isolation-only companion rp2040_gpio_isolation_ac7ec63a3245 outright and is the only isolated form. Core parts are positionally identical to rp2040; DO NOT place this block alongside rp2040. It already contains that core. Designators are the 600s band.

Decoupling: C603 (1 uF) is the +3.3V bulk at VREG_IN and seven 100 nF serve the nine +3.3V supply pins: C605 at IOVDD 1, C614 at IOVDD 10, C609 at IOVDD 22, C607 at IOVDD 33, and C610, C611 and C613 at the corner of IOVDD 42, ADC_AVDD 43, VREG_IN 44, USB_VDD 48 and IOVDD 49, where the routed PCB flies the pairing. C612 bypasses the flash VCC (U602 pin 8); C615 to C619 bypass VCC pin 20 of U603 to U606 in turn. The regulator's +1.1V has C606 at DVDD 23, C608 at VREG_VOUT 45 and C606 (1 uF) beside DVDD 50.

1. THE INTERFACE IS SIX PORTS AND GPIO9 IS NOT ONE OF THEM: 29 raw MCU ports GPIO0–GPIO8 and GPIO10–GPIO29, 29 switched ports ISO0–ISO8 and ISO10–ISO29, BUS_SW_EN, +3.3V, GND, and the enable BUS_SW_EN with its instrument tap BUS_SW_EN_INST, both for observation only. GPIO9 is spent on the bus—switch enable and has no GPIO or ISO port; there is no ISO9 and no separate OE port. Any board placing this block gives up GPIO9 and inherits BUS_SW_EN as a firmware constant. tms51x0-driver-dev-pcb puts the same signal on GPIO19 and does NOT use this block; do not align them.

2. GPIOn AND ISOn ARE THE SAME NODE WHENEVER THE BUS IS ENABLED. Per index they are an either/or, not a fan-out. Wiring both shorts whatever sits on the always-on side to whatever sits on the switched side the instant firmware pulls BUS_SW_EN low, and neither ERC nor DRC will flag it. Pick one per signal: GPIOn for a node that must survive sleep, ISOn for one that may be powered down. Mixing them on one net is a latent fault.

3. THE ISO SIDE IS A BARE PASS GATE: no level shift, no buffer, no protection, no direction. Switch I/O is rated 0–5.5 V but the other end of every channel is an RP2040 pad limited to IOVDD+0.3 V, so a 5 V pull-up or a 5 V driver on an ISO pin damages the MCU, not the switch. Do not give ISO ports a direction shape; the gate is symmetric and they are passive by construction. Pull-ups and pull-downs on the switched side must reference the SWITCHED rail, never +3.3V, or they back-power the dead domain through the fet chip's input clamps inside a block where the bus switch cannot see it.

4. THE ENABLE IS THE MCU'S, ACTIVE LOW, AND DISABLED BY DEFAULT: GPIO9 drives BUS_SW_EN to all four pin 19 inputs, with R607 7.87 k to +3.3V so the bus is isolated at power-on until firmware asserts it. The enable cannot sit behind the switch it enables, and an MCU must be able to connect a bus that is currently disconnected, so the board never sources its BUS_SW_EN leaves the block only to be observed, and BUS_SW_EN_INST through R604 (1 k) to its instrument tap. NEVER drive it from the board; a second driver fights the MCU and the pull-up is the only thing defining the reset state. Sequencing is board policy and firmware must follow it: isolate first, then drop the rail: raise the rail, confirm it, then connect last. Lan 14 ns max and tzls 13 ns max at 3.3 V, so the disconnect is deterministic and instantaneous relative to the rail.

5. SUPPLY IS THE ALWAYS-ON 3.3 V RAIL, DELIBERATELY, AND THERE IS NO 1uff SECOND LINE OF DEFENCE. One +3.3V port feeds the MCU, all four VCC pins and the pull-up. Powering the switches from the switched domain would give free isolation through 1uff at VCC=0 and cost no GPIO, and is REJECTED. It hands sequencing to a rail ramp, removes the ability to isolate before powering down, and leaves the always-on MCU driving an enable input on an unpowered part. 1uff is specified for the data terminals (VCC=0: 0 to 5.5 V, 1 uA max) with no control-input condition stated, and VCC=0 is characterized only over VCC 2.3–3.6 V. Isolation therefore rests entirely on the MCU holding BUS_SW_EN high, which R607 makes the reset default. This contradicts the catalog note on DW-MSG-SNTHCB3Q3245RGYR, which recommends switched-domain power; the block and the boards with, see kicad-libs docs/rp2040-gpio-isolation-design-block-plan.md.

6. THE PACKAGE IS RGY-20 (VQFN-20, 3.5 mm x 4.5 mm typ and 2 mA max per package with the switch ON OR OFF, because the charge pump runs regardless, so four packages draw about 4 mA typ and 8 mA max continuously from the always-on rail even with every channel isolated. That is the price of 5 V coverage and it is accepted.

7. ONE CHANNEL PER GPIO, AND THREE SPARES. Pairing on the RGY-20 package is A_n = pin (n+1) and B_n = pin (19−n): A 1E THE SWITCHED SIDE AND B IS THE MCU SIDE. U603 carries GPIO0–GPIO7 to ISO0–ISO7, U604 GPIO8 and GPIO10–GPIO15 to ISO8 and ISO10–ISO15, U605 GPIO16–GPIO23 to ISO16–ISO23, U606 GPIO24–GPIO29 to ISO24–ISO29. The three unused channels are U604 channel 2, freed by the enable, and U606 channels 7 and 8. Treatment for every spare is the same and is not arbitrary: MCU-side B pin to GND, A pin left open; so no node floats on the always-on rail and no switched-side pin is a hidden hard ground.

8. THE BOARD OWNS THE BUS_SW_EN NET. The block exports it and its instrument tap; the board ties them no-connect rather than leaving them dangling. Unused channels need nothing else: the pass gate has no internal buffer, so an open data pin is not a floating CMOS input. Bus terminations, input bias and instrument taps are board-level or belong to the far-end block, never here. USB_D+ and USB_D– leave OUTSIDE the 27 ohm series resistors R601 and R602; do not add more series resistance at the board.

9. CORE GOTCHAS CARRIED FROM rp2040 (full text in that block's description): SWD IS NOT EXPOSED; pins 24 and 25 are deliberately open and no debug-connector footprint exists in the libraries, so this block offers no debug header. Place SW602 (RUN) physically adjacent to SW601 (BOOTSEL) on the same board edge or the one-handed hold-BOOTSEL-tap-RUN recovery gesture becomes a two-handed operation on an isolated board. rp_C615 is the exception to that adjacency: it decouples RUN and belongs hard against pin 26 with a short return. RUN has no external pull-up and needs none (the internal 50–80 k is the only one) and needs neither the 1 k series nor the 10 k pull-up that belong to BOOTSEL's QSPI_SS. A RUN reset does NOT reset U602, so a warm reset that hangs where a power cycle works is the flash. RUN also releases every GPIO to high-Z, so the polling board must ensure each domain it controls defaults to safe on MCU reset.

10. TWO INSTANCES NEED SEPARATE SHEETS or the internal nets (RUN, USB_BOOT, QSPI_SS, XIN, XOUT, XOUTB, +1.1V, 0+ and 0–) silently merge between copies.

INTERFACES

+3.3V — Always-on 3.3 V for the MCU, flash, four switches and pull-ups.

GND — Common return: core, flash, switches (GND, EPAD), crystal, switch frames.

GPIO0 — Raw MCU GPIO0. 3.3 V: one node with ISO0 via U603 B1 (pin 18) when enabled.

GPIO1 — Raw MCU GPIO1. 3.3 V: one node with ISO1 via U603 B2 (pin 17) when enabled.

GPIO2 — Raw MCU GPIO2. 3.3 V: one node with ISO2 via U603 B3 (pin 16) when enabled.

GPIO3 — Raw MCU GPIO3. 3.3 V: one node with ISO3 via U603 B4 (pin 15) when enabled.

GPIO4 — Raw MCU GPIO4. 3.3 V: one node with ISO4 via U603 B5 (pin 14) when enabled.

GPIO5 — Raw MCU GPIO5. 3.3 V: one node with ISO5 via U603 B6 (pin 13) when enabled.

GPIO6 — Raw MCU GPIO6. 3.3 V: one node with ISO6 via U603 B7 (pin 12) when enabled.

GPIO7 — Raw MCU GPIO7. 3.3 V: one node with ISO7 via U603 B8 (pin 11) when enabled.

GPIO8 — Raw MCU GPIO8. 3.3 V: one node with ISO8 via U604 B1 (pin 18) when enabled.

GPIO10 — Raw MCU GPIO10. 3.3 V: one node with ISO10 via U604 B3 (pin 16) when enabled.

GPIO11 — Raw MCU GPIO11. 3.3 V: one node with ISO11 via U604 B4 (pin 15) when enabled.

GPIO12 — Raw MCU GPIO12. 3.3 V: one node with ISO12 via U605 B5 (pin 13) when enabled.

GPIO13 — Raw MCU GPIO13. 3.3 V: one node with ISO13 via U604 B6 (pin 13) when enabled.

GPIO14 — Raw MCU GPIO14. 3.3 V: one node with ISO14 via U604 B7 (pin 12) when enabled.

GPIO15 — Raw MCU GPIO15. 3.3 V: one node with ISO15 via U604 B8 (pin 11) when enabled.

GPIO16 — Raw MCU GPIO16. 3.3 V: one node with ISO16 via U605 B1 (pin 18) when enabled.

GPIO17 — Raw MCU GPIO17. 3.3 V: one node with ISO17 via U605 B2 (pin 17) when enabled.

GPIO18 — Raw MCU GPIO18. 3.3 V: one node with ISO18 via U605 B3 (pin 16) when enabled.

GPIO19 — Raw MCU GPIO19. 3.3 V: one node with ISO19 via U605 B4 (pin 15) when enabled.

GPIO20 — Raw MCU GPIO20. 3.3 V: one node with ISO20 via U605 B5 (pin 14) when enabled.

GPIO21 — Raw MCU GPIO21. 3.3 V: one node with ISO21 via U605 B6 (pin 13) when enabled.

GPIO22 — Raw MCU GPIO22. 3.3 V: one node with ISO22 via U605 B7 (pin 12) when enabled.

GPIO23 — Raw MCU GPIO23. 3.3 V: one node with ISO23 via U605 B8 (pin 11) when enabled.

GPIO24 — Raw MCU GPIO24. 3.3 V: one node with ISO24 via U606 B1 (pin 18) when enabled.

GPIO25 — Raw MCU GPIO25. 3.3 V: one node with ISO25 via U606 B2 (pin 17) when enabled.

GPIO26/ADC0 — Raw MCU GPIO26/ADC0. 3.3 V: one node with ISO26 via U606 B3 (pin 16) when enabled.

GPIO27/ADC1 — Raw MCU GPIO27/ADC1. 3.3 V: one node with ISO27 via U606 B4 (pin 15) when enabled.

GPIO28/ADC2 — Raw MCU GPIO28/ADC2. 3.3 V: one node with ISO28 via U606 B5 (pin 14) when enabled.

GPIO29/ADC3 — Raw MCU GPIO29/ADC3. 3.3 V: one node with ISO29 via U606 B6 (pin 13) when enabled.

USB_D+ — USB D+ outside R601 (27 ohm). USB_HS class.

USB_D– — USB D– outside R602 (27 ohm). USB_HS class.

BUS_SW_EN — GPIO9 drives all four OE. R607 holds it high (isolated) at reset. Never drive it.

ISO0 — Switched GPIO0. U603 A1 (pin 2): bare pass gate, 3.3 V domain only.

ISO1 — Switched GPIO1. U603 A2 (pin 3): bare pass gate, 3.3 V domain only.

ISO2 — Switched GPIO2. U603 A3 (pin 4): bare pass gate, 3.3 V domain only.

ISO3 — Switched GPIO3. U603 A4 (pin 5): bare pass gate, 3.3 V domain only.

ISO4 — Switched GPIO4. U603 A5 (pin 6): bare pass gate, 3.3 V domain only.

ISO5 — Switched GPIO5. U603 A6 (pin 7): bare pass gate, 3.3 V domain only.

ISO6 — Switched GPIO6. U603 A7 (pin 8): bare pass gate, 3.3 V domain only.

ISO7 — Switched GPIO7. U603 A8 (pin 9): bare pass gate, 3.3 V domain only.

ISO8 — Switched GPIO8. U604 A1 (pin 2): bare pass gate, 3.3 V domain only.

ISO10 — Switched GPIO10. U604 A3 (pin 4): bare pass gate, 3.3 V domain only.

ISO11 — Switched GPIO11. U604 A4 (pin 5): bare pass gate, 3.3 V domain only.

ISO12 — Switched GPIO12. U604 A5 (pin 6): bare pass gate, 3.3 V domain only.

ISO13 — Switched GPIO13. U604 A6 (pin 7): bare pass gate, 3.3 V domain only.

ISO14 — Switched GPIO14. U604 A7 (pin 8): bare pass gate, 3.3 V domain only.

ISO15 — Switched GPIO15. U604 A8 (pin 9): bare pass gate, 3.3 V domain only.

ISO16 — Switched GPIO16: U605 A1 (pin 2): bare pass gate, 3.3 V domain only.

ISO17 — Switched GPIO17: U605 A2 (pin 3): bare pass gate, 3.3 V domain only.

ISO18 — Switched GPIO18: U605 A3 (pin 4): bare pass gate, 3.3 V domain only.

ISO19 — Switched GPIO19: U605 A4 (pin 5): bare pass gate, 3.3 V domain only.

ISO20 — Switched GPIO20: U605 A5 (pin 6): bare pass gate, 3.3 V domain only.

ISO21 — Switched GPIO21: U605 A6 (pin 7): bare pass gate, 3.3 V domain only.

ISO22 — Switched GPIO22: U605 A7 (pin 8): bare pass gate, 3.3 V domain only.

ISO23 — Switched GPIO23: U605 A8 (pin 9): bare pass gate, 3.3 V domain only.

ISO24 — Switched GPIO24: U606 A1 (pin 2): bare pass gate, 3.3 V domain only.

ISO25 — Switched GPIO25: U606 A2 (pin 3): bare pass gate, 3.3 V domain only.

ISO26 — Switched GPIO26: U606 A3 (pin 4): bare pass gate, 3.3 V domain only.

ISO27 — Switched GPIO27: U606 A4 (pin 5): bare pass gate, 3.3 V domain only.

ISO28 — Switched GPIO28: U606 A5 (pin 6): bare pass gate, 3.3 V domain only.

ISO29 — Switched GPIO29: U606 A6 (pin 7): bare pass gate, 3.3 V domain only.

BUS_SW_EN_INST — Instrument tap of BUS_SW_EN through R604 (1 k); observe only.

Circuit and PCB layout guidance
Migrated from the saved library sheet: circuit and PCB unchanged
Orb Weaver
File: rp2040/rp2040_with_gpio_isolation_ac7ec63a3245/
File: rp2040_with_gpio_isolation_ac7ec63a3245.kicad_sch

Title: RP2040 core with GPIO isolation

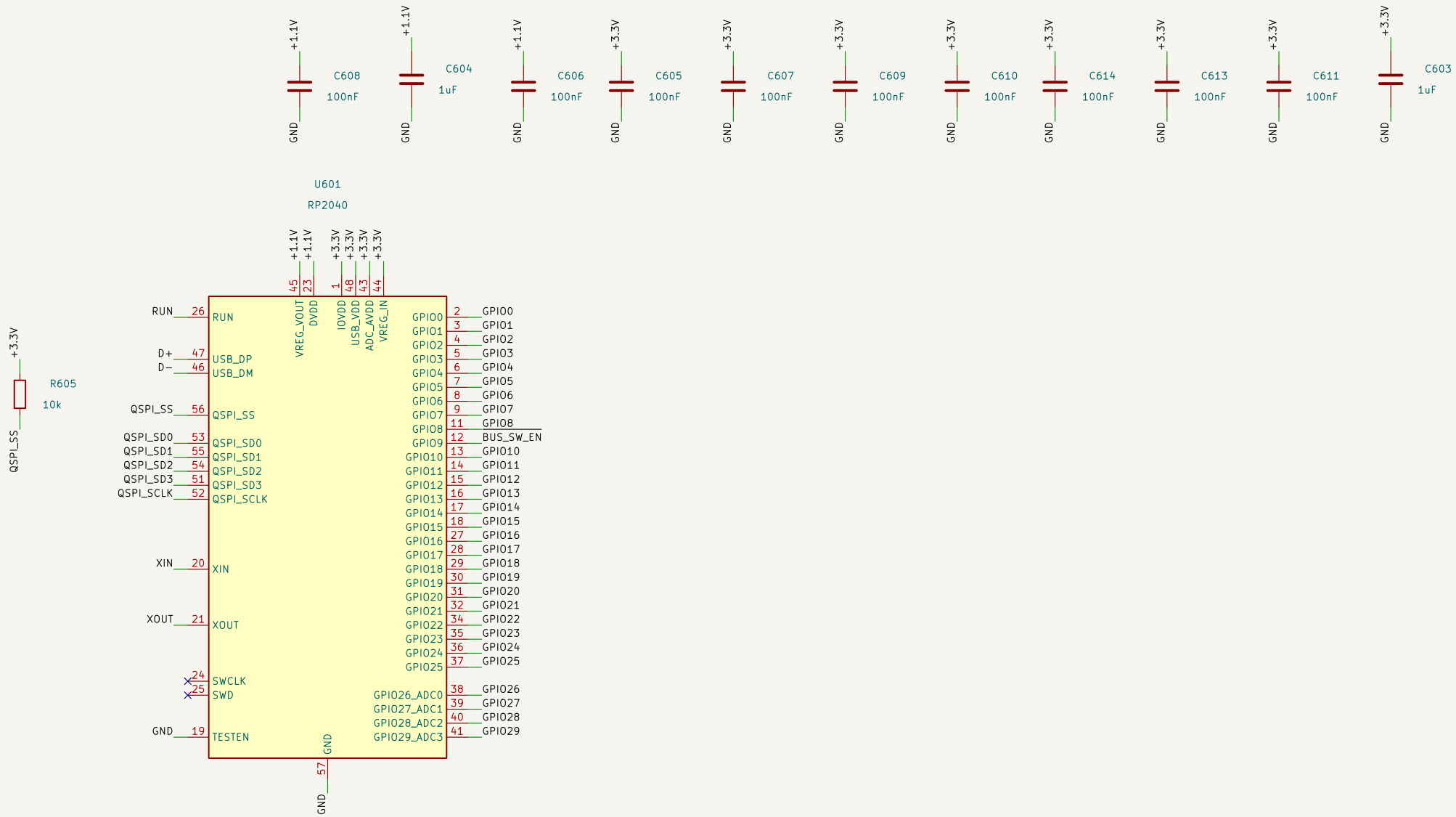
Size: A3	Date: 2026-05-04
Rev: Source migration 1	
KiCad 10.0.0	Id: 6/29

RP2040 controller core and its GPIO isolation in one block: the full rp2040 core — W25Q128JVPIQ QSPI flash, 12 MHz ABM8 crystal, decoupling, BOOTSEL and RUN switches — plus four SN74CB3Q3245RGYR 8-channel bidirectional FET bus switches, wit

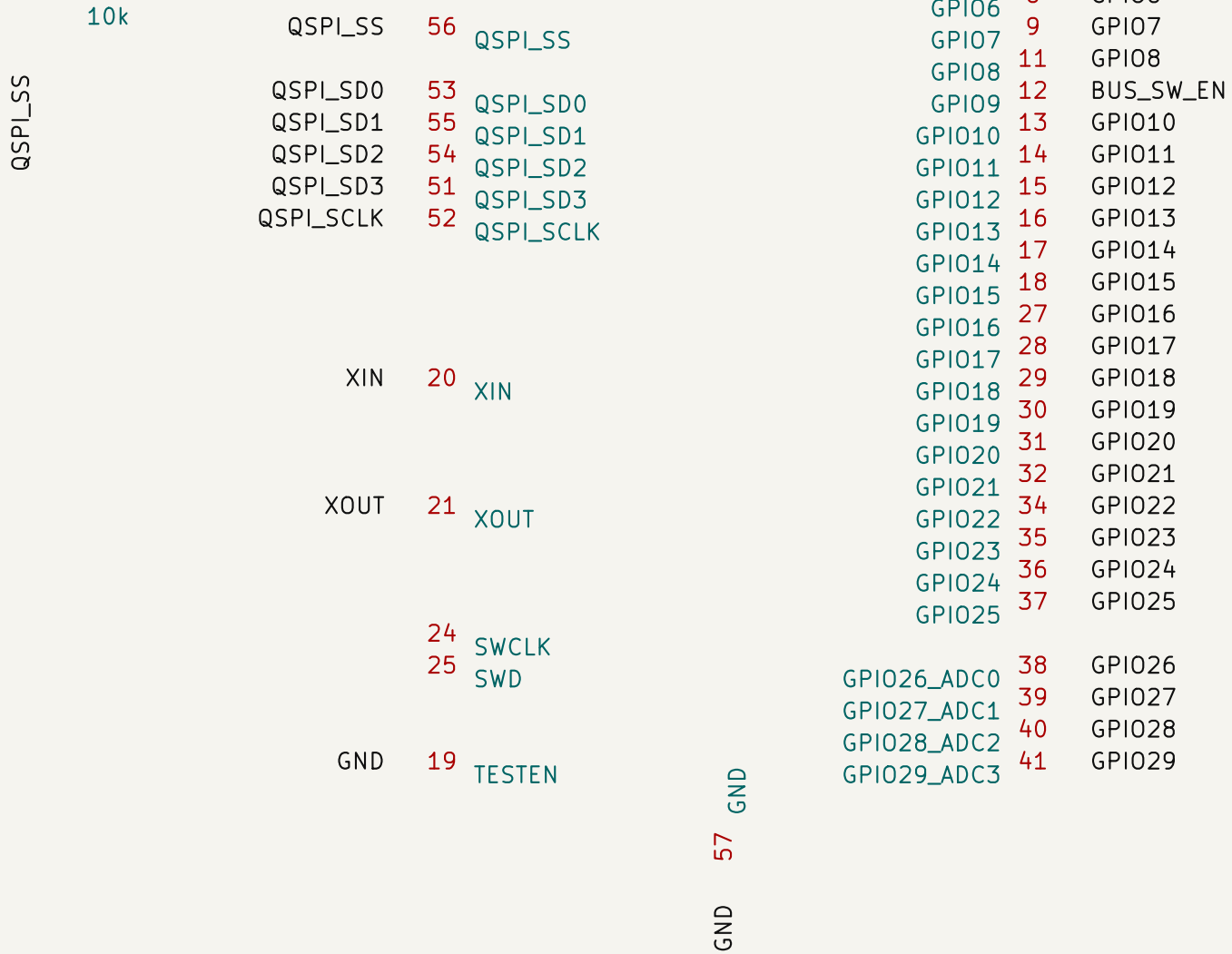
Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Controller core

U601: QSPI to U602, USB through R601/R602, GPIO0–29 to the switches' B side, GPIO9 as the enable. +3.3V: C603 (1 uF) bulk at VREG_IN and seven 100 nF for the nine +3.3V supply pins: C605 at IOVDD 1, C614 at IOVDD 10, C609 at IOVDD 22, C607 at IOVDD 33; C610, C611 and C613 at the corner of IOVDD 42, ADC_AVDD 43, VREG_IN 44, USB_VDD 48 and IOVDD 49, where the routed PCB fixes the pairing. +1.1V: C606 at DVDD 23, C608 at VREG_VOUT 45, C604 (1 uF) beside DVDD 50.



Controller core; GPIO9 is the switch enable
C605: IOVDD pin 1 bypass, 100 nF; C607: IOVDD pin 33 bypass, 100 nF; C609: IOVDD pin 22 bypass, 100 nF; C610: Corner bypass, pins 42–44, 48, 49, 100 nF; C614: IOVDD pin 10 bypass, 100 nF; one per IOVDD pins 1, 10, 22, 33, 42, 49
C604: +1.1V bulk beside DVDD pin 50, 1 uF; C606: DVDD pin 23 bypass, 100 nF; one per DVDD pins 23, 50
C603: +3.3V bulk at VREG_IN pin 44, 1 uF
C611, C613: Corner bypass, pins 42–44, 48, 49, 100 nF
R605: QSPI_SS pull-up, 10 k
C608: VREG_VOUT pin 45 bypass, 100 nF



Controller core; GPIO9 is the switch enable
C605: IOVDD pin 1 bypass, 100 nF; C607: IOVDD pin 33 bypass, 100 nF; C609: IOVDD pin 22 bypass, 100 nF; C610: Corner bypass, pins 42–44, 48, 49, 100
C604: +1.1V bulk beside DVDD pin 50, 1 uF; C606: DVDD pin 23 bypass, 100 nF; one per DVDD pins 23, 50
C603: +3.3V bulk at VREG_IN pin 44, 1 uF
C611, C613: Corner bypass, pins 42–44, 48, 49, 100 nF
R605: QSPI_SS pull–up, 10 k
C608: VREG_VOUT pin 45 bypass, 100 nF

PLACE: Exposed pad to GND copper with vias; GPIO escapes toward the switches.

PLACE: Each capacitor hard against its pin with the shortest return to the GND pad (57); the corner pins 42 to 44, 48 and 49 share C610, C611 and C613.

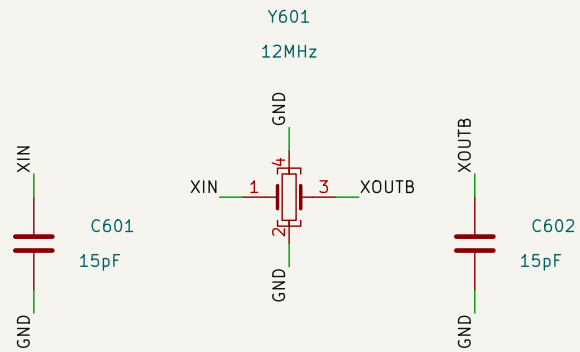
ROUTE: Switched signals leave on the A side; raw GPIO ports are the same B–side traces.

ROUTE: +1.1V stays inside the block; the switches' VCC pins have their own capacitors.

11 12 13 14 15

2. Clock

Y601 (12 MHz) between XIN and XOUTB with 15 pF loads; R603 (1 k) in the XOUT leg.



12 MHz crystal
C601, C602: Crystal load capacitors (15 pF, C0G)

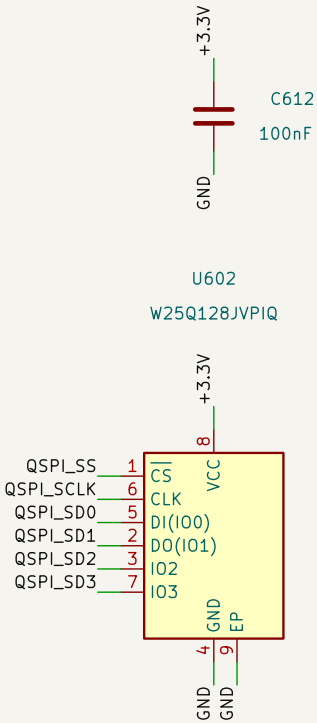
Crystal drive limit, 1 k, XOUT

PLACE: All four at pins 20 and 21 over a local ground; nothing else beside the crystal.

ROUTE: Short traces, no vias, GND fill around; keep switching lines away.

3. QSPI flash

U602 (W25Q128JVPIQ) on QSPI_SCLK, SD0–SD3 and QSPI_SS; C612 decouples pin 8.



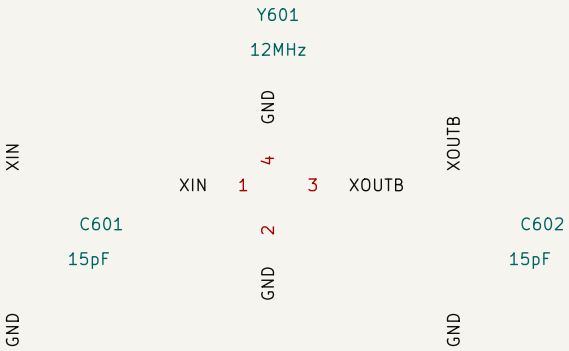
QSPI boot flash, 16 MB
C612: U602 VCC pin 8
bypass, 100 nF

PLACE: Next to pins 51–56, C612 at pin 8, pad 9 to GND.

ROUTE: Six short QSPI lines of similar length; up to 133 MHz.

2. Clock

Y601 (12 MHz) between XIN and XOUTB with 15 pF loads; R603 (1 k) in the XOUT leg.



12 MHz crystal
C601, C602: Crystal load capacitors (15 pF, C0G)

Crystal drive limit, 1 k, XOUT

PLACE: All four at pins 20 and 21 over a local ground; nothing else beside the crystal.

ROUTE: Short traces, no vias, GND fill around; keep switching lines away.

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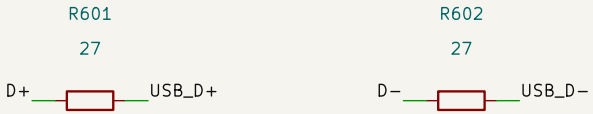
4. USB

R601/R602 (27 ohm) between the pads (D+, D−) and the USB_D+/USB_D− ports.

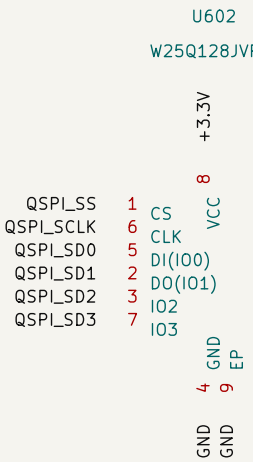


USB_DP series, 27 R

USB_DM series, 27 R

PLACE: At pins 46 and 47; the ports leave outside them.

ROUTE: USB_HS class, routed as a pair, no stubs.



QSPI boot flash, 16 MB
C612: U602 VCC pin 8
bypass, 100 nF

PLACE: Next to pins 51–56, C612 at pin 8, pad 9 to GND.

ROUTE: Six short QSPI lines of similar length; up to 133 MHz.

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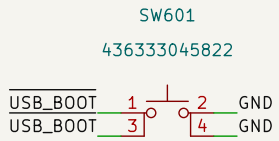
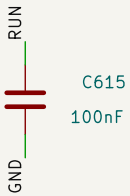
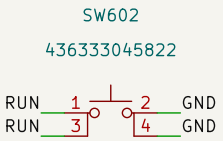
5. BOOTSEL and RUN

R605 pulls QSPI_SS up; SW601 grounds $\overline{\text{USB_BOOT}}$ via R606; SW602 grounds RUN, C615 filters it.



BOOTSEL switch, grounds
$\overline{\text{USB_BOOT}}$





RUN switch, grounds RUN pin 26
C615: RUN pin 26 filter, 100 nF

BOOTSEL series, 1 k, QSPI_SS to
$\overline{\text{USB_BOOT}}$

PLACE: SW602 beside SW601 on one edge (hold BOOTSEL, tap RUN); C615 hard against pin 26.

ROUTE: RUN is DC with an internal pull-up: length is free, noise is not.

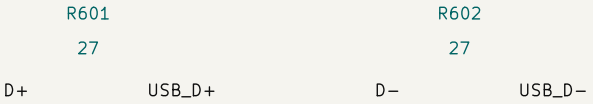
Crystal drive limit, 1 k, XOUT

PLACE: All four at pins 20 and 21 over a local ground; nothing else beside the crystal.

ROUTE: Short traces, no vias, GND fill around; keep switching lines away.

4. USB

R601/R602 (27 ohm) between the pads (D+, D−) and the USB_D+/USB_D− ports.



USB_DP series, 27 R

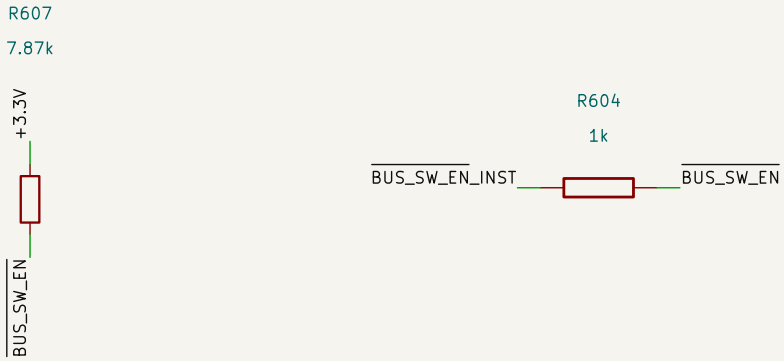
USB_DM series, 27 R

PLACE: At pins 46 and 47; the ports leave outside them.

ROUTE: USB_HS class, routed as a pair, no stubs.

6. Bus switch enable

R607 (7.87 k) holds $\overline{\text{BUS_SW_EN}}$ high at reset; R604 (1 k) makes $\overline{\text{BUS_SW_EN_INST}}$.



$\overline{\text{BUS_SW_EN}}$ pull−up: bus isolated at reset

$\overline{\text{BUS_SW_EN}}$ instrument tap, 1 k

PLACE: R607 near pin 12; R604 toward the instrument escape.

ROUTE: One net to all four pin 19 inputs.

Controller core; GPIO9 is the switch enable
C605: IOVDD pin 1 bypass, 100 nF; C607: IOVDD pin 33 bypass, 100 nF; C609: IOVDD pin 22 bypass, 100 nF; C610: Corner bypass, pins 42–44, 48, 49, 100 nF; C614: IOVDD pin 10 bypass, 100 nF; one per IOVDD pins 1, 10, 22, 33, 42, 49
C604: +1.1V bulk beside DVDD pin 50, 1 uF; C606: DVDD pin 23 bypass, 100 nF; one per DVDD pins 23, 50
C603: +3.3V bulk at VREG_IN pin 44, 1 uF
C611, C613: Corner bypass, pins 42–44, 48, 49, 100 nF
R605: QSPI_SS pull–up, 10 k
C608: VREG_VOUT pin 45 bypass, 100 nF

PLACE: Exposed pad to GND copper with vias; GPIO escapes toward the switches.

PLACE: Each capacitor hard against its pin with the shortest return to the GND pad (57); the corner pins 42 to 44, 48 and 49 share C610, C611 and C613.

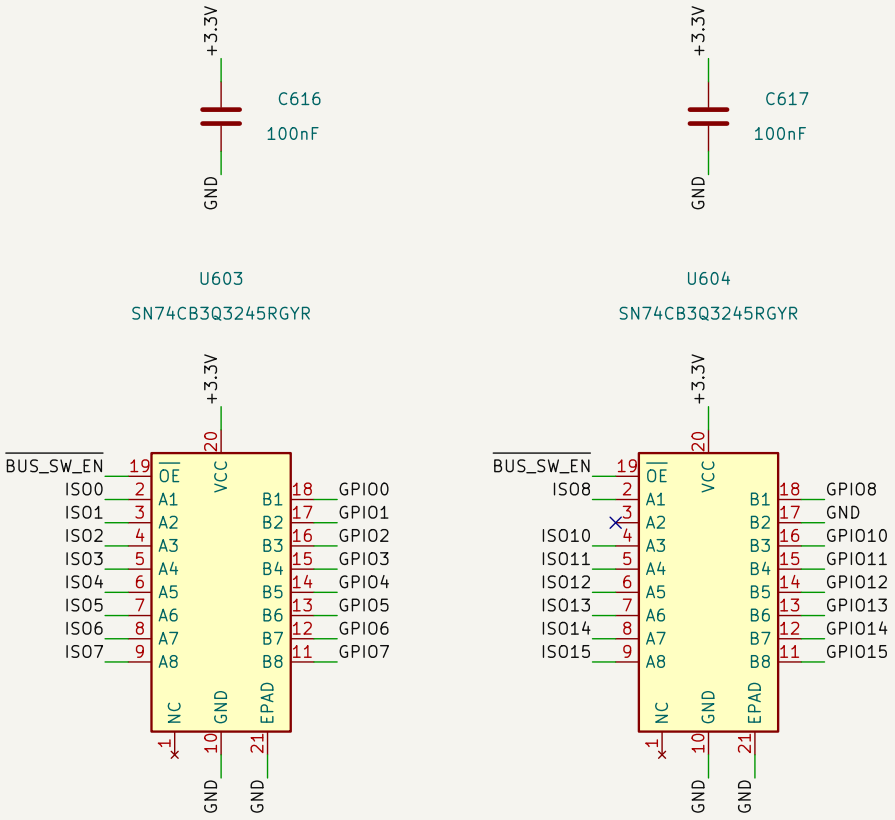
ROUTE: Switched signals leave on the A side; raw GPIO ports are the same B–side traces.

ROUTE: +1.1V stays inside the block; the switches' VCC pins have their own capacitors.

---

7. Bus switches U603 and U604

U603 and U604 pass GPIO0–7 and GPIO8, GPIO10–15 to the ISO ports (B side MCU, A side switched); C616 (U603) and C617 (U604) decouple pin 20. U604 channel 2 spare (B2 pin 17 to GND, A2 pin 3 open).



FET bus switch, GPIO0–7 to ISO0–7
C616: U603 VCC pin 20 bypass, 100 nF

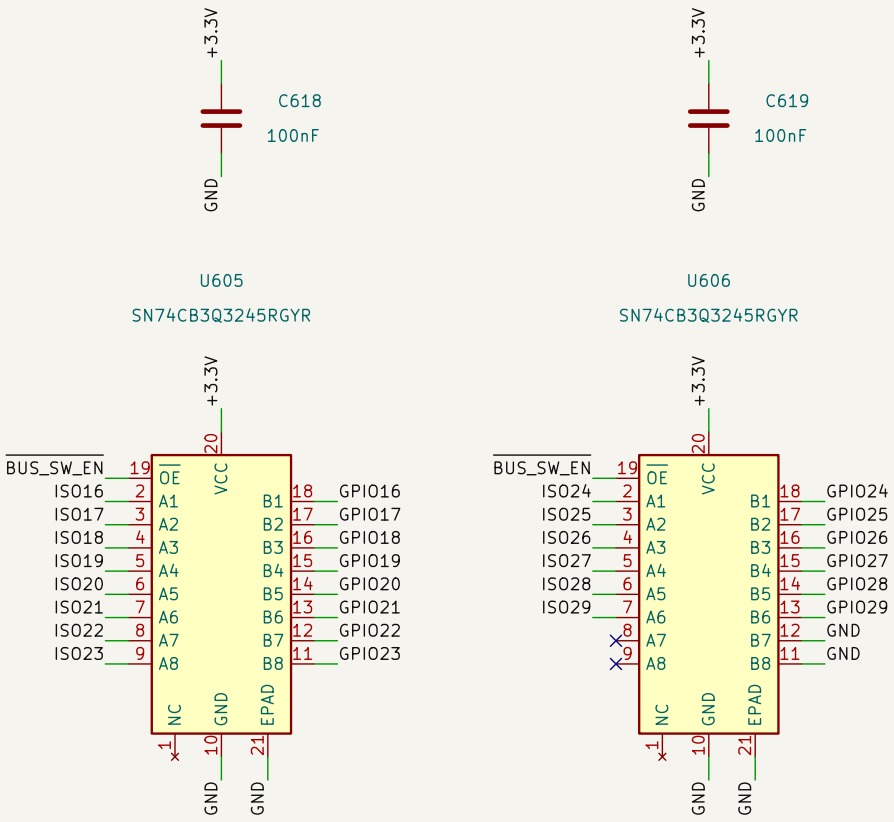
FET bus switch, GPIO8,10–15 to ISO8,10–15
C617: U604 VCC pin 20 bypass, 100 nF

PLACE: C616 and C617 at pin 20 with short returns to pin 10 and the EPAD.

ROUTE: B side to the MCU, A side to the ISO port vias; EPADs to GND.

8. Bus switches U605 and U606

U605 and U606 pass GPIO16–23 and GPIO24–29 to the ISO ports (B side MCU, A side switched); C618 (U605) and C619 (U606) decouple pin 20. U606 channels 7 and 8 spare (B7/B8 pins 12/11 to GND, A7/A8 pins 8/9 open).



FET bus switch, GPIO16–23 to ISO16–23
C618: U605 VCC pin 20 bypass, 100 nF

FET bus switch, GPIO24–29 to ISO24–29
C619: U606 VCC pin 20 bypass, 100 nF

PLACE: C618 and C619 at pin 20 with short returns to pin 10 and the EPAD.

ROUTE: B side to the MCU, A side to the ISO port vias; EPADs to GND.

INTERFACES

+3.3V +3.3V

Always-on 3.3 V for the MCU, flash, four switches and pull-ups.

GND GND

Common return: core, flash, switches (GND, EPAD), crystal, switch frames.

GPIO0 GPIO0

Raw MCU GPIO0, 3.3 V; one node with ISO0 via U603 B1 (pin 18) when enabled.

GPIO1 GPIO1

Raw MCU GPIO1, 3.3 V; one node with ISO1 via U603 B2 (pin 17) when enabled.

GPIO2 GPIO2

Raw MCU GPIO2, 3.3 V; one node with ISO2 via U603 B3 (pin 16) when enabled.

GPIO3 GPIO3

Raw MCU GPIO3, 3.3 V; one node with ISO3 via U603 B4 (pin 15) when enabled.

GPIO4 GPIO4

Raw MCU GPIO4, 3.3 V; one node with ISO4 via U603 B5 (pin 14) when enabled.

GPIO5 GPIO5

Raw MCU GPIO5, 3.3 V; one node with ISO5 via U603 B6 (pin 13) when enabled.

GPIO6 GPIO6

Raw MCU GPIO6, 3.3 V; one node with ISO6 via U603 B7 (pin 12) when enabled.

GPIO7 GPIO7

Raw MCU GPIO7, 3.3 V; one node with ISO7 via U603 B8 (pin 11) when enabled.

GPIO8 GPIO8

Raw MCU GPIO8, 3.3 V; one node with ISO8 via U604 B1 (pin 18) when enabled.

GPIO10 GPIO10

Raw MCU GPIO10, 3.3 V; one node with ISO10 via U604 B3 (pin 16) when enabled.

GPIO11 GPIO11

Raw MCU GPIO11, 3.3 V; one node with ISO11 via U604 B4 (pin 15) when enabled.

GPIO12 GPIO12

Raw MCU GPIO12, 3.3 V; one node with ISO12 via U604 B5 (pin 14) when enabled.

GPIO13 GPIO13

Raw MCU GPIO13, 3.3 V; one node with ISO13 via U604 B6 (pin 13) when enabled.

GPIO14 GPIO14

Raw MCU GPIO14, 3.3 V; one node with ISO14 via U604 B7 (pin 12) when enabled.

GPIO15 GPIO15

Raw MCU GPIO15, 3.3 V; one node with ISO15 via U604 B8 (pin 11) when enabled.

GPIO16 GPIO16

Raw MCU GPIO16, 3.3 V; one node with ISO16 via U605 B1 (pin 18) when enabled.

GPIO17 GPIO17

Raw MCU GPIO17, 3.3 V; one node with ISO17 via U605 B2 (pin 17) when enabled.

GPIO18 GPIO18

Raw MCU GPIO18, 3.3 V; one node with ISO18 via U605 B3 (pin 16) when enabled.

GPIO19 GPIO19

Raw MCU GPIO19, 3.3 V; one node with ISO19 via U605 B4 (pin 15) when enabled.

GPIO20 ◇— GPIO20

Raw MCU GPIO20, 3.3 V; one node with ISO20 via U605 B5 (pin 14) when enabled.

GPIO21 ◇— GPIO21

Raw MCU GPIO21, 3.3 V; one node with ISO21 via U605 B6 (pin 13) when enabled.

GPIO22 ◇— GPIO22

Raw MCU GPIO22, 3.3 V; one node with ISO22 via U605 B7 (pin 12) when enabled.

GPIO23 ◇— GPIO23

Raw MCU GPIO23, 3.3 V; one node with ISO23 via U605 B8 (pin 11) when enabled.

GPIO24 ◇— GPIO24

Raw MCU GPIO24, 3.3 V; one node with ISO24 via U606 B1 (pin 18) when enabled.

GPIO25 ◇— GPIO25

Raw MCU GPIO25, 3.3 V; one node with ISO25 via U606 B2 (pin 17) when enabled.

GPIO26 □— GPIO26

Raw MCU GPIO26/ADC0, 3.3 V; one node with ISO26 via U606 B3 (pin 16) when enabled.

GPIO27 □— GPIO27

Raw MCU GPIO27/ADC1, 3.3 V; one node with ISO27 via U606 B4 (pin 15) when enabled.

GPIO28 □— GPIO28

Raw MCU GPIO28/ADC2, 3.3 V; one node with ISO28 via U606 B5 (pin 14) when enabled.

GPIO29 □— GPIO29

Raw MCU GPIO29/ADC3, 3.3 V; one node with ISO29 via U606 B6 (pin 13) when enabled.

USB_D+ ◇— USB_D+

USB D+ outside R601 (27 ohm), USB_HS class.

USB_D− ◇— USB_D−

USB D− outside R602 (27 ohm), USB_HS class.

$\overline{\text{BUS_SW_EN}}$ ◇— $\overline{\text{BUS_SW_EN}}$

GPIO9 drives all four $\overline{\text{OE}}$; R607 holds it high (isolated) at reset. Never drive it.

ISO0 □— ISO0

Switched GPIO0: U603 A1 (pin 2); bare pass gate, 3.3 V domain only.

ISO1 □— ISO1

Switched GPIO1: U603 A2 (pin 3); bare pass gate, 3.3 V domain only.

ISO2 □— ISO2

Switched GPIO2: U603 A3 (pin 4); bare pass gate, 3.3 V domain only.

ISO3 □— ISO3

Switched GPIO3: U603 A4 (pin 5); bare pass gate, 3.3 V domain only.

ISO4 □— ISO4

Switched GPIO4: U603 A5 (pin 6); bare pass gate, 3.3 V domain only.

ISO5 □— ISO5

Switched GPIO5: U603 A6 (pin 7); bare pass gate, 3.3 V domain only.

ISO6 □— ISO6

Switched GPIO6: U603 A7 (pin 8); bare pass gate, 3.3 V domain only.

ISO7 ISO7

Switched GPIO7: U603 A8 (pin 9); bare pass gate, 3.3 V domain only.

ISO8 ISO8

Switched GPIO8: U604 A1 (pin 2); bare pass gate, 3.3 V domain only.

ISO10 ISO10

Switched GPIO10: U604 A3 (pin 4); bare pass gate, 3.3 V domain only.

ISO11 ISO11

Switched GPIO11: U604 A4 (pin 5); bare pass gate, 3.3 V domain only.

ISO12 ISO12

Switched GPIO12: U604 A5 (pin 6); bare pass gate, 3.3 V domain only.

ISO13 ISO13

Switched GPIO13: U604 A6 (pin 7); bare pass gate, 3.3 V domain only.

ISO14 ISO14

Switched GPIO14: U604 A7 (pin 8); bare pass gate, 3.3 V domain only.

ISO15 ISO15

Switched GPIO15: U604 A8 (pin 9); bare pass gate, 3.3 V domain only.

ISO16 ISO16

Switched GPIO16: U605 A1 (pin 2); bare pass gate, 3.3 V domain only.

ISO17 ISO17

Switched GPIO17: U605 A2 (pin 3); bare pass gate, 3.3 V domain only.

ISO18 ISO18

Switched GPIO18: U605 A3 (pin 4); bare pass gate, 3.3 V domain only.

ISO19 ISO19

Switched GPIO19: U605 A4 (pin 5); bare pass gate, 3.3 V domain only.

ISO20 ISO20

Switched GPIO20: U605 A5 (pin 6); bare pass gate, 3.3 V domain only.

ISO21 ISO21

Switched GPIO21: U605 A6 (pin 7); bare pass gate, 3.3 V domain only.

ISO22 ISO22

Switched GPIO22: U605 A7 (pin 8); bare pass gate, 3.3 V domain only.

ISO23 ISO23

Switched GPIO23: U605 A8 (pin 9); bare pass gate, 3.3 V domain only.

ISO24 ISO24

Switched GPIO24: U606 A1 (pin 2); bare pass gate, 3.3 V domain only.

ISO25 ISO25

Switched GPIO25: U606 A2 (pin 3); bare pass gate, 3.3 V domain only.

ISO26 ISO26

Switched GPIO26: U606 A3 (pin 4); bare pass gate, 3.3 V domain only.

ISO27 ISO27

Switched GPIO27: U606 A4 (pin 5); bare pass gate, 3.3 V domain only.

ISO28 ISO28

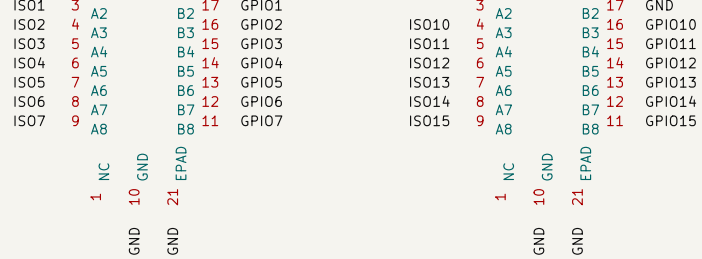
Switched GPIO28: U606 A5 (pin 6); bare pass gate, 3.3 V domain only.

ISO29 ISO29

Switched GPIO29: U606 A6 (pin 7); bare pass gate, 3.3 V domain only.

$\overline{\text{BUS_SW_EN_INST}}$ $\overline{\text{BUS_SW_EN_INST}}$

Instrument tap of $\overline{\text{BUS_SW_EN}}$ through R604 (1 k); observe only.

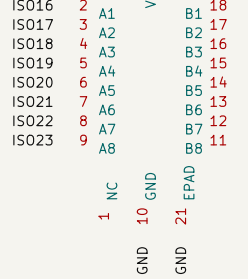


FET bus switch, GPIO0–7 to ISO0–7
C616: U603 VCC pin 20 bypass, 100 nF

FET bus switch, GPIO8,10–15 to ISO8,10–15
C617: U604 VCC pin 20 bypass, 100 nF

PLACE: C616 and C617 at pin 20 with short returns to pin 10 and the EPAD.

ROUTE: B side to the MCU, A side to the ISO port vias; EPADs to GND.



FET bus switch, GPIO16–23 to ISO16–2
C618: U605 VCC pin 20 bypass, 100 nF

PLACE: C618 and C619 at pin 20 with short

ROUTE: B side to the MCU, A side to the ISO

OPERATION

64 ports: GPIO0–8 and GPIO10–29 are the raw pads, ISO0–8 and ISO10–29 the same pads behind one switch channel each; BUS_SW_EN and its tap BUS_SW_EN_INST leave for observation only. GPIO9 (pin 12) is the enable and has no GPIO or ISO port. Per index, GPIOn and ISOn are one node when enabled: wire one or the other, by the far end's power domain.

The ISO side is a bare pass gate: no level shift, buffer or protection. Switch I/O is rated to 5.5 V but the MCU pad behind it is limited to IOVDD + 0.3 V; pulls on the switched side reference the switched rail, never +3.3V. Unused ports get no-connect flags on the placing sheet.

Enable: GPIO9 drives BUS_SW_EN (active low) to the four OE pins; R607 (7.87 k) keeps the bus isolated from power-on; R604 (1 k) makes the instrument tap. t_en 14 ns, t_dis 13 ns max at 3.3 V. Firmware: isolate, drop the rail; raise, confirm, connect.

Supply: always-on +3.3V for IOVDD, USB_VDD, ADC_AVDD, VREG_IN, the flash and the switches' VCC (2.3–3.6 V); the regulator makes +1.1V for DVDD. Each switch draws 1 mA typ, 2 mA max on or off (about 4 mA typ, 8 mA max total). Isolation rests on the enable, not on Ioff.

Core: Y601 12 MHz with C601/C602 (15 pF) and R603 (1 k); W25Q128 on QSPI; BOOTSEL grounds USB_BOOT (R606 1 k to QSPI_SS, R605 10 k up); RUN grounds pin 26 (C615, internal pull-up only), does not reset the flash, releases GPIO to high-Z. SWD is not exposed. Two instances need separate sheets.

DESIGN CONTRACT

RP2040 controller core and its GPIO isolation in one block: the full rp2040 core (W25Q128JVPIQ QSPI flash, 12 MHz ABM8 crystal, decoupling, BOOTSEL and RUN switches) plus four SN74CB3Q3245RGYR 8-channel bidirectional FET bus switches, with all 29 MCU-to-switch connections made inside the block so that routing is placed once instead of re-drawn per board. Derived from rp2040, which remains canonical for an MCU with no isolation and is the upstream for the core half: fix core circuitry there first, then refresh here. The switch half has no upstream; fix it here. This block replaces the retired isolation-only companion rp2040_gpio_isolation_sn74cb3q3245 outright and is the only isolated form. Core parts are positionally identical to rp2040. DO NOT place this block alongside rp2040: it already contains that core. Designators are the 40xxx band.
Decoupling: C603 (1 uF) is the +3.3V bulk at VREG_IN and seven 100 nF serve the nine +3.3V supply pins: C605 at IOVDD 1, C614 at IOVDD 10, C609 at IOVDD 22, C607 at IOVDD 33, and C610, C611 and C613 at the corner of IOVDD 42, ADC_AVDD 43, VREG_IN 44, USB_VDD 48 and IOVDD 49, where the routed PCB fixes the pairing. C612 bypasses the flash VCC (U602 pin 8); C616 to C619 bypass VCC pin 20 of U603 to U606 in turn. The regulator's +1.1V has C606 at DVDD 23, C608 at VREG_VOUT 45 and C604 (1 uF) beside DVDD 50.

1. THE INTERFACE IS 64 PORTS AND GPIO9 IS NOT ONE OF THEM: 29 raw MCU ports GPIO0–GPIO8 and GPIO10–GPIO29, 29 switched ports ISO0–ISO8 and ISO10–ISO29, USB_D+, USB_D-, +3.3V, GND, and the enable BUS_SW_EN with its instrument tap BUS_SW_EN_INST, both for observation only. GPIO9 is spent on the bus-switch enable and has no GPIO or ISO port; there is no ISO9 and no separate OE port. Any board placing this block gives up GPIO9 and inherits BUS_SW_EN as a firmware constant. tmc51x0-driver-dev-pcb puts the same signal on GPIO19 and does NOT use this block; do not align them.
2. GPIOn AND ISOn ARE THE SAME NODE WHENEVER THE BUS IS ENABLED. Per index they are an either/or, not a fan-out. Wiring both shorts whatever sits on the always-on side to whatever sits on the switched side the instant firmware pulls BUS_SW_EN low, and neither ERC nor DRC can see it. The board chooses per signal, and the rule is the powered domain of the far end: a GPIO goes through the switch if and only if its far end sits on a switched rail. See mouse-joystick-pcb docs/interface-map.md, The Rule — Follow The Far End's Power Domain.
3. THE ISO SIDE IS A BARE PASS GATE: no level shift, no buffer, no protection, no direction. Switch I/O is rated 0–5.5 V but the other end of every channel is an RP2040 pad limited to IOVDD+0.3 V, so a 5 V pull-up or a 5 V driver on an ISO pin damages the MCU, not the switch. Do not give ISO ports a direction shape: the gate is symmetric and they are passive by construction. Pull-ups and pull-downs on the switched side must reference the SWITCHED rail, never +3.3V, or they back-power the dead domain through the far chip's input clamps inside a block where the bus switch cannot see it.
4. THE ENABLE IS THE MCU'S, ACTIVE LOW, AND DISABLED BY DEFAULT: GPIO9 drives BUS_SW_EN to all four pin 19 inputs, with R607 7.87 k to +3.3V so the bus is isolated at power-on until firmware asserts it. The enable cannot sit behind the switch it enables, and an MCU must be able to connect a bus that is currently disconnected, so the board never sources it: BUS_SW_EN leaves the block only to be observed, and BUS_SW_EN_INST through R604 (1 k) is its instrument tap. NEVER drive it from the board; a second driver fights the MCU and the pull-up is the only thing defining the reset state. Sequencing is board policy and firmware must follow it: isolate first, then drop the rail; raise the rail, confirm it, then connect last. t_en is 14 ns max and t_dis 13 ns max at 3.3 V, so the disconnect is deterministic and instantaneous relative to any rail.
5. SUPPLY IS THE ALWAYS-ON 3.3 V RAIL, DELIBERATELY, AND THERE IS NO Ioff SECOND LINE OF DEFENCE. One +3.3V port feeds the MCU, all four V_CC pins and the pull-up. Powering the switches from the switched domain would give free isolation through Ioff at V_CC=0 and cost no GPIO, and is REJECTED: it hands sequencing to a rail ramp, removes the ability to isolate before powering down, and leaves the always-on MCU driving an enable input on an unpowered part; Ioff is specified for the data terminals (V_CC=0, 0 to 5.5 V, 1 uA max) with no control-input condition stated, and V_IH is characterized only over V_CC 2.3–3.6 V. Isolation therefore rests entirely on the MCU holding BUS_SW_EN high, which R607 makes the reset default. This contradicts the catalog note on OW-MISC-SN74CB3Q3245RGYR, which recommends switched-domain power; the block and the boards win, see kicad-libs docs/rp2040-gpio-isolation-design-block-plan.md.
6. IT COSTS 4 mA JUST BY EXISTING: I_CC is 1 mA typ and 2 mA max per package with the switch ON OR OFF, because the charge pump runs regardless, so four packages draw about 4 mA typ and 8 mA max continuously from the always-on rail even with every channel isolated. That is the price of 1:1 coverage and it is accepted.
7. ONE CHANNEL PER GPIO, AND THREE SPARES. Pairing on the RGY-20 package is A_n = pin (n+1) and B_n = pin (19-n); A IS THE SWITCHED SIDE AND B IS THE MCU SIDE. U603 carries GPIO0–GPIO7 to ISO0–ISO7, U604 GPIO8 and GPIO10–GPIO15 to ISO8 and ISO10–ISO15, U605 GPIO16–GPIO23 to ISO16–ISO23, U606 GPIO24–GPIO29 to ISO24–ISO29. The three unused channels are U604 channel 2, freed by the enable, and U606 channels 7 and 8. Treatment for every spare is the same and is not arbitrary: MCU-side B pin to GND, A pin left open, so no node floats on the always-on rail and no switched-side pin is a hidden hard ground.
8. THE BOARD OWES NO-CONNECTS AND ITS OWN BIAS. Most ISO and raw ports are unused on any given board; flag them no-connect rather than leaving them dangling. Unused channels need nothing else: the pass gate has no internal buffer, so an open data pin is not a floating CMOS input. Bus terminations, input bias and instrument taps are board-level or belong to the far-end block, never here. USB_D+ and USB_D- leave OUTSIDE the 27 ohm series resistors R601 and R602; do not add more series resistance at the board.
9. CORE GOTCHAS CARRIED FROM rp2040 (full text in that block's description): SWD IS NOT EXPOSED, pins 24 and 25 are deliberately open and no debug-connector footprint exists in the libraries, so this block offers no debug header. Place SW602 (RUN) physically adjacent to SW601 (BOOTSEL) on the same board edge or the one-handed hold-BOOTSEL-tap-RUN recovery gesture becomes a two-handed operation on an installed rig. C615 is the exception to that adjacency: it decouples RUN and belongs hard against pin 26 with a short return. RUN has no external pull-up and needs none (the internal 50–80 k is the only one) and needs neither the 1 k series nor the 10 k pull-up that belong to BOOTSEL's QSPI_SS. A RUN reset does NOT reset U602, so a warm reset that hangs where a power cycle works is the flash. RUN also releases every GPIO to high-Z, so the placing board must ensure each domain it controls defaults to safe on MCU reset.
10. TWO INSTANCES NEED SEPARATE SHEETS or the internal nets (RUN, USB_BOOT, QSPI_SS, XIN, XOUT, XOUTB, +1.1V, D+ and D-) silently merge between copies.

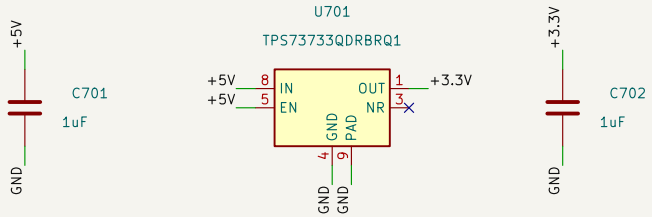
5 V to 3.3 V regulator | TPS73733 fixed 3.3 V LDO

Clean 3.3 V linear regulator from a 5 V input rail using the TI TPS73733 fixed 3.3 V 1 A LDO.

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Regulator and bypass

U701 regulates +5V to +3.3V with EN tied to IN. C701 bypasses IN to GND, C702 holds OUT to GND; NR is open.



Input bypass

Fixed 3.3 V LDO

Output capacitor

PLACE: Place C701 at pins 8 and 4 and C702 at pins 1 and 4 with short local ground returns; tie the thermal pad to GND copper.

ROUTE: +5V and +3.3V carry the rail classes (PWR_5V_LOCAL, PWR_3V3_LOCAL); the GND return of the pad is the regulator's heat path as well.

INTERFACES

+5V — +5V

Input rail; also drives EN, so the regulator is on whenever it is present.

GND — GND

Common return; regulator ground pin and thermal pad.

+3.3V — +3.3V

Regulated output, 3.3 V fixed.

OPERATION

Signal path: +5V -> U701 (IN, pin 8) -> +3.3V (OUT, pin 1). EN (pin 5) is tied to IN, so the regulator is on whenever +5V is present; there is no enable control inside this block.

NR (pin 3) is left open: no noise-reduction capacitor is fitted. GND (pin 4) and the thermal pad (pin 9) return to GND.

C701 (1 uF) bypasses the input, C702 (1 uF) is the output capacitor; both are the catalog 0402 1 uF part. The rail is rated by the TPS73733 (fixed 3.3 V, 1 A class per the catalog description); derate for the board's actual load and dropout.

DESIGN CONTRACT

Clean 3.3 V linear regulator from a 5 V input rail using the TI TPS73733 fixed 3.3 V 1 A LDO. Intended for MCU, RP2040, TMC logic, encoder interface, and other low-voltage digital circuitry.

Circuit and PCB layout guidance

Migrated from the saved library sheet; circuit and PCB unchanged

Orb Weaver

Sheet: /mcu/5v_to_3v3_tps73733_1/

File: 5v_to_3v3_tps73733_1.kicad_sch

Title: 5 V to 3.3 V regulator

Size: A4	Date: 2026-10-04	**Rev: Source migration 1**
KiCad E.D.A. 10.0.6		Id: 7/20

5 V to 3.3 V regulator | TPS73733 fixed 3.3 V LDO

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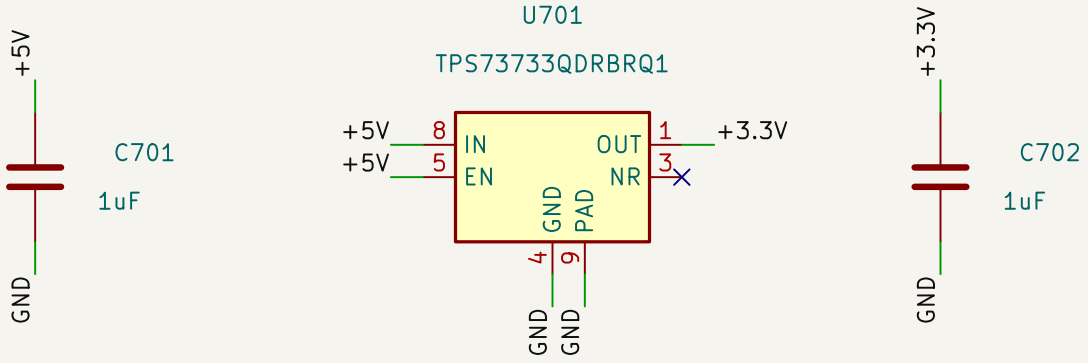

Input bypass

Fixed 3.3 V LDO

Output capacitor

PLACE: Place C701 at pins 8 and 4 and C702 at pins 1 and 4 with short local ground returns; tie the thermal pad to GND copper.

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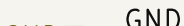
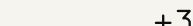
INTERFACES

Input rail; also drives EN, so the regulator is on whenever it is present.



Common return; regulator ground pin and thermal pad.



Regulated output, 3.3 V fixed.

OPERATION

Signal path: +5V –> U701 (IN, pin 8) –> +3.3V (OUT, pin 1). EN (pin 5) is tied to IN, so the regulator is on whenever +5V is present; there is no enable control inside this block.

NR (pin 3) is left open: no noise–reduction capacitor is fitted. GND (pin 4) and the thermal pad (pin 9) return to GND.

C701 (1 uF) bypasses the input, C702 (1 uF) is the output capacitor; both are the catalog 0402 1 uF part. The rail is rated by the TPS73733 (fixed 3.3 V, 1 A class per the catalog description); derate for the board's actual load and dropout.

DESIGN CONTRACT

Clean 3.3 V linear regulator from a 5 V input rail using the TI TPS73733 fixed 3.3 V 1 A LDO. Intended for MCU, RP2040, TMC logic, encoder interface, and other low–voltage digital circuitry.

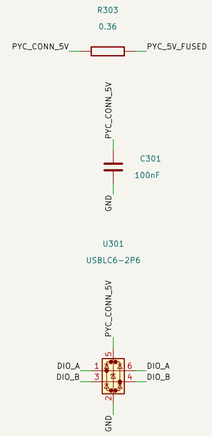
pyControl behavior port, vertical shielded jack | 8P8C, 100 ohm series, USBLC6 clamp, 5 V diode-OR, instrument taps

pyControl behavior-port boundary on a VERTICAL, top-entry SHIELDED 8P8C RJ-45 jack: Molex 855085001, OW-CONN-RJ45-8P8C-THT-VERT, Cat5e, 16.5 mm tall, 1.5 A per contact, through-hole signal contacts plus two through-hole shell legs and two locator pegs.

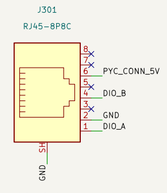
Matching net labels are connected. Group order explains function: PCB placement priorities are stated below.

1. Shielded jack and ESD clamp

J301 brings DIO-A (pin 1), GND (pin 2), DIO-B (pin 4) and port 5 V (pin 6) onto the board; U301 clamps DIO_A and DIO_B to GND and to PYC_CONN_5V at the connector. The shell pads SH return to GND.



ESD clamp on DIO-A, DIO-B and 5 V
C301: Port 5 V bypass at the clamp
R303: Polyfuse position (0.36 ohm jumper)



modular-jack

PLACE: Place U301 hard against J301 pins 1 and 4 with a ground via at its pin 2; route DIO_A and DIO_B in one I/O pad and out the other so the clamp connection stays short.

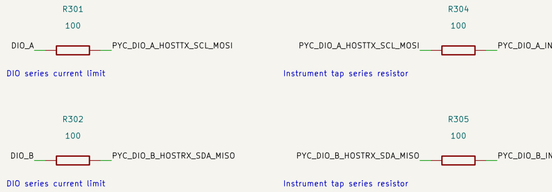
PLACE: Verify J301 pin 1 against the latch and keyway, not the footprint's local pad order: the vertical footprint numbers pads in the opposite direction to the horizontal one.

PLACE: Place the two SH shell-leg holes and the two 3.25 mm locator holes before pouring GND or routing the port; the part does not seat without them.

ROUTE: DIO_A and DIO_B are short connector-side nets; GND from J301 pin 2 is the clamp's return and must reach U301 pin 2 directly.

2. DIO series resistors and instrument taps

R301 and R302 (100 ohm) stand between the clamped connector-side nets and the board's PYC_DIO_A and PYC_DIO_B ports; R304 and R305 (100 ohm) tap the board side of each line for the instrument port.



DIO series current limit

Instrument tap series resistor

DIO series current limit

Instrument tap series resistor

PLACE: Place R301 and R302 just inboard of U301, so the clamp sits on the connector side; between them and the MCU it would protect nothing.

ROUTE: PYC_DIO_A and PYC_DIO_B are Default-class logic to the MCU sheet, which assigns RX to DIO-A and TX to DIO-B.

ROUTE: PYC_DIO_A_INST and PYC_DIO_B_INST are INSTRUMENT-class taps; they carry no drive.

3. Port 5 V, fuse position and diode-OR

C301 bypasses the raw PYC_CONN_5V node; R303 (fuse position) and D301 (series Schottky) make +5V_PYC, the diode-ORable copy of the port's 5 V.

Diode-OR Schottky

PLACE: Place C301 at J301 pin 6 and U301 pin 5 with a short return; R303 is a 1206 position, keep it accessible for the PPTC swap.

ROUTE: PYC_CONN_5V and +5V_PYC are Default-class rails sized for the port's 1.0 A shared budget; +5V_PYC leaves at the port via to be ORed with +5V_USB.

4. Power drive declarations

These nets have an explicit ERC power source declaration.

Power driven:
PYC_CONN_5V

INTERFACES

PYC_CONN_5V — PYC_CONN_5V

Raw port 5 V, J301 pin 6, before R303; the clamp's upper reference.

+5V_PYC — +5V_PYC

Port 5 V after fuse position R303 and Schottky D301: diode-OR with +5V_USB.

GND — GND

Signal return, J301 pin 2 and shell SH; clamp and bypass return.

PYC_DIO_A_HOSTTX_SCL_MOSI — PYC_DIO_A_HOSTTX_SCL_MOSI

DIO-A (J301 pin 1) after R301: controller TX, this board's RX; SCL or MOSI.

PYC_DIO_B_HOSTRX_SDA_MISO — PYC_DIO_B_HOSTRX_SDA_MISO

DIO-B (J301 pin 4) after R302: controller RX, this board's TX; SDA or MISO.

PYC_DIO_A_INST — PYC_DIO_A_INST

Instrument tap of DIO-A through R304 (100 ohm); observe only.

PYC_DIO_B_INST — PYC_DIO_B_INST

Instrument tap of DIO-B through R305 (100 ohm); observe only.

OPERATION

Pin map of J301: 1 DIO-A, 2 GND, 4 DIO-B, 6 port 5 V; pins 3, 5, 7 and 8 are no-connect. DIO-A carries the controller's TX, SCL or MOSI and is this board's RX; DIO-B is the controller's RX, SDA or MISO and this board's TX (board-interfaces pycontrol-behavior-port.md, the one invariant). Ports are named by connector position so a board cannot mirror them; cross to RX/TX once, at the MCU sheet.

Each DIO line passes a 100 ohm series resistor (R301 on DIO-A, R302 on DIO-B); U301 (USBLC6-2P6) clamps both lines and the 5 V node on the connector side of the resistors, so each line routes in one I/O pad and out the other. The controller has nothing in series (its ports carry only an ESD array), so these resistors are the link's only current limit; 100 ohm into the clamp's 3.5 pF is far below the 8.7 us bit of 115200 8N1. USBLC6-2P6: 6 V minimum VBUS breakdown, 12 V typical clamp at 1 A 8/20 us, IEC 61000-4-2 level 4 (15 kV).

PYC_CONN_5V is the raw pin-6 node, bypassed by C301 (100 nF) and the clamp's upper reference, so pin 6 must be wired for the clamps to reference: +5V_PYC is the same node through R303 and D301 (MBR120VLSFT1G, 20 V 1 A Schottky, 0.34 V max at 1 A, 0.6 mA leakage at 25 C) for diode-ORing with the USB block's +5V_USB. R303 is a polyfuse position: the pyControl port shares one 1.0 A supply with the controller's own regulator and has no per-port fuse, so the stocked 0.36 ohm 1206 is a jumper until a 250 to 500 mA PPTC is in the catalog. R303 and D301 may be DNP on a board that takes no port power.

Not every port has a UART: Breakout 1.2 has one on ports 1, 3 and 4 only, the H7 breakout routes seven but the firmware declares none yet (pycontrol-behavior-port.md). Pin 5 is DIO-C on some ports and a POW-C sink-driver output on others, which is why it stays unconnected. The placing board records the port assignment and uses a UART-capable port; the pin map is cited from the syringe-pump module and H7 breakout schematics, not bench-verified.

R304 and R305 (100 ohm) tap DIO-A and DIO-B for the instrument port (INSTRUMENT class), observe only; these are the block's own signals, so the taps live here (convention 14).

Beyond the two instrument taps, the only schematic difference from the horizontal block: the jack is shielded and both shell legs (pad SH, joined by the shell) are tied to GND here; break that tie and terminate through a pad/cap network if the cable shield must float from signal ground.

DESIGN NOTES

DIO_A (pin 1) is ALWAYS the host's driving line: UART TX, I2C SCL, SPI MOSI.
- DIO_B (pin 4) is the host's input: UART RX, I2C SDA, SPI MISO. No exceptions on any pyControl breakout. So DIO_A = this board's RX.
- Breakout 1.2 UART ports: 1 (UART4), 3 (USART1), 4 (USART3). I2C only on 3, 4.
- H7 breakout UART ports: 1,2,3,4,5,9,10. I2C on 1, 6. SPI on 7, 8.
- Breakout 1.2 analog-in on DIO_A/B works on ports 1 and 6 ONLY (2/3/4/5 are GPIOB6-13, no ADC channel). Port 6 DIO_B is the same net as BNC-2.
- DIO_C (pin 5) is NOT 5V tolerant where it is a DAC (PA4/PA5). DIO_A/DIO_B are FT.

DESIGN CONTRACT

pyControl behavior-port boundary on a VERTICAL, top-entry SHIELDED 8P8C RJ-45 jack: Molex 855085001, OW-CONN-RJ45-8P8C-THT-VERT, Cat5e, 16.5 mm tall, 1.5 A per contact, through-hole signal contacts plus two through-hole shell legs and two locator pegs. NOT Ethernet and no magnetics - the jack is a connector family, nothing more. The same front end as the horizontal pycontrol_behavior_port_rj45_boundary block: pin map 1 DIO-A, 2 GND, 4 DIO-B, 6 5V with pins 3, 5, 7, 8 explicitly no-connect; 100 ohm series resistance and a USBLC6-2P6 channel on both DIO lines, with the clamp on the connector side of the resistors and each line routing in one I/O pad and out the other; 100nF on the raw 5 V node; and the same 5 V branch exposing PYC_CONN_5V, the raw pin-6 node, and +5V_PYC, the same node through R303 and a MBR120VLSFT1G series Schottky, for diode-ORing with other 5 V sources - pair it with usb2_vertical's +5V_USB. WATCH THE DIRECTION: pin 1 DIO-A carries the host's transmit and is the DEVICE'S RX; pin 4 DIO-B is the device's TX. Boundary pins are named by connector position, not by direction, so a board cannot mirror them by accident.
R303 IS A POLYFUSE POSITION, not protection: the pyControl port supplies a shared 1.0 A that also feeds the controller's own logic regulator, with no per-port fuse, so a fault on the board can reset the experiment controller. Populate a 1206 PPTC holding 250-500 mA when one is in the catalog; the 0.36 ohm resistor is only a stocked 1206 jumper, and the position must be populated or the branch is open. The USBLC6's clamp rail taps PYC_CONN_5V upstream of R303 so it stays low-impedance and stays referenced if the fuse trips, which also means pin 6 must be present for the I/O clamps to have an upper reference. On a board that takes no port power, R303 and D301 can both be DNP; Pin 5 is DIO-C on some breakout ports and a POW-C sink driver output on others, so it is deliberately unconnected; do not repurpose it without fixing the port assignment first. The assigned port must be UART-capable.
Two schematic differences from the horizontal block. This jack is shielded: both shell legs are pad SH, joined by the metal shell (duplicate_pad_numbers_are_jumpers), and this block ties SH directly to GND. If the cable shield ever needs isolating from signal ground, break that tie here and terminate through a pad/cap network instead - the same choice usb2 makes for the USB-C shell. And the DIO lines carry instrument taps: R304 and R305 (100 ohm) tap the board side of DIO-A and DIO-B to PYC_DIO_A_INST and PYC_DIO_B_INST, observe only; these are the block's own signals, so the taps live here. Ports PYC_DIO_A, PYC_DIO_B, PYC_CONN_5V, +5V_PYC and GND keep their names from the horizontal block; the two INST taps are added.
The land pattern differs completely from the horizontal block, which is why this is a separate block and not a footprint swap. Signal rows are staggered at y = 0 (pins 1, 3, 5, 7) and y = -2.54 (pins 2, 4, 6, 8), 1.27 mm x pitch, 1.4 mm pads on a 0.89 mm drill, against the horizontal 43860-0001's y = 1.78 / 0 at 1.02 mm pitch on 1.5 mm pads. PAD ORDER REVERSES: pin 1 sits at x = 0 and ascends in +x to pin 8 at x = 8.89, where the horizontal starts pin 1 at x = +3.56 and descends. Two SH pads are 2.11 mm on a 1.6 mm drill at y = 9.4, far outboard of the signal rows, and the two 3.25 mm NPTH locators move from y = 4.32 to y = 6.35. No pad lands where it used to. Unlike the tier 1 terminal blocks and usb2_vertical, this footprint GROWS rather than shrinking: courtyard is x -4.66 to 13.55, y -4.70 to 13.10, roughly 18.2 x 17.8 mm, against the horizontal's x +/-8.00, y -5.84 to 9.65, roughly 16.0 x 15.5 mm, and the body no longer overhangs the board edge, so budget the area before placing.
VERIFY PIN 1 PHYSICALLY against the latch and keyway, not against the footprint's local x order, because the two footprints number pads in opposite directions and a mirrored 8P8C map produces a silently crossed pyControl port: check against .../mouse-joystick-pcb/docs/pycontrol-port-pinout.md. The two locator holes are not optional - the part will not seat without them, they sit inside the connector body where it is tempting to route, and the shell legs punch every layer, so place all four holes before pouring GND or routing the port. Retention is the reason to prefer this part over the SMD OW-CONN-RJ45-8P8C-SMD-VERT fallback: insertion and extraction force goes into the board rather than into solder joints, on a rig that gets handled. The cable now leaves perpendicular to the board, so the enclosure in .../mouse-joysticks-mech needs an aperture above the jack plus clearance for the plug body, its latch, and the wire loop, well beyond the 16.5 mm jack height. Not pad-compatible with OW-CONN-438600001 or OW-CONN-RJ45-8P8C-SMD-VERT, and deliberately shares no equiv_group with either.
Pinout is schematic-derived from the syringe-pump pyControl module and the pyControl H7 breakout, which agree on all eight positions, but it is CITED, NOT BENCH-VERIFIED - confirm continuity and cable polarity on real hardware before trusting a populated board. +5V_PYC leaves D301 pad 1 into a port via, where a placing board picks the rail up.

Circuit and PCB layout guidance
Migrated from the saved library sheet; circuit and PCB unchanged
Orb Weaver

Sheet: /pycontrol_behavior_port_rj45_boundary_vertical/
File: pycontrol_behavior_port_rj45_boundary_vertical.kicad_sch

Title: pyControl behavior port, RJ-45 vertical shielded

Size: A2	Date: 2026-10-04	**Rev: Source migration 1**
KiCad E.D.A. 10.0.6		Id: 3/20

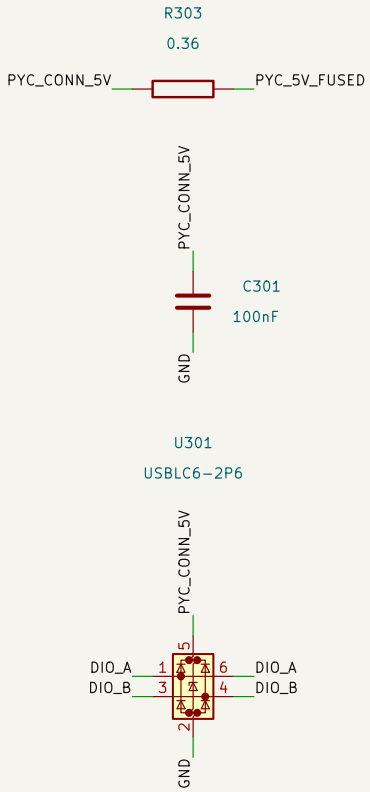
pyControl behavior port, vertical shielded jack | 8P8C, 100 ohm series, USBLC6 clamp, 5 V diode–C

pyControl behavior–port boundary on a VERTICAL, top–entry SHIELDED 8P8C RJ–45 jack: Molex 855085001, OW–CONN–RJ45–8P8C–THT–VERT, Cat5e, 16.5 mm tall, 1.5 A

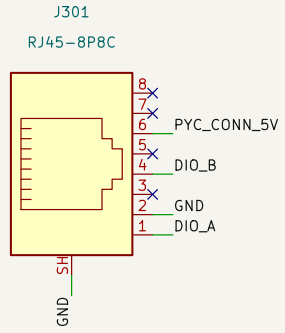
Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Shielded jack and ESD clamp

J301 brings DIO–A (pin 1), GND (pin 2), DIO–B (pin 4) and port 5 V (pin 6) onto the board; U301 clamps DIO_A and DIO_B to GND and to PYC_CONN_5V at the connector. The shell pads SH return to GND.



ESD clamp on DIO–A, DIO–B and 5 V
C301: Port 5 V bypass at the clamp
R303: Polyfuse position (0.36 ohm jumper)



modular–jack

PLACE: Place U301 hard against J301 pins 1 and 4 with a ground via at its pin 2; route DIO_A and DIO_B in one I/O pad and out the other so the clamp connection stays short.

PLACE: Verify J301 pin 1 against the latch and keyway, not the footprint's local pad order: the vertical footprint numbers pads in the opposite direction to the horizontal one.

PLACE: Place the two SH shell–leg holes and the two 3.25 mm locator holes before pouring GND or routing the port; the part does not seat without them.

ROUTE: DIO_A and DIO_B are short connector–side nets; GND from J301 pin 2 is the clamp's return and must reach U301 pin 2 directly.

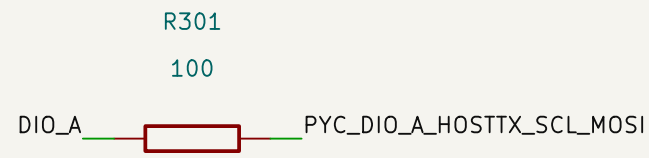
5 6 7 8

instrument taps

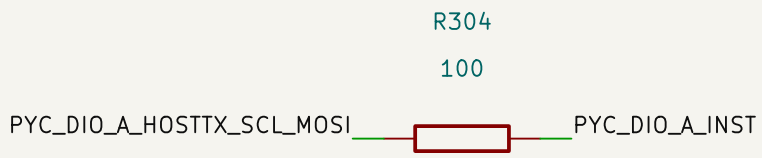
r contact, through-hole signal contacts plus two through-hole shell legs and two locator pegs.

2. DIO series resistors and instrument taps

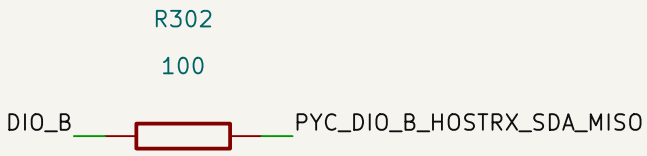
R301 and R302 (100 ohm) stand between the clamped connector-side nets and the board's PYC_DIO_A and PYC_DIO_B ports; R304 and R305 (100 ohm) tap the board side of each line for the instrument port.



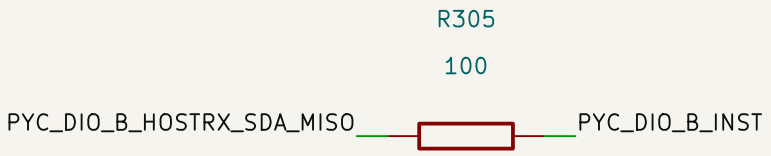
DIO series current limit



Instrument tap series resistor



DIO series current limit



Instrument tap series resistor

PLACE: Place R301 and R302 just inboard of U301, so the clamp sits on the connector side; between them and the MCU it would protect nothing.

ROUTE: PYC_DIO_A and PYC_DIO_B are Default-class logic to the MCU sheet, which assigns RX to DIO-A and TX to DIO-B.

ROUTE: PYC_DIO_A_INST and PYC_DIO_B_INST are INSTRUMENT-class taps; they carry no drive.

board side of each line for the instrument port.

R301
100
DIO_A
PYC_DIO_A_HOSTTX_SCL_MOSI
DIO series current limit

R304
100
PYC_DIO_A_HOSTTX_SCL_MOSI
PYC_DIO_A_INST
Instrument tap series resistor

R302
100
DIO_B
PYC_DIO_B_HOSTRX_SDA_MISO
DIO series current limit

R305
100
PYC_DIO_B_HOSTRX_SDA_MISO
PYC_DIO_B_INST
Instrument tap series resistor

PLACE: Place R301 and R302 just inboard of U301, so the clamp sits on the connector side; between them and the MCU it would protect nothing.

ROUTE: PYC_DIO_A and PYC_DIO_B are Default-class logic to the MCU sheet, which assigns RX to DIO-A and TX to DIO-B.

ROUTE: PYC_DIO_A_INST and PYC_DIO_B_INST are INSTRUMENT-class taps; they carry no drive.

---

3. Port 5 V, fuse position and diode-OR

C301 bypasses the raw PYC_CONN_5V node; R303 (fuse position) and D301 (series Schottky) make +5V_PYC, the diode-ORable copy of the port's 5 V.

D301
MBR120VLSFT1G
PYC_5V_FUSED
+5V_PYC

Diode-OR Schottky

PLACE: Place C301 at J301 pin 6 and U301 pin 5 with a short return; R303 is a 1206 position, keep it accessible for the PPTC swap.

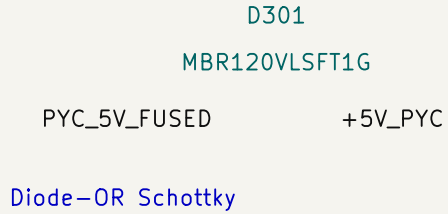
ROUTE: PYC_CONN_5V and +5V_PYC are Default-class rails sized for the port's 1.0 A shared budget; +5V_PYC leaves at the port via to be ORed with +5V_USB.

ROUTE: PYC_DIO_A and PYC_DIO_B are Default-class logic to the MCU sheet, which assigns RX to DIO-A and TX to DIO-B.

ROUTE: PYC_DIO_A_INST and PYC_DIO_B_INST are INSTRUMENT-class taps; they carry no drive.

3. Port 5 V, fuse position and diode-OR

C301 bypasses the raw PYC_CONN_5V node; R303 (fuse position) and D301 (series Schottky) make +5V_PYC, the diode-ORable copy of the port's 5 V.



PLACE: Place C301 at J301 pin 6 and U301 pin 5 with a short return; R303 is a 1206 position, keep it accessible for the PPTC swap.

ROUTE: PYC_CONN_5V and +5V_PYC are Default-class rails sized for the port's 1.0 A shared budget; +5V_PYC leaves at the port via to be ORed with +5V_USB.

---

4. Power drive declarations

These nets have an explicit ERC power source declaration.

Power driven:
PYC_CONN_5V

INTERFACES

Raw port 5 V, J301 pin 6, before R303; the clamp's upper reference.

Port 5 V after fuse position R303 and Schottky D301; diode-OR with +5V_USB.

Signal return, J301 pin 2 and shell SH; clamp and bypass return.

DIO-A (J301 pin 1) after R301: controller TX, this board's RX; SCL or MOSI.

DIO-B (J301 pin 4) after R302: controller RX, this board's TX; SDA or MISO.

Instrument tap of DIO-A through R304 (100 ohm); observe only.

Instrument tap of DIO-B through R305 (100 ohm); observe only.

OPERATION

Pin map of J301: 1 DIO−A, 2 GND, 4 DIO−B, 6 port 5 V; pins 3, 5, 7 and 8 are no−connect. DIO−A carries the controller's TX, SCL or MOSI and is this board's RX; DIO−B is the controller's RX, SDA or MISO and this board's TX (board−interfaces pycontrol−behavior−port.md, the one invariant). Ports are named by connector position so a board cannot mirror them; cross to RX/TX once, at the MCU sheet.

Each DIO line passes a 100 ohm series resistor (R301 on DIO−A, R302 on DIO−B); U301 (USBLC6−2P6) clamps both lines and the 5 V node on the connector side of the resistors, so each line routes in one I/O pad and out the other. The controller has nothing in series (its ports carry only an ESD array), so these resistors are the link's only current limit; 100 ohm into the clamp's 3.5 pF is far below the 8.7 us bit of 115200 8N1. USBLC6−2P6: 6 V minimum VBUS breakdown, 12 V typical clamp at 1 A 8/20 us, IEC 61000−4−2 level 4 (15 kV).

PYC_CONN_5V is the raw pin−6 node, bypassed by C301 (100 nF) and the clamp's upper reference, so pin 6 must be wired for the clamps to reference; +5V_PYC is the same node through R303 and D301 (MBR120VLSFT1G, 20 V 1 A Schottky, 0.34 V max at 1 A, 0.6 mA leakage at 25 C) for diode−ORing with the USB block's +5V_USB. R303 is a polyfuse position: the pyControl port shares one 1.0 A supply with the controller's own regulator and has no per−port fuse, so the stocked 0.36 ohm 1206 is a jumper until a 250 to 500 mA PPTC is in the catalog. R303 and D301 may be DNP on a board that takes no port power.

Not every port has a UART: Breakout 1.2 has one on ports 1, 3 and 4 only, the H7 breakout routes seven but the firmware declares none yet (pycontrol−behavior−port.md). Pin 5 is DIO−C on some ports and a POW−C sink−driver output on others, which is why it stays unconnected. The placing board records the port assignment and uses a UART−capable port; the pin map is cited from the syringe−pump module and H7 breakout schematics, not bench−verified.

R304 and R305 (100 ohm) tap DIO−A and DIO−B for the instrument port (INSTRUMENT class), observe only; these are the block's own signals, so the taps live here (convention 14).

Beyond the two instrument taps, the only schematic difference from the horizontal block: the jack is shielded and both shell legs (pad SH, joined by the shell) are tied to GND here; break that tie and terminate through a pad/cap network if the cable shield must float from signal ground.

DESIGN NOTES

DIO_A (pin 1) is ALWAYS the host's driving line: UART TX, I2C SCL, SPI MOSI.
□ DIO_B (pin 4) is the host's input: UART RX, I2C SDA, SPI MISO. No exceptions □ on any pyControl breakout. So DIO_A = this board's RX.
□ Breakout 1.2 UART ports: 1 (UART4), 3 (USART1), 4 (USART3). I2C only on 3, 4.
□ H7 breakout UART ports: 1,2,3,4,5,9,10. I2C on 1, 6. SPI on 7, 8.
□ Breakout 1.2 analog−in on DIO_A/B works on ports 1 and 6 ONLY (2/3/4/5 are □ GPIOB6−13, no ADC channel). Port 6 DIO_B is the same net as BNC−2.
□ DIO_C (pin 5) is NOT 5V tolerant where it is a DAC (PA4/PA5). DIO_A/DIO_B are FT.

DESIGN CONTRACT

pyControl behavior−port boundary on a VERTICAL, top−entry SHIELDED 8P8C RJ−45 jack: Molex 855085001, OW−CONN−RJ45−8P8C−THT−VERT, Cat5e, 16.5 mm tall, 1.5 A per contact, through−hole signal contacts plus two through−hole shell legs and two locator pegs. NOT Ethernet and no magnetics − the jack is a connector family, nothing more. The same front end as the horizontal pycontrol_behavior_port_rj45_boundary block: pin map 1 DIO−A, 2 GND, 4 DIO−B, 6 5V with pins 3, 5, 7, 8 explicitly no−connect; 100 ohm series resistance and a USBLC6−2P6 channel on both DIO lines, with the clamp on the connector side of the resistors and each line routing in one I/O pad and out the other; 100nF on the raw 5 V node; and the same 5 V branch exposing PYC_CONN_5V, the raw pin−6 node, and +5V_PYC, the same node through R303 and a MBR120VLSFT1G series Schottky, for diode−ORing with other 5 V sources − pair it with usb2_vertical's +5V_USB. WATCH THE DIRECTION: pin 1 DIO−A carries the host's transmit and is the DEVICE'S RX; pin 4 DIO−B is the device's TX. Boundary pins are named by connector position, not by direction, so a board cannot mirror them by accident.
R303 IS A POLYFUSE POSITION, not protection: the pyControl port supplies a shared 1.0 A that also feeds the controller's own logic regulator, with no per−port fuse, so a fault on the board can reset the experiment controller. Populate a 1206 PPTC holding 250−500 mA when one is in the catalog; the 0.36 ohm resistor is only a stocked 1206 jumper, and the position must be populated or the branch is open. The USBLC6's clamp rail taps PYC_CONN_5V upstream of R303 so it stays low−impedance and stays referenced if the fuse trips, which also means pin 6 must be present for the I/O clamps to have an upper reference. On a board that takes no port power, R303 and D301 can both be DNP. Pin 5 is DIO−C on some breakout ports and a POW−C sink driver output on others, so it is deliberately unconnected; do not repurpose it without fixing the port assignment first. The assigned port must be UART−capable.
Two schematic differences from the horizontal block. This jack is shielded: both shell legs are pad SH, joined by the metal shell (duplicate_pad_numbers_are_jumpers), and this block ties SH directly to GND. If the cable shield ever needs isolating from signal ground, break that tie here and terminate through a pad/cap network instead − the same choice usb2 makes for the USB−C shell. And the DIO lines carry instrument taps: R304 and R305 (100 ohm) tap the board side of DIO−A and DIO−B to PYC_DIO_A_INST and PYC_DIO_B_INST, observe only; these are the block's own signals, so the taps live here. Ports PYC_DIO_A, PYC_DIO_B, PYC_CONN_5V, +5V_PYC and GND keep their names from the horizontal block; the two INST taps are added.
The land pattern differs completely from the horizontal block, which is why this is a separate block and not a footprint swap. Signal rows are staggered at y = 0 (pins 1, 3, 5, 7) and y = −2.54 (pins 2, 4, 6, 8), 1.27 mm x pitch, 1.4 mm pads on a 0.89 mm drill, against the horizontal 43860−0001's y = 1.78 / 0 at 1.02 mm pitch on 1.5 mm pads. PAD ORDER REVERSES: pin 1 sits at x = 0 and ascends in +x to pin 8 at x = 8.89, where the horizontal starts pin 1 at x = +3.56 and descends. Two SH pads are 2.11 mm on a 1.6 mm drill at y = 9.4, far outboard of the signal rows, and the two 3.25 mm NPTH locators move from y = 4.32 to y = 6.35. No pad lands where it used to. Unlike the tier 1 terminal blocks and usb2_vertical, this footprint GROWS rather than shrinking: courtyard is x −4.66 to 13.55, y −4.70 to 13.10, roughly 18.2 x 17.8 mm, against the horizontal's x +/−8.00, y −5.84 to 9.65, roughly 16.0 x 15.5 mm, and the body no longer overhangs the board edge, so budget the area before placing.
VERIFY PIN 1 PHYSICALLY against the latch and keyway, not against the footprint's local x order, because the two footprints number pads in opposite directions and a mirrored 8P8C map produces a silently crossed pyControl port; check against ../mouse−joystick−pcb/docs/pycontrol−port−pinout.md. The two locator holes are not optional − the part will not seat without them, they sit inside the connector body where it is tempting to route, and the shell legs punch every layer, so place all four holes before pouring GND or routing the port. Retention is the reason to prefer this part over the SMD OW−CONN−RJ45−8P8C−SMD−VERT fallback: insertion and extraction force goes into the board rather than into solder joints, on a rig that gets handled. The cable now leaves perpendicular to the board, so the enclosure in ../mouse−joysticks−mech needs an aperture above the jack plus clearance for the plug body, its latch, and the wire loop, well beyond the 16.5 mm jack height. Not pad−compatible with OW−CONN−438600001 or OW−CONN−RJ45−8P8C−SMD−VERT, and deliberately shares no equiv_group with either.
Pinout is schematic−derived from the syringe−pump pyControl module and the pyControl H7 breakout, which agree on all eight positions, but it is CITED, NOT BENCH−VERIFIED − confirm continuity and cable polarity on real hardware before trusting a populated board. +5V_PYC leaves D301 pad 1 into a port via, where a placing board picks the rail up.

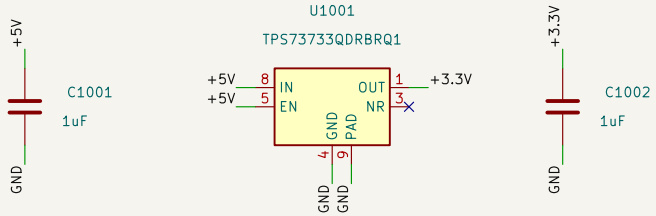
5 V to 3.3 V regulator | TPS73733 fixed 3.3 V LDO

Clean 3.3 V linear regulator from a 5 V input rail using the TI TPS73733 fixed 3.3 V 1 A LDO.

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Regulator and bypass

U701 regulates +5V to +3.3V with EN tied to IN. C701 bypasses IN to GND, C702 holds OUT to GND; NR is open.



Input bypass

Fixed 3.3 V LDO

Output capacitor

PLACE: Place C701 at pins 8 and 4 and C702 at pins 1 and 4 with short local ground returns; tie the thermal pad to GND copper.

ROUTE: +5V and +3.3V carry the rail classes (PWR_5V_LOCAL, PWR_3V3_LOCAL); the GND return of the pad is the regulator's heat path as well.

INTERFACES

+5V — +5V

Input rail; also drives EN, so the regulator is on whenever it is present.

GND — GND

Common return; regulator ground pin and thermal pad.

+3.3V — +3.3V

Regulated output, 3.3 V fixed.

OPERATION

Signal path: +5V -> U701 (IN, pin 8) -> +3.3V (OUT, pin 1). EN (pin 5) is tied to IN, so the regulator is on whenever +5V is present; there is no enable control inside this block.

NR (pin 3) is left open: no noise-reduction capacitor is fitted. GND (pin 4) and the thermal pad (pin 9) return to GND.

C701 (1 uF) bypasses the input, C702 (1 uF) is the output capacitor; both are the catalog 0402 1 uF part. The rail is rated by the TPS73733 (fixed 3.3 V, 1 A class per the catalog description); derate for the board's actual load and dropout.

DESIGN CONTRACT

Clean 3.3 V linear regulator from a 5 V input rail using the TI TPS73733 fixed 3.3 V 1 A LDO. Intended for MCU, RP2040, TMC logic, encoder interface, and other low-voltage digital circuitry.

Circuit and PCB layout guidance
Migrated from the saved library sheet; circuit and PCB unchanged
Orb Weaver

Sheet: /5v_to_3v3_tps73733_2/
File: 5v_to_3v3_tps73733_2.kicad_sch

Title: 5 V to 3.3 V regulator

Size: A4	Date: 2026-10-04	**Rev: Source migration 1**
KiCad E.D.A. 10.0.6		Id: 10/20

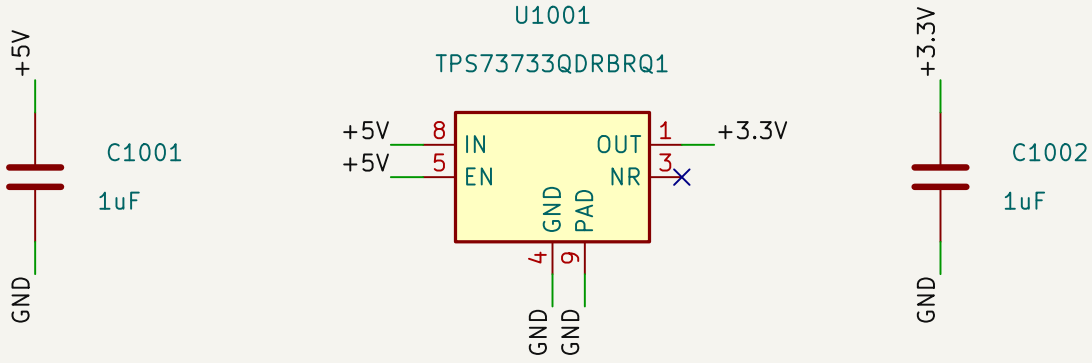
5 V to 3.3 V regulator | TPS73733 fixed 3.3 V LDO

Clean 3.3 V linear regulator from a 5 V input rail using the TI TPS73733 fixed 3.3 V 1 A LDO.

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Regulator and bypass

U701 regulates +5V to +3.3V with EN tied to IN. C701 bypasses IN to GND, C702 holds OUT to GND; NR is open.



Input bypass

Fixed 3.3 V LDO

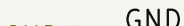
Output capacitor

PLACE: Place C701 at pins 8 and 4 and C702 at pins 1 and 4 with short local ground returns; tie the thermal pad to GND copper.

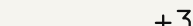
ROUTE: +5V and +3.3V carry the rail classes (PWR_5V_LOCAL, PWR_3V3_LOCAL); the GND return of the pad is the regulator's heat path as well.

INTERFACES

Input rail; also drives EN, so the regulator is on whenever it is present.



Common return; regulator ground pin and thermal pad.



Regulated output, 3.3 V fixed.

OPERATION

Signal path: +5V –> U701 (IN, pin 8) –> +3.3V (OUT, pin 1). EN (pin 5) is tied to IN, so the regulator is on whenever +5V is present; there is no enable control inside this block.

NR (pin 3) is left open: no noise–reduction capacitor is fitted. GND (pin 4) and the thermal pad (pin 9) return to GND.

C701 (1 uF) bypasses the input, C702 (1 uF) is the output capacitor; both are the catalog 0402 1 uF part. The rail is rated by the TPS73733 (fixed 3.3 V, 1 A class per the catalog description); derate for the board's actual load and dropout.

DESIGN CONTRACT

Clean 3.3 V linear regulator from a 5 V input rail using the TI TPS73733 fixed 3.3 V 1 A LDO. Intended for MCU, RP2040, TMC logic, encoder interface, and other low–voltage digital circuitry.

USB-C USB2 device port, vertical receptacle | USB4145, USBLC6 clamp, Rd 5.1 k, 5 V diode-OR

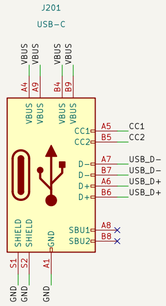
USB-C USB2 device-port front end on a VERTICAL, top-entry receptacle: GCT USB4145-03-0070-C, OW-CONN-USB-C-USB2-SMD-VERT, 16P USB2-only, SMT contacts plus four through-hole shell legs, 7.46 mm tall.

Matching net labels are connected. Group order explains function: PCB placement priorities are stated below.

1. Receptacle and ESD clamp

J201 brings VBUS, GND, D+/D-, CC1/CC2 and the shell onto the board; U201 clamps USB_D+, USB_D- and VBUS to GND right at the receptacle. C201 holds the raw VBUS node at the clamp; D201 passes VBUS to +5V_USB and blocks the other 5 V source from feeding back into the host.

ESD clamp on D+, D- and VBUS
C201: VBUS bypass at the clamp
D201: Diode-OR Schottky



usb-connector

PLACE: Place U201 hard against J201 with a ground via at its pin 2; route each data line in one I/O pad and out the other.

PLACE: Place J201's four shell-leg holes and two locator pegs before pouring GND or routing the port; the part does not seat without them.

PLACE: Place C201 between U201 pin 5 and the GND via; D201 sits where +5V_USB leaves the block at its port via.

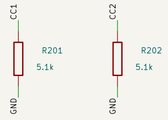
ROUTE: USB_D+ and USB_D- are the USB_HS pair: equal length, coupled at the class gap, brought to the block boundary already coupled.

ROUTE: Jump one leg of each pair once at the body centre for the A/B tie; the 0.3 mm gap at the outer contacts is unroutable.

ROUTE: VBUS and +5V_USB are Default-class rails for the port's 5 V budget; +5V_USB is picked up at the port via by the placing board.

2. CC sink declaration

R201 and R202 (5.1 k) pull CC1 and CC2 to GND: the port presents itself as a sink; nothing reads the source's advertisement.



CC Rd sink pulldowns CC Rd sink pulldowns

PLACE: Keep R201 at A5 and R202 at B5 with short returns: no other load on CC1 or CC2.

ROUTE: CC1 and CC2 are Default-class local nets that end at the resistors.

3. Power drive declarations

These nets have an explicit ERC power source declaration.

Power driven: VBUS

INTERFACES

VBUS — VBUS

Raw bus 5 V, J201 A4, A9, B4, B9; bypassed by C201, the clamp's reference.

+5V_USB — +5V_USB

VBUS through D201 (Schottky, about 0.3 V drop) for diode-ORing with +5V_PYC.

GND — GND

USB ground: J201 A1, B1, A12, B12 and shell S1 to S4; clamp and Rd return.

USB_D+ — USB_D+

USB 2.0 D+, J201 A6 and B6, after the U201 clamp; USB_HS pair with USB_D-.

USB_D- — USB_D-

USB 2.0 D-, J201 A7 and B7, after the U201 clamp; USB_HS pair with USB_D+.

INTERNAL NETS

CC1: Configuration channel for one plug orientation, J201 A5 to R201 (Rd, 5.1 k to GND); nothing reads it.

CC2: Configuration channel for the other orientation, J201 B5 to R202 (Rd, 5.1 k to GND); nothing reads it.

OPERATION

Signal path: J201 D+ (A6, B6) and D- (A7, B7) pass U201's I/O pads to USB_D+ and USB_D-; both receptacle rows are tied so either plug orientation works. SBU1 and SBU2 (A8, B8) are no-connect: USB2 only, for an RP2040-class device controller.

CC: R201 on CC1 (A5) and R202 on CC2 (B5), 5.1 k to GND, declare a UFP (sink). Nothing reads the CC level, so budget the load against a default-power source unless the host is known to advertise 1.5 A or 3 A.

ESD: U201 (USBLC6-2P6) clamps D+, D- and VBUS: 3.5 pF max per line, 1.7 pF max line to line, 6 V minimum VBUS breakdown, 12 V typical clamp at 1 A 8/20 us, IEC 61000-4-2 level 4 (15 kV air and contact). Clamp performance is set by connection inductance: pin 2 to a ground via, each data line in one I/O pad and out the other.

VBUS: C201 (100 nF) bypasses the raw bus; D201 (MBR120VLSFT1G, 20 V 1 A Schottky, 0.34 V max at 1 A, 0.6 mA leakage at 25 C) makes +5V_USB for diode-ORing with the pyControl block's +5V_PYC. The shell pads S1 to S4 are tied to GND here; isolate them through a pad/cap network instead if the shield must float.

Land pattern (from the block's own record): contacts in two rows on opposite sides of the body at 0.5 mm pitch, every pad 0.3 mm wide; the A/B ties for D+ and D- cross at the body centre with one via jump per pair leg and equal lengths; VBUS and GND each land on four pads to be used in parallel for the 3 A rating. Four plated shell legs and two 0.71 mm locator pegs are mandatory for seating. The cable leaves perpendicular to the board (7.46 mm connector height), so the enclosure needs an aperture above it.

DESIGN CONTRACT

USB-C USB2 device-port front end on a VERTICAL, top-entry receptacle: GCT USB4145-03-0070-C, OW-CONN-USB-C-USB2-SMD-VERT, 16P USB2-only, SMT contacts plus four through-hole shell legs, 7.46 mm tall. Electrically identical to the horizontal usb2 block: USBLC6-2P6 ESD clamp on D+/D- and VBUS, 5.1k Rd pulldowns on CC1 (A5) and CC2 (B5) declaring a sink, 100nF on VBUS, a MBR120VLSFT1G series Schottky from VBUS to +5V_USB for diode-ORing with other 5 V sources (pair it with pycontrol_behavior_port_j145's +5V_PYC), PWR_FLAG on VBUS, SBU1/SBU2 deliberately unconnected, all four shell pads S1-S4 tied to GND. Ports are VBUS, +5V_USB, GND, USB_D+, USB_D-.
Nothing reads the CC advertisement, so budget the load against a default-power source unless the host is known to advertise 1.5 A or 3 A.
Only the land pattern differs from usb2, and it differs completely, which is why this is a separate block and not a footprint swap: contacts sit in two rows on OPPOSITE sides of the body at y = +/-1.485, 0.5 mm pitch across the six inner contacts and 1.5 mm out to the outer pads, and EVERY pad is 0.3 mm wide, where the horizontal GT-USB-7047C merges A and B into one row and gives VBUS and GND 0.6 mm pads. Three consequences follow for the layout. The A/B ties are the layout's work: D+ (A6/B6) and D- (A7/B7) cross at the body centre and cannot be taken around the ends, because the 0.3 mm gap between the outer contact and the shell-leg pad is unroutable at 0.2/0.2 and the plated leg blocks every layer there, so budget one via jump for one leg of the pair and keep both legs equal length. VBUS lands on four 0.3 mm pads (A4/A9/B4/B9) and GND on four (A1/A12/B1/B12): use all four of each in parallel for the 3 A rating and drop their ties to an inner layer rather than crowding the 1.8 mm corridor between the rows, which the two data joins need. The four shell legs are plated ovals on a 1.1 x 0.6 drill at x = +/-4 and punch every layer, and the two 0.71 mm NPTH locator pegs at (+/-4, 0) are mandatory for seating: place all six before pouring GND or routing the port.
Mechanically the courtyard shrinks to x +/-5.05, y +/-2.31 from the horizontal part's x +/-6.00, y -1.25 to +6.75, so the connector stops needing about 6.75 mm of board past the contacts and can move inboard, but the cable now leaves perpendicular to the board: the enclosure needs an aperture above it plus clearance for the plug body and its wire loop, well beyond the 7.46 mm connector height.
Keep the USBLC6 hard against the receptacle with a ground via at its pin 2 and route each data line in one I/O pad and out the other (clamp performance is dominated by connection inductance), and bring USB_D+/USB_D- to the block boundary already coupled at the USB_HS netclass gap.
+5V_USB leaves D201 pad 1 into a port via, where a placing board picks the rail up.

Circuit and PCB layout guidance
Migrated from the saved library sheet; circuit and PCB unchanged
Orb Weaver

Sheet: /usb2_vertical/	
File: usb2_vertical.kicad_sch	
Title: USB-C USB2 device port, vertical	
Size: A2	Date: 2026-10-04
KiCad E.D.A. 10.0.6	**Rev: Source migration 1**
	Id: 2/20

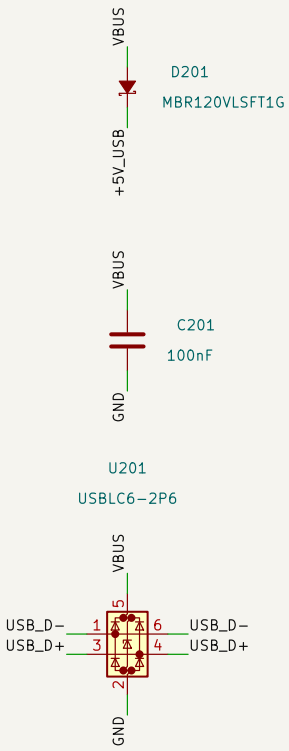
USB-C USB2 device port, vertical receptacle | USB4145, USBLC6 clamp, Rd 5.1 k, 5 V diode-OR

USB-C USB2 device-port front end on a VERTICAL, top-entry receptacle: GCT USB4145-03-0070-C, OW-CONN-USB-C-USB2-SMD-VERT, 16P USB2-only, SMT contacts

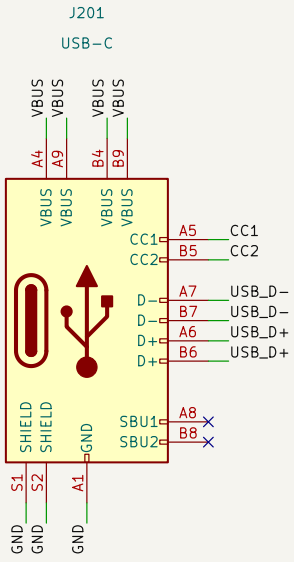
Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Receptacle and ESD clamp

J201 brings VBUS, GND, D+/D-, CC1/CC2 and the shell onto the board; U201 clamps USB_D+, USB_D- and VBUS to GND right at the receptacle. C201 holds the raw VBUS node at the clamp; D201 passes VBUS to +5V_USB and blocks the other 5 V source from feeding back into the host.



ESD clamp on D+, D- and VBUS
C201: VBUS bypass at the clamp
D201: Diode-OR Schottky



usb-connector

PLACE: Place U201 hard against J201 with a ground via at its pin 2; route each data line in one I/O pad and out the other.

PLACE: Place J201's four shell-leg holes and two locator pegs before pouring GND or routing the port; the part does not seat without them.

PLACE: Place C201 between U201 pin 5 and the GND via; D201 sits where +5V_USB leaves the block at its port via.

ROUTE: USB_D+ and USB_D- are the USB_HS pair: equal length, coupled at the class gap, brought to the block boundary already coupled.

ROUTE: Jump one leg of each pair once at the body centre for the A/B tie; the 0.3 mm gap at the outer contacts is unroutable.

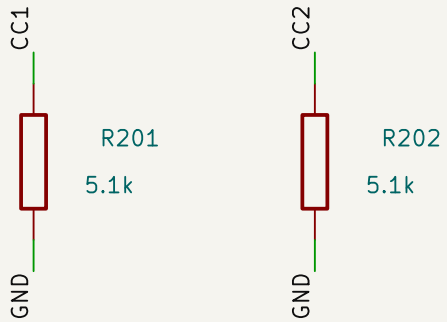
ROUTE: VBUS and +5V_USB are Default-class rails for the port's 5 V budget; +5V_USB is picked up at the port via by the placing board.

5 6 7 8

s four through-hole shell legs, 7.46 mm tall.

2. CC sink declaration

R201 and R202 (5.1 k) pull CC1 and CC2 to GND: the port presents itself as a sink; nothing reads the source's advertisement.



CC Rd sink pulldowns CC Rd sink pulldowns

PLACE: Keep R201 at A5 and R202 at B5 with short returns; no other load on CC1 or CC2.

ROUTE: CC1 and CC2 are Default-class local nets that end at the resistors.

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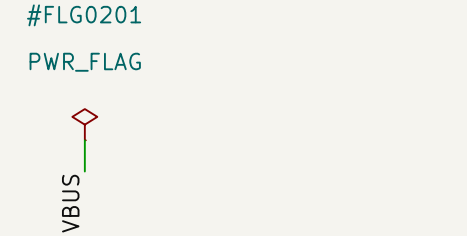
3. Power drive declarations

These nets have an explicit ERC power source declaration.



Power driven: VBUS

INTERFACES

Raw bus 5 V, J201 A4, A9, B4, B9; bypassed by C201, the clamp's reference.

VBUS through D201 (Schottky, about 0.3 V drop) for diode−ORing with +5V_PYC.

USB ground: J201 A1, B1, A12, B12 and shell S1 to S4; clamp and Rd return.

USB 2.0 D+, J201 A6 and B6, after the U201 clamp; USB_HS pair with USB_D−.

USB 2.0 D−, J201 A7 and B7, after the U201 clamp; USB_HS pair with USB_D+.

INTERNAL NETS

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CC2: Configuration channel for the other orientation, J201 B5 to R202 (Rd, 5.1 k to GND); nothing reads it.

OPERATION

Signal path: J201 D+ (A6, B6) and D− (A7, B7) pass U201's I/O pads to USB_D+ and USB_D−; both receptacle rows are tied so either plug orientation works. SBU1 and SBU2 (A8, B8) are no−connect: USB2 only, for an RP2040−class device controller.

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DESIGN CONTRACT

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Mechanically the courtyard shrinks to x +/−5.05, y +/−2.31 from the horizontal part's x +/−6.00, y −1.25 to +6.75, so the connector stops needing about 6.75 mm of board past the contacts and can move inboard, but the cable now leaves perpendicular to the board: the enclosure needs an aperture above it plus clearance for the plug body and its wire loop, well beyond the 7.46 mm connector height.
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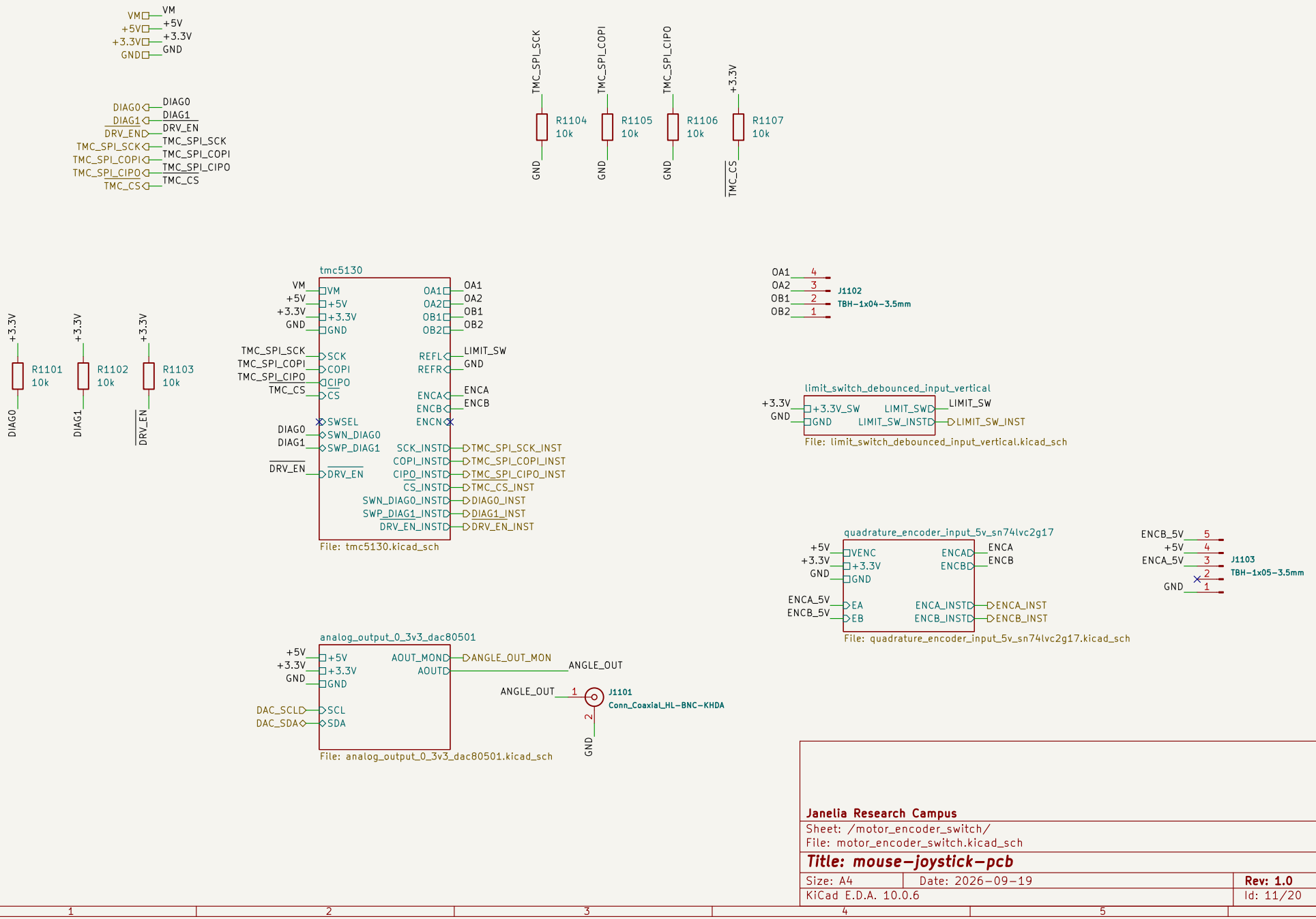
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+5V
+3.3V
GND
DIAG0
DIAG1
DRV_EN
TMC_SPI_SCK
TMC_SPI_COPI
TMC_SPI_CIPO
TMC_CS
R1104 10k
R1105 10k
R1106 10k
R1107 10k
R1101 10k
R1102 10k
R1103 10k
tmc5130
SWSEL
SWN_DIAG0
SWP_DIAG1
OA1
OA2
OB1
OB2
LIMIT_SW
SCK_INST
COPI_INST
CIPO_INST
CS_INST
SWN_DIAG0_INST
SWP_DIAG1_INST
DRV_EN_INST
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J1102
TBH-1x04-3.5mm
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LIMIT_SW_INST
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EB
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ENCB
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Date: 2026-09-19
Rev: 1.0
KiCad E.D.A. 10.0.6
Id: 11/20

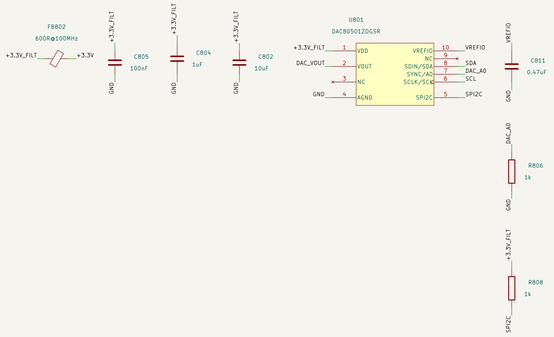
Analog output 0–1.650 V | DAC80501 on I2C, 987 Hz Sallen–Key, OPA197 x1.32, /2 divider

Single-channel buffered 0–1.650 V precision analog voltage output, safe on a Neuropixels OneBox ADC channel or an unprotected 3.3 V MCU pin: a DAC80501ZDGSR at 3.3 V on I2C at address 0x4B on its internal 2.5 V reference, a 2-pole 987 Hz Sallen–Key reconstruction filter, an OPA197 on a ferrite-filtered 5 V rail at a non-inverting DC gain of 1.32 that is also the filter's active element, a /2 output divider, a 249 ohm series output resistor, an ESD clamp and a separately isolated monitor tap.

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. DAC and address straps

U801 generates 0–2.5 V on its internal reference; R808 selects I2C. RR06 sets the address 0x48. CB11 bypasses VREFIO. FB801 filters +5V to +5V_FILT for U802 (CB01, CB03, CB06, CB08); FB802 filters +3.3V to +3.3V_FILT for U801 (CB02, CB04, CB05).



16-bit I2C DAC, internal 2.5 V reference
C802: 3.3 V rail bulk bypass; C804: Rail bypass; C805: U801 VDD pin 1 bypass; FB802: Rail ferrites
RR06: A0 strap to GND, address 0x48
R808: SPI2C strap to VDD, I2C mode
C811: VREFIO reference bypass

PLACE: C811 (0.47 uF; 150 nF or more is required) hard against pin 10 with the shortest return to pin 4 (AGND).

PLACE: Silkscreen the address next to RR06.

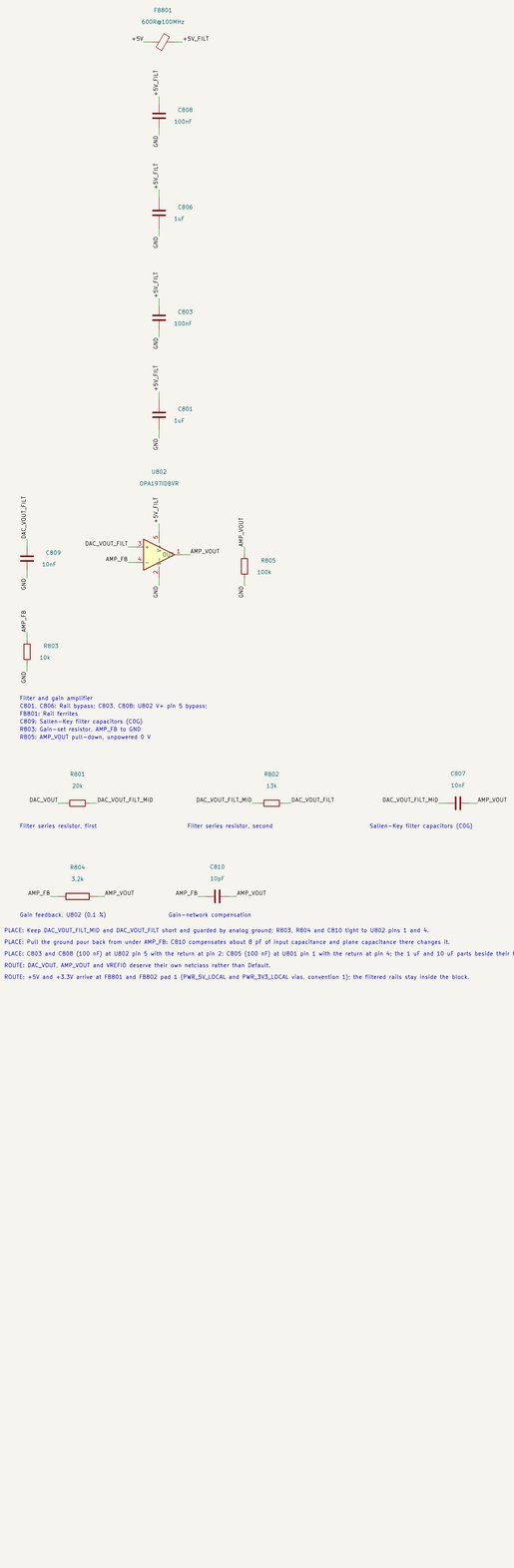
PLACE: C803 and C808 (100 nF) at U802 pin 5 with the return at pin 2; C805 (100 nF) at U801 pin 1 with the return at pin 4: the 1 uF and 10 uF parts beside their ferrites.

ROUTE: SCL and SDA run straight from the ports to pins 6 and 8: no termination or tap inside the block (conventions 10 and 14: the shared I2C pulls are the board's).

ROUTE: +5V and +3.3V arrive at FB801 and FB802 pad 1 (PWR_5V_LOCAL and PWR_3V3_LOCAL vias, convention 1): the filtered rails stay inside the block.

2. Reconstruction filter and gain amplifier

R801, R802, C807 and C809 around U802 form the 987 Hz Sallen–Key filter: RR03 and RR04 set the gain 1.32 and CB10 compensates the gain network. FB801 filters +5V to +5V_FILT for U802 (C801, C803, C806, C808); FB802 filters +3.3V to +3.3V_FILT for U801 (C802, C804, C805).



Filter and gain amplifier
CB01, CB06: Rail bypass; CB03, CB08: U802 V+ pin 5 bypass;
FB801: Rail ferrites
CB09: Sallen–Key filter capacitors (COG)
RR03: Gain-set resistor, AMP_FB to GND
RR05: AMP_VOUT pull-down, unpowered 0 V

Filter series resistor, first

Filter series resistor, second

Sallen–Key filter capacitors (COG)

Gain feedback, U802 (0.1 %)

Gain-network compensation

PLACE: Keep DAC_VOUT_FILT_MID and DAC_VOUT_FILT short and guarded by analog ground: RR03, RR04 and CB10 tight to U802 pins 1 and 4.

PLACE: Pull the ground pour back from under AMP_FB: CB10 compensates about 8 pF of input capacitance and plane capacitance there changes it.

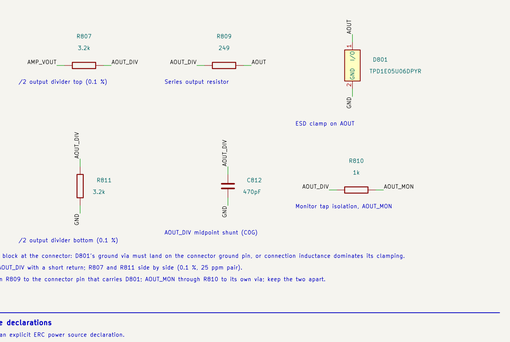
PLACE: C803 and C808 (100 nF) at U802 pin 5 with the return at pin 2; C805 (100 nF) at U801 pin 1 with the return at pin 4: the 1 uF and 10 uF parts beside their ferrites.

ROUTE: DAC_VOUT, AMP_VOUT and VREFIO deserve their own netclass rather than Default.

ROUTE: +5V and +3.3V arrive at FB801 and FB802 pad 1 (PWR_5V_LOCAL and PWR_3V3_LOCAL vias, convention 1): the filtered rails stay inside the block.

3. Output divider, series resistor and ESD clamp

RR07 and RR11 halve AMP_VOUT to AOUT_DIV; RR09 delivers AOUT with DB01 clamping it; RR10 isolates the AOUT_MON tap; RR05 defines AMP_VOUT at 0 V unpowered: CB12 shunts pickup on the midpoint.



PLACE: Place the block at the connector: DB01's ground via must land on the connector ground pin, or connection inductance dominates its clamping.

PLACE: CB12 at AOUT_DIV with a short return: RR07 and RR11 side by side (0.1 %, 25 ppm pair).

ROUTE: AOUT from RR09 to the connector pin that carries DB01: AOUT_MON through RR10 to its own via; keep the two apart.

4. Power drive declarations

These nets have an explicit ERC power source declaration.

INTERFACES

+5V — +5V

Amplifier supply, a regulated 5.0 V rail in the same switched domain, through FB801 to +5V_FILT (U802 V+, 4.5 V minimum).

+3.3V — +3.3V

DAC supply, the switched 3.3 V domain, through FB802 to +3.3V_FILT (U801 VDD): must be the switched rail or the DAC's input clamps back-power the domain.

GND — GND

Analog return of the DAC, amplifier, filter, divider and ESD clamp; flagged once at board level, not here.

SCL — SCL

I2C clock to U801 pin 6 (SCLK/SCL); leaves as a single-pin net, the board fits the pull-up.

SDA — SDA

I2C data, U801 pin 8 (SDIN/SDA), address 0x4B; leaves as a single-pin net, the board fits the pull-up.

AOUT — AOUT

Delivered output, 0–1.650 V from a 1.849 kohm source (RR09 plus the divider); needs a >= 1 Mohm load; ESD-clamped by DB01; any single fault is bounded to 2.55 V.

AOUT_MON — AOUT_MON

Monitor tap of AOUT_DIV through RR10 (1 k): the same 0–1.650 V as AOUT, isolated from it: an instrument reads here.

OPERATION

Signal path: U801 VOUT (pin 2, 0–2.5 V on the internal reference) -> RR01 (20 k) -> DAC_VOUT_FILT_MID -> RR02 (13 k) -> DAC_VOUT_FILT -> U802 + (pin 3). CB07 (10 nF, midpoint to AMP_VOUT) and CB09 (10 nF to GND) make a Sallen-Key low-pass with U802 as the active element: f0 987 Hz, Q 0.61, group delay 266 us, matched to the torque block's 263 us. RR04 (5.2 k) over RR03 (10 k) sets the gain 1 + 5.2/10 = 1.32, so AMP_VOUT is 0–3.300 V: RR07 and RR11 (3.2 k each) halve it to AOUT_DIV, 0–1.650 V (LSB 25.2 uV); RR09 (249 ohm) delivers AOUT and RR10 (1 k) taps AOUT_MON.

I2C, address 0x4B: RR08 (1 k to +3.3V_FILT) latches SPI2C for I2C at power-up; RR06 (1 k to GND) sets A0 to 0x4B (the brake block takes 0x49). A0 is a four-state pin re-sampled during the first byte of every frame, so a floating A0 gives an address that changes between frames: never lift RR06 without re-wiring it in the same operation. The block owns no bus termination: SCL and SDA leave as single-pin nets and the board fits one 2.2 k pull-up pair per bus segment, the DAC-side pair on the switched 3.3 V rail.

Firmware writes GAIN (4h) = 0x0101 before any DATA write. At a 3.3 V VDD the reset default is out of spec against the 2.5 V reference, so the reference alarm holds VOUT at 0 V until that write lands, and STATUS reports it over I2C. The measured output floor is 4.5 mV at AMP_VOUT, 2.25 mV at AOUT: map the signal range above it and keep 0 V for unpowered or faulted.

Loading and fault bounds: AOUT needs a >= 1 Mohm load (−0.185 % of gain into 1 Mohm, −1.82 % into 100 kohm). RR09 bounds a short to ground at 6.6 mA: the /2 divider bounds any single fault, including U802's output stuck at its 5 V rail, to 2.55 V at the connector. DB01 (TPD1EO5U06, 5.5 V working, +−12 kV contact) clamps ESD transients only, not a DC fault. AOUT and AOUT_MON both tap AOUT_DIV and are electrically interchangeable: verify on the netlist that DB01 shares its net with the connector pin.

Supplies: +5V from a regulated 5.0 V rail (U802 needs 4.5 V) and +3.3V from the switched 3.3 V rail, both in the same switched domain so the output goes dark with its data source: FB801 and FB802 filter them to +5V_FILT and +3.3V_FILT, each carrying a PWR_FLAG. Two instances need separate sheets or DAC_A0, SPI2C and the filtered rails merge.

CB07, CB09 and CB12 are C0G: class-2 dielectric is piezoelectric and this board is coupled to a stepper and a hand-driven joystick. Retune the filter by scaling RR01 and RR02 together; do not raise f0 and do not use CB10 for band limiting. RR05 (100 k) stays on AMP_VOUT, not on the midpoint, where it would become part of the ratio.

DESIGN NOTES

GAIN register (4h) reset = 0x0001 = the 0–5 V span. Write 0x0101 (REF-DIV=1, BUFF-GAIN=1) -> 0–2.5 V at the DAC, 0–3.300 V at AMP_VOUT, 0–1.650 V at AOUT. Do this before any DAC data write.
At a 3.3 V VDD the reset default is out of spec against the 2.5 V internal reference, so the reference alarm shuts the reference buffer down and forces VOUT to 0 V until that write lands: read that 0 V as unpowered or faulted, never as a valid end-of-travel angle. Do not use REF-DIV=0 to recover the 0–5 V span.

A0=GND 0x48

2-POLE SALLEN-KEY RECONSTRUCTION / ANTI-ALIAS FILTER: RR01 (20.0 k), RR02 (13.0 k), CB07 and CB09 (10 nF each) around U802. f0 = 1/(2 pi C sqrt(RR01 x RR02)) with CB07 = CB09 = C; 1/Q = 1/sqrt(a) + sqrt(a) x (2 − K), a = RR01/RR02 = 1.538; K = 1.32; As built: f0 = 987 Hz, Q = 0.606, −3 dB at 827 Hz, −52.3 dB at 20 kHz, 266 us group delay.
WHY IT EXISTS: the acquisition (OneBox AD7616) samples at a fixed 30.3 kHz behind only a 1st-order 39 kHz filter, so it does not anti-alias. The TMCS130A chopper runs 16–30 kHz (the datasheet-recommended range) and every value in that range folds into 0–15 kHz, where it is indistinguishable from joystick motion. This filter is the only band limit in the chain. It also cuts the DAC code-change glitch from 9.9 mV to 14 uV: the OneBox LSB is 152.6 uV on the +/−5 V range.
TO RETUNE: scale RR01 and RR02 by the SAME factor. Q depends only on their ratio, so the shape is preserved and only f0 moves. Do not change C. Ladder, RR01/RR02: f0, rejection at 20 kHz, group delay:
− 64.9k/42.2k: 304 Hz, −72.7 dB, 864 us.
− 39.2k/25.5k: 503 Hz, −64.0 dB, 522 us.
− 20.0k/13.0k: 987 Hz, −52.3 dB, 266 us (as built).
− 9.76k/6.34k: 2.02 kHz, −39.8 dB, 130 us.
− 6.49k/4.22k: 3.04 kHz, −32.7 dB, 86 us.
− 3.92k/2.55k: 5.03 kHz, −24.0 dB, 52 us.
− 2.00k/1.30k: 9.87 kHz, −13.2 dB, 27 us (chopper barely attenuated).
SINGLE-POLE FALLBACK (same pads): RR01 = 0 R jumper, CB07 = DNP, RR02 = 15.0 k; CB09 = 10 nF -> 1.061 kHz, one pole, −25.5 dB at 20 kHz, 150 us. CB07 MUST be DNP in this configuration: with RR01 shorted it would hang 10 nF from the DAC output to the op-amp output.
CONSTRAINTS. C0G ONLY (TI DACx0501 datasheet 9.2.2.6): class-2 dielectric is piezoelectric and this board sits next to a stepper: the series R can only bleed self-generated charge with time constant R x C, which is fixed by f0, so it cannot be filtered away.
CB07 and CB09 must be the SAME value and ideally the same reel. Q depends on CB07/CB09 = 1: matched capacitors make Q immune to capacitor tolerance.
RR01 and RR02 carry no DC current (op-amp Ib = 10 pA), so the DC gain is set ENTIRELY by RR03 and RR04, 1 % here is plenty; do not "upgrade" to 0.1 %.
Keep CB10 = 10 pF. Its pole is at 4.97 MHz and it rolls K toward 1.0 at HF, which lowers Q up there: stabilizing, not destabilizing.
Do not put a shunt capacitor on the connector side of RR09. One large enough to matter there (640 nF for 1 kHz) drives U802 into its +/−65 mA limit on every step, and its corner would track the researcher's cable capacitance.
Group delay is a latency you must MEASURE and report, not assume.
The Sallen-Key stopband floors out above about 1 MHz as the op-amp output impedance rises and CB07 stops bootstrapping. Irrelevant at 16–30 kHz.
LAYOUT: keep DAC_VOUT_FILT_MID and DAC_VOUT_FILT short and surrounded by analog GND.

DESIGN CONTRACT

Single-channel buffered 0–1.650 V precision analog voltage output, safe on a Neuropixels OneBox ADC channel or an unprotected 3.3 V MCU pin: a DAC80501ZDGSR at 3.3 V on I2C at address 0x4B on its internal 2.5 V reference, a 2-pole 987 Hz Sallen–Key reconstruction filter, an OPA197 on a ferrite-filtered 5 V rail at a non-inverting DC gain of 1.32 that is also the filter's active element, a /2 output divider, a 249 ohm series output resistor, an ESD clamp and a separately isolated monitor tap. AMP_VOUT full scale is 2.5 V x (1 + 3.2k/10k) = 3.300 V and AOUT is half of it, 1.650 V, LSB 25.2 uV. Built for the mouse-joystick-pcb encoder angle output, but THE CONNECTOR DELIBERATELY LIVES OUTSIDE THE BLOCK so one block serves any housing. The full derivation, values, return ladder, layout rules and accuracy budget are in kicad-libs docs/analog-output-design.md: this note carries only what breaks silently without it. Designators are not stable (KiCad auto-annotation orders by sheet position), so everything below is named by net.
1. I2C, NOT SPI, AND THE ADDRESS IS ONE RESISTOR. SPI2C is strapped to +3.3V_FILT through 1k for I2C mode; A0 is strapped to GND through 1k for 0x4B, and brake_current_sink_0_v9ma_dac80501 takes 0x49. A0 is a FOUR-STATE pin (AGND 0x4B, VDD 0x49, SDA 0x4A, SCL 0x4B), so a rail strap reaches only the first two. A0 is re-sampled during the first byte of EVERY frame, so a floating A0 gives an address that changes between frames rather than a clean failure: never lift that resistor without re-wiring it in the same operation.
2. THIS BLOCK OWNS NO BUS TERMINATIONS and must not gain any. An earlier revision advertised three 10k SPI idle resistors as a feature: they are DELETED, because two DAC blocks on one bus would put 5k to GND on SDA and SCL and idle the bus at 2.29 V against a 2.2k pull-up, on top of the DAC's 1.62 V VIH minimum. SCL and SDA leave as single-pin nets. The board fits ONE 2.2k pull-up pair PER BUS SEGMENT: the DAC-side pair on the SWITCHED 3.3 V rail, because an always-on pull-up reaching a DAC whose VDD is at 0 V exceeds the VDD+0.3 V digital-input absolute maximum and back-feeds +3.3V_FILT through the internal clamps; the MCU-side pair on the ALWAYS-ON rail, because the SN74CBS3245 is open by default.
3. AOUT AND AOUT_MON ARE TWO DIFFERENT PORTS AND CROSSING THEM IS A DEFECT ERC CANNOT CATCH. Both tap AOUT_DIV, the divider midpoint, so the monitor and the connector read the same voltage. AOUT is the delivered output and carries the 249 ohm source resistor and the ESD clamp; AOUT_MON is a 1k instrument tap. Both are validly driven either way round, so verify on the netlist that the clamp shares a net with the connector pin. Backwards leaves the human-accessible connector with NO ESD protection. This happened once, on mouse-joystick-pcb, 2026-08-27.
4. THE 100k OUTPUT PULL-DOWN STAYS ON AMP_VOUT, upstream of the /2 divider. It defines 0 V when the block is unpowered: on the midpoint it would parallel the bottom leg for about −1.6% of ratio, and it is a 1% 100ppm/C thick film against the divider's 0.1% 25ppm/C pair. General rule: anything whose job is to define a node when the amplifier is dead belongs on the AMP side of a divider; anything in parallel with a divider leg becomes part of the RATIO.
5. AOUT IS 0–1.650 V FROM A 1.849 kohm SOURCE AND NEEDS A >=1 Mohm LOAD. The source is the 249 ohm series resistor PLUS the divider's 1.6 kohm, not 249 ohm alone: against the OneBox AD7616-P's 1 Mohm that is −0.185% of gain, systematic and absorbed by per-board calibration, but a 100 kohm load costs −1.82% and a 50 ohm terminated input reads a fraction of the correct value. The 249 ohm still bounds a short of AOUT to ground at 6.6 mA and 11 mW inside a 62.5 mW 0402. The /2 divider is what bounds a single fault, including the amp's own output stage shorted to its 5 V rail, to 2.55 V on a connector pin, inside an STM32F405's 4.0 V absolute maximum. That bound is a property of the copper, not of a register write. The ESD clamp is a transient device and does NOT bound a DC fault.
6. THE FILTER IS NOT OPTIONAL, ITS CAPACITORS MUST BE C0G from one reel, AND SO MUST THE 470 pF DIVIDER MIDPOINT SHUNT. Class-2 dielectric is piezoelectric, this board is coupled to a stepper and a hand-driven joystick, and on the midpoint that pickup becomes signal. Retune by scaling BOTH series resistors by the same factor and leaving the capacitors alone: Q depends only on their ratio. Do not raise f0 to buy passband: rejection falls as (f0/20kHz)^2 and the chopper is the whole point. The 266 us group delay is a latency to MEASURE and report, and it is deliberately matched to torque_bridge_0_3_ina821's 263 us. The midpoint shunt is 470 pF because it adds only 0.75 us against that budget: the brake block's 10 nF would add 16 us and land the corner a decade above the 987 Hz filter.
7. FIRMWARE MUST WRITE GAIN (4h) = 0x0101 BEFORE ANY DATA WRITE, and at 3.3 V that is a SAFETY PROPERTY rather than a hazard. The reset default 0x0001 is out of spec against the 2.5 V internal reference at a 3.3 V VDD, so the reference alarm holds the output at 0 V until that write lands. This block used to run its DAC at 5 V, where the same default commanded 5 V x 1.32 and the amp clipped near 4.85 V into whatever was on the connector. Over I2C the alarm is also READABLE in STATUS, which is why this block is on I2C at all. Do not use REF-DIV=0 to recover the old span.
8. THE OUTPUT FLOOR IS 4.5 mV MEASURED, 2.25 mV AFTER THE DIVIDER. Map the valid signal range to start above it and reserve true 0 V as the out-of-band unhomed, faulted or unpowered level. That leaves only about 2 mV between a firmware-signalled fault and a dead output section, so STATUS, not the analog level, is the primary discriminator.
9. BIND +3.3V AND +5V TO THE SAME SWITCHED DOMAIN. Feed +5V from a REGULATED 5.0 V rail, never a diode-ORed host rail, so the output goes dark with its data source instead of holding a stale angle. The DAC's +3.3V MUST be the switched rail or it back-powers the switched domain through the DAC's input clamps.
10. PWR_FLAG ON BOTH +3.3V_FILT AND +5V_FILT is required: there are two ferrites and each breaks driver propagation. GND is flagged once at board level, not here.
11. TWO INSTANCES NEED SEPARATE SHEETS or their local nets merge, and DAC_A0 merging would silently put both copies on 0x4B. A twin-axis board needs the SDA and SCL strap states, 0x4A and 0x4B, which a rail strap cannot reach.

Circuit and PCB layout guidance
Migrated from the saved library sheet: circuit and PCB unchanged
Orb Weaver

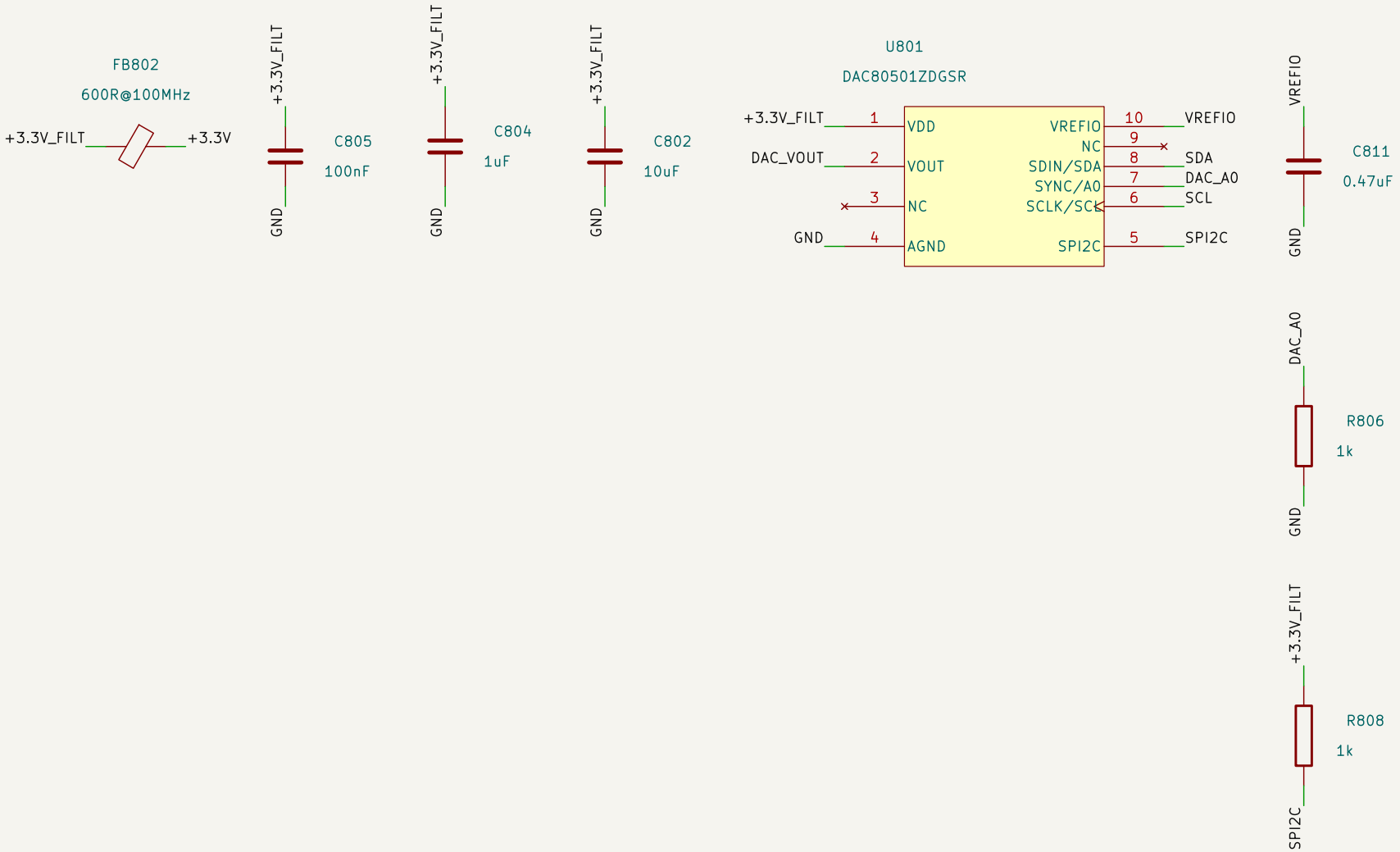
Sheet: /motor_encoder_switch/analog_output_0_3v3_dac80501/
File: analog_output_0_3v3_dac80501.kicad_sch

Title: Analog output 0–1.65 V, DAC80501 and OPA197

Size: A1 | Date: 2026-10-04 | **Rev: Source migration 1**
KiCad E.D.A. 10.0.6 | Id: 8/20

1. DAC and address straps

U801 generates 0–2.5 V on its internal reference; R808 selects I2C, R806 sets the address 0x48, C811 bypasses VREFIO. FB801 filters +5V to +5V_FILT for U802 (C801, C803, C806, C808); FB802 filters +3.3V to +3.3V_FILT for U801 (C802, C804, C805).



16–bit I2C DAC, internal 2.5 V reference
C802: 3.3 V rail bulk bypass; C804: Rail bypass; C805: U801 VDD pin 1 bypass; FB802: Rail ferrites
R806: A0 strap to GND, address 0x48
R808: SPI2C strap to VDD, I2C mode
C811: VREFIO reference bypass

PLACE: C811 (0.47 uF; 150 nF or more is required) hard against pin 10 with the shortest return to pin 4 (AGND).

PLACE: Silkscreen the address next to R806.

PLACE: C803 and C808 (100 nF) at U802 pin 5 with the return at pin 2; C805 (100 nF) at U801 pin 1 with the return at pin 4; the 1 uF and 10 uF parts beside their ferrites.

ROUTE: SCL and SDA run straight from the ports to pins 6 and 8; no termination or tap inside the block (conventions 10 and 14: the shared I2C pulls are the board's).

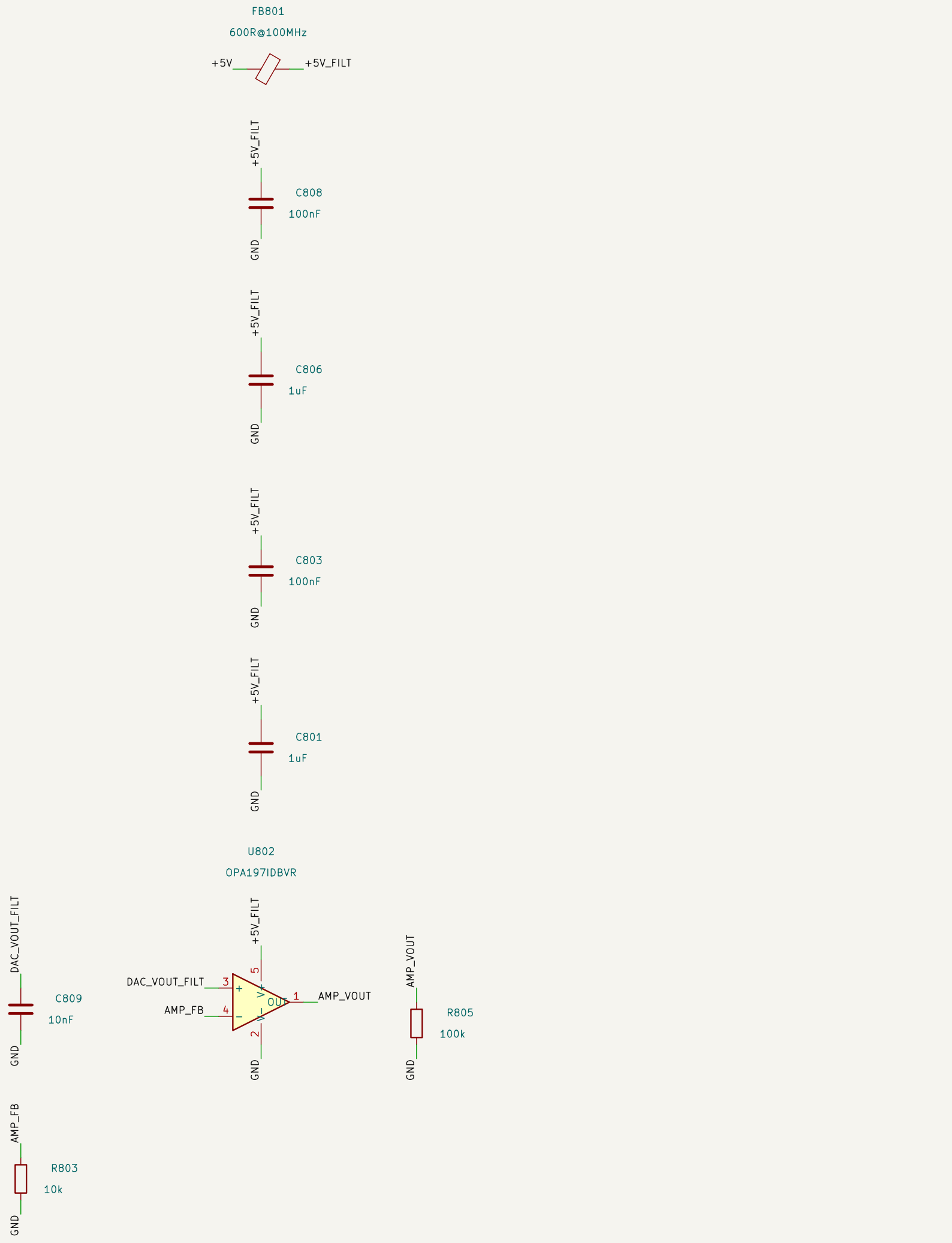
ROUTE: +5V and +3.3V arrive at FB801 and FB802 pad 1 (PWR_5V_LOCAL and PWR_3V3_LOCAL vias, convention 1); the filtered rails stay inside the block.

5 6 7 8 9

address 0x48 on its internal 2.5 V reference, a 2−pole 987 Hz Sallen−Key reconstruction filter, an OPA197 on a ferrite−filtered 5 V rail at a non−inverting DC gain of 1.32 that is a

2. Reconstruction filter and gain amplifier

R801, R802, C807 and C809 around U802 form the 987 Hz Sallen−Key filter; R803 and R804 set the gain 1.32 and C810 compensates the gain network. FB801 filters +5V to +5V_FILT for U802 (C801, C803, C806, C808); FB802 filters +3.3V to +3.3V_FILT for U801 (C802, C804, C805).



Filter and gain amplifier
C801, C806: Rail bypass; C803, C808: U802 V+ pin 5 bypass;
FB801: Rail ferrites
C809: Sallen–Key filter capacitors (C0G)
R803: Gain–set resistor, AMP_FB to GND
R805: AMP_VOUT pull–down, unpowered 0 V

GND

GND

AMP_FB

R803

10k

GND

Filter and gain amplifier
C801, C806: Rail bypass; C803, C808: U802 V+ pin 5 bypass;
FB801: Rail ferrites
C809: Sallen–Key filter capacitors (C0G)
R803: Gain–set resistor, AMP_FB to GND
R805: AMP_VOUT pull–down, unpowered 0 V

R801

20k

DAC_VOUT

DAC_VOUT_FILT_MID

Filter series resistor, first

R802

13k

DAC_VOUT_FILT_MID

DAC_VOUT_FILT

Filter series resistor, second

C807

10nF

DAC_VOUT_FILT_MID

AMP_VOUT

Sallen–Key filter capacitors (C0G)

R804

3.2k

AMP_FB

AMP_VOUT

Gain feedback, U802 (0.1 %)

C810

10pF

AMP_FB

AMP_VOUT

Gain–network compensation

PLACE: Keep DAC_VOUT_FILT_MID and DAC_VOUT_FILT short and guarded by analog ground; R803, R804 and C810 tight to U802 pins 1 and 4.

PLACE: Pull the ground pour back from under AMP_FB: C810 compensates about 8 pF of input capacitance and plane capacitance there changes it.

PLACE: C803 and C808 (100 nF) at U802 pin 5 with the return at pin 2; C805 (100 nF) at U801 pin 1 with the return at pin 4; the 1 uF and 10 uF parts beside their ferrites.

ROUTE: DAC_VOUT, AMP_VOUT and VREFIO deserve their own netclass rather than Default.

ROUTE: +5V and +3.3V arrive at FB801 and FB802 pad 1 (PWR_5V_LOCAL and PWR_3V3_LOCAL vias, convention 1); the filtered rails stay inside the block.

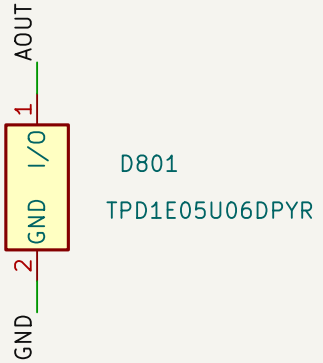
he filter's active element, a /2 output divider, a 249 ohm series output resistor, an ESD clamp and a separately isolated monitor tap.

3. Output divider, series resistor and ESD clamp

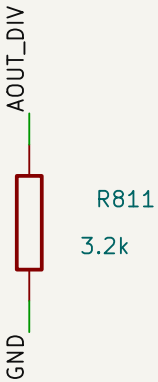
R807 and R811 halve AMP_VOUT to AOUT_DIV; R809 delivers AOUT with D801 clamping it; R810 isolates the AOUT_MON tap; R805 defines AMP_VOUT at 0 V unpowered; C812 shunts pickup on the midpoint.

/2 output divider top (0.1 %)

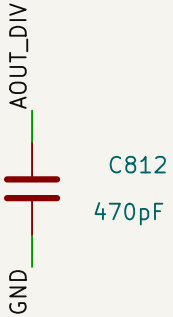
Series output resistor



ESD clamp on AOUT



/2 output divider bottom (0.1 %)



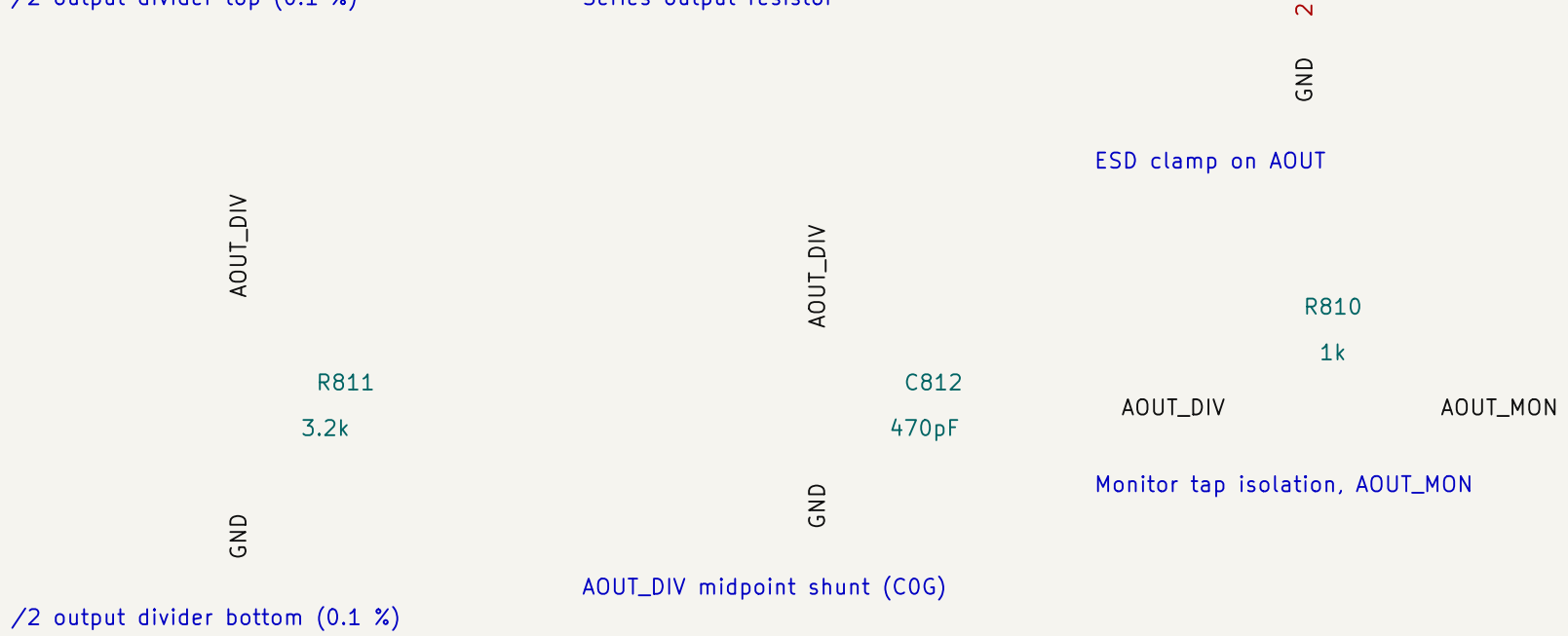
AOUT_DIV midpoint shunt (C0G)

Monitor tap isolation, AOUT_MON

PLACE: Place the block at the connector: D801's ground via must land on the connector ground pin, or connection inductance dominates its clamping.

PLACE: C812 at AOUT_DIV with a short return; R807 and R811 side by side (0.1 %, 25 ppm pair).

ROUTE: AOUT from R809 to the connector pin that carries D801; AOUT_MON through R810 to its own via; keep the two apart.



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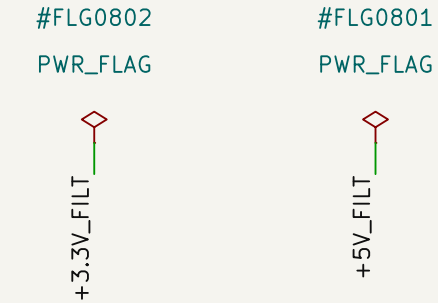
ROUTE: AOUT from R809 to the connector pin that carries D801; AOUT_MON through R810 to its own via; keep the two apart.

4. Power drive declarations

These nets have an explicit ERC power source declaration.



INTERFACES

Amplifier supply, a regulated 5.0 V rail in the same switched domain, through FB801 to +5V_FILT (U802 V+, 4.5 V minimum).

DAC supply, the switched 3.3 V domain, through FB802 to +3.3V_FILT (U801 VDD); must be the switched rail or the DAC's input clamps back-power the domain.

Analog return of the DAC, amplifier, filter, divider and ESD clamp; flagged once at board level, not here.

I2C clock to U801 pin 6 (SCLK/SCL); leaves as a single-pin net, the board fits the pull-up.

I2C data, U801 pin 8 (SDIN/SDA), address 0x48; leaves as a single-pin net, the board fits the pull-up.

Delivered output, 0–1.650 V from a 1.849 kohm source (R809 plus the divider); needs a >= 1 Mohm load; ESD-clamped by D801; any single fault is bounded to 2.55 V.

Monitor tap of AOUT_DIV through R810 (1 k): the same 0–1.650 V as AOUT, isolated from it; an instrument reads here.

AOUT AOUT

Delivered output, 0–1.650 V from a 1.849 kohm source (R809 plus the divider); needs a >= 1 Mohm load; ESD-clamped by D801; any single fault is bounded to 2.55 V.

AOUT_MON AOUT_MON

Monitor tap of AOUT_DIV through R810 (1 k): the same 0–1.650 V as AOUT, isolated from it; an instrument reads here.

OPERATION

Signal path: U801 VOUT (pin 2, 0–2.5 V on the internal reference) -> R801 (20 k) -> DAC_VOUT_FILT_MID -> R802 (13 k) -> DAC_VOUT_FILT -> U802 + (pin 3). C807 (10 nF, midpoint to AMP_VOUT) and C809 (10 nF to GND) make a Sallen-Key low-pass with U802 as the active element: f0 987 Hz, Q 0.61, group delay 266 us, matched to the torque block's 263 us. R804 (3.2 k) over R803 (10 k) sets the gain 1 + 3.2/10 = 1.32, so AMP_VOUT is 0–3.300 V; R807 and R811 (3.2 k each) halve it to AOUT_DIV, 0–1.650 V (LSB 25.2 uV); R809 (249 ohm) delivers AOUT and R810 (1 k) taps AOUT_MON.

I2C, address 0x48: R808 (1 k to +3.3V_FILT) latches SPI2C for I2C at power-up; R806 (1 k to GND) sets A0 to 0x48 (the brake block takes 0x49). A0 is a four-state pin re-sampled during the first byte of every frame, so a floating A0 gives an address that changes between frames: never lift R806 without re-wiring it in the same operation. The block owns no bus termination; SCL and SDA leave as single-pin nets and the board fits one 2.2 k pull-up pair per bus segment, the DAC-side pair on the switched 3.3 V rail.

Firmware writes GAIN (4h) = 0x0101 before any DATA write. At a 3.3 V VDD the reset default is out of spec against the 2.5 V reference, so the reference alarm holds VOUT at 0 V until that write lands, and STATUS reports it over I2C. The measured output floor is 4.5 mV at AMP_VOUT, 2.25 mV at AOUT: map the signal range above it and keep 0 V for unpowered or faulted.

Loading and fault bounds: AOUT needs a >= 1 Mohm load (−0.185 % of gain into 1 Mohm, −1.82 % into 100 kohm). R809 bounds a short to ground at 6.6 mA; the /2 divider bounds any single fault, including U802's output stuck at its 5 V rail, to 2.55 V at the connector. D801 (TPD1E05U06, 5.5 V working, +−12 kV contact) clamps ESD transients only, not a DC fault. AOUT and AOUT_MON both tap AOUT_DIV and are electrically interchangeable: verify on the netlist that D801 shares its net with the connector pin.

Supplies: +5V from a regulated 5.0 V rail (U802 needs 4.5 V) and +3.3V from the switched 3.3 V rail, both in the same switched domain so the output goes dark with its data source; FB801 and FB802 filter them to +5V_FILT and +3.3V_FILT, each carrying a PWR_FLAG. Two instances need separate sheets or DAC_A0, SPI2C and the filtered rails merge.

C807, C809 and C812 are C0G: class-2 dielectric is piezoelectric and this board is coupled to a stepper and a hand-driven joystick. Retune the filter by scaling R801 and R802 together; do not raise f0 and do not use C810 for band limiting. R805 (100 k) stays on AMP_VOUT, not on the midpoint, where it would become part of the ratio.

DESIGN NOTES

GAIN register (4h) reset = 0x0001 = the 0–5 V span. Write 0x0101 (REF-DIV=1, BUFF-GAIN=1) -> 0–2.5 V at the DAC, 0–3.300 V at AMP_VOUT, 0–1.650 V at AOUT. Do this before any DAC data write.
At a 3.3 V VDD the reset default is out of spec against the 2.5 V internal reference, so the reference alarm shuts the reference buffer down and forces VOUT to 0 V until that write lands; read that 0 V as unpowered or faulted, never as a valid end-of-travel angle. Do not use REF-DIV=0 to recover the 0–5 V span.

A0=GND 0x48

2-POLE SALLEN-KEY RECONSTRUCTION / ANTI-ALIAS FILTER: R801 (20.0 k), R802 (13.0 k), C807 and C809 (10 nF each) around U802. f0 = 1/(2 pi C sqrt(R801 x R802)) with C807 = C809 = C; 1/Q = 1/sqrt(a) + sqrt(a) x (2 − K), a = R801/R802 = 1.538, K = 1.32. As built: f0 = 987 Hz, Q = 0.606, −3 dB at 827 Hz, −52.3 dB at 20 kHz, 266 us group delay.
WHY IT EXISTS: the acquisition (OneBox, AD7616) samples at a fixed 30.3 kHz behind only a 1st-order 39 kHz filter, so it does not anti-alias. The TMC5130A chopper runs 16–30 kHz (the datasheet-recommended range) and every value in that range folds into 0–15 kHz, where it is indistinguishable from joystick motion. This filter is the only band limit in the chain. It also cuts the DAC code-change glitch from 9.9 mV to 14 uV; the OneBox LSB is 152.6 uV on the +/−5 V range.
TO RETUNE: scale R801 and R802 by the SAME factor. Q depends only on their ratio, so the shape is preserved and only f0 moves. Do not change C. Ladder, R801/R802: f0, rejection at 20 kHz, group delay:
- 64.9k/42.2k: 304 Hz, −72.7 dB, 864 us.
- 39.2k/25.5k: 503 Hz, −64.0 dB, 522 us.
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- 3.92k/2.55k: 5.03 kHz, −24.0 dB, 52 us.
- 2.00k/1.30k: 9.87 kHz, −13.2 dB, 27 us (chopper barely attenuated).

SINGLE-POLE FALLBACK (same pads): R801 = 0 R jumper, C807 = DNP, R802 = 15.0 k, C809 = 10 nF -> 1.061 kHz, one pole, −25.5 dB at 20 kHz, 150 us. C807 MUST be DNP in this configuration: with R801 shorted it would hang 10 nF from the DAC output to the op-amp output.
CONSTRAINTS. C0G ONLY (TI DACx0501 datasheet 9.2.2.6): class-2 dielectric is piezoelectric and this board sits next to a stepper; the series R can only bleed self-generated charge with time constant R x C, which is fixed by f0, so it cannot be filtered away.
C807 and C809 must be the SAME value and ideally the same reel. Q depends on C807/C809 = 1; matched capacitors make Q immune to capacitor tolerance.
R801 and R802 carry no DC current (op-amp Ib = 10 pA), so the DC gain is set ENTIRELY by R803 and R804. 1 % here is plenty; do not "upgrade" to 0.1 %.
Keep C810 = 10 pF. Its pole is at 4.97 MHz and it rolls K toward 1.0 at HF, which lowers Q up there: stabilizing, not destabilizing.
Do not put a shunt capacitor on the connector side of R809. One large enough to matter there (640 nF for 1 kHz) drives U802 into its +/−65 mA limit on every step, and its corner would track the researcher's cable capacitance.
Group delay is a latency you must MEASURE and report, not assume.
The Sallen-Key stopband floors out above about 1 MHz as the op-amp output impedance rises and C807 stops bootstrapping. Irrelevant at 16–30 kHz.
LAYOUT: keep DAC_VOUT_FILT_MID and DAC_VOUT_FILT short and surrounded by analog GND.

DESIGN CONTRACT

Single-channel buffered 0-1.650 V precision analog voltage output, safe on a Neuropixels OneBox ADC channel or an unprotected 3.3 V MCU pin: a DAC80501ZDGSR at 3.3 V on I2C at address 0x48 on its internal 2.5 V reference, a 2-pole 987 Hz Sallen-Key reconstruction filter, an OPA197 on a ferrite-filtered 5 V rail at a non-inverting DC gain of 1.32 that is also the filter's active element, a /2 output divider, a 249 ohm series output resistor, an ESD clamp and a separately isolated monitor tap. AMP_VOUT full scale is 2.5 V x (1 + 3.2k/10k) = 3.300 V and AOUT is half of it, 1.650 V, LSB 25.2 uV. Built for the mouse-joystick-pcb encoder angle output, but THE CONNECTOR DELIBERATELY LIVES OUTSIDE THE BLOCK so one block serves any housing. The full derivation, values, retune ladder, layout rules and accuracy budget are in kicad-libs docs/analog-output-design.md; this note carries only what breaks silently without it. Designators are not stable (KiCad auto-annotation orders by sheet position), so everything below is named by net.

1. I2C, NOT SPI, AND THE ADDRESS IS ONE RESISTOR. SPI2C is strapped to +3.3V_FILT through 1k for I2C mode; A0 is strapped to GND through 1k for 0x48, and brake_current_sink_0_49ma_dac80501 takes 0x49. A0 is a FOUR-STATE pin (AGND 0x48, VDD 0x49, SDA 0x4A, SCL 0x4B), so a rail strap reaches only the first two. A0 is re-sampled during the first byte of EVERY frame, so a floating A0 gives an address that changes between frames rather than a clean failure; never lift that resistor without re-wiring it in the same operation.
2. THIS BLOCK OWNS NO BUS TERMINATIONS and must not gain any. An earlier revision advertised three 10k SPI idle resistors as a feature; they are DELETED, because two DAC blocks on one bus would put 5k to GND on SDA and SCL and idle the bus at 2.29 V against a 2.2k pull-up, on top of the DAC's 1.62 V VIH minimum. SCL and SDA leave as single-pin nets. The board fits ONE 2.2k pull-up pair PER BUS SEGMENT: the DAC-side pair on the SWITCHED 3.3 V rail, because an always-on pull-up reaching a DAC whose VDD is at 0 V exceeds the VDD+0.3 V digital-input absolute maximum and back-feeds +3.3V_FILT through the internal clamps; the MCU-side pair on the ALWAYS-ON rail, because the SN74CB3Q3245 is open by default.
3. AOUT AND AOUT_MON ARE TWO DIFFERENT PORTS AND CROSSING THEM IS A DEFECT ERC CANNOT CATCH. Both tap AOUT_DIV, the divider midpoint, so the monitor and the connector read the same voltage. AOUT is the delivered output and carries the 249 ohm source resistor and the ESD clamp; AOUT_MON is a 1k instrument tap. Both are validly driven either way round, so verify on the netlist that the clamp shares a net with the connector pin. Backwards leaves the human-accessible connector with NO ESD protection. This happened once, on mouse-joystick-pcb, 2026-08-27.
4. THE 100k OUTPUT PULL-DOWN STAYS ON AMP_VOUT, upstream of the /2 divider. It defines 0 V when the block is unpowered; on the midpoint it would parallel the bottom leg for about -1.6% of ratio, and it is a 1% 100ppm/C thick film against the divider's 0.1% 25ppm/C pair. General rule: anything whose job is to define a node when the amplifier is dead belongs on the AMP side of a divider; anything in parallel with a divider leg becomes part of the RATIO.
5. AOUT IS 0-1.650 V FROM A 1.849 kohm SOURCE AND NEEDS A >=1 Mohm LOAD. The source is the 249 ohm series resistor PLUS the divider's 1.6 kohm, not 249 ohm alone: against the OneBox AD7616-P's 1 Mohm that is -0.185% of gain, systematic and absorbed by per-board calibration, but a 100 kohm load costs -1.82% and a 50 ohm terminated input reads a fraction of the correct value. The 249 ohm still bounds a short of AOUT to ground at 6.6 mA and 11 mW inside a 62.5 mW 0402. The /2 divider is what bounds a single fault, including the amp's own output stage shorted to its 5 V rail, to 2.55 V on a connector pin, inside an STM32F405's 4.0 V absolute maximum. That bound is a property of the copper, not of a register write. The ESD clamp is a transient device and does NOT bound a DC fault.
6. THE FILTER IS NOT OPTIONAL, ITS CAPACITORS MUST BE C0G from one reel, AND SO MUST THE 470 pF DIVIDER MIDPOINT SHUNT. Class-2 dielectric is piezoelectric, this board is coupled to a stepper and a hand-driven joystick, and on the midpoint that pickup becomes signal. Retune by scaling BOTH series resistors by the same factor and leaving the capacitors alone: Q depends only on their ratio. Do not raise f0 to buy passband: rejection falls as (f0/20kHz)^2 and the chopper is the whole point. The 266 us group delay is a latency to MEASURE and report, and it is deliberately matched to torque_bridge_0_3v3_ina821's 263 us. The midpoint shunt is 470 pF because it adds only 0.75 us against that budget; the brake block's 10 nF would add 16 us and land the corner a decade above the 987 Hz filter.
7. FIRMWARE MUST WRITE GAIN (4h) = 0x0101 BEFORE ANY DATA WRITE, and at 3.3 V that is a SAFETY PROPERTY rather than a hazard. The reset default 0x0001 is out of spec against the 2.5 V internal reference at a 3.3 V VDD, so the reference alarm holds the output at 0 V until that write lands. This block used to run its DAC at 5 V, where the same default commanded 5 V x 1.32 and the amp clipped near 4.85 V into whatever was on the connector. Over I2C the alarm is also READABLE in STATUS, which is why this block is on I2C at all. Do not use REF-DIV=0 to recover the old span.
8. THE OUTPUT FLOOR IS 4.5 mV MEASURED, 2.25 mV AFTER THE DIVIDER. Map the valid signal range to start above it and reserve true 0 V as the out-of-band unhomed, faulted or unpowered level. That leaves only about 2 mV between a firmware-signalled fault and a dead output section, so STATUS, not the analog level, is the primary discriminator.
9. BIND +3.3V AND +5V TO THE SAME SWITCHED DOMAIN. Feed +5V from a REGULATED 5.0 V rail, never a diode-ORed host rail, so the output goes dark with its data source instead of holding a stale angle. The DAC's +3.3V MUST be the switched rail or it back-powers the switched domain through the DAC's input clamps.
10. PWR_FLAG ON BOTH +3.3V_FILT AND +5V_FILT is required: there are two ferrites and each breaks driver propagation. GND is flagged once at board level, not here.
11. TWO INSTANCES NEED SEPARATE SHEETS or their local nets merge, and DAC_A0 merging would silently put both copies on 0x48. A twin-axis board needs the SDA and SCL strap states, 0x4A and 0x4B, which a rail strap cannot reach.

5 V quadrature encoder input | SN74LVC2G17 Schmitt buffer, RC conditioning, instrument taps

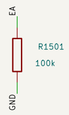
Single-ended 5 V quadrature encoder input: per-channel series/RC conditioning plus an SN74LVC2G17 dual Schmitt-trigger buffer that translates an encoder's 5 V push-pull A/B outputs into clean 3.3 V logic.

Matching net labels are connected. Group order explains function: PCB placement priorities are stated below.

1. Channel A input conditioning

EA passes through R1503 to EA_FILT; R1501 pulls the harness side to GND, C1502 shunts the filtered node to GND (72 kHz corner with R1503).

Series limit, RC 72 kHz with C1502



Pull-down, harness side, 100 k

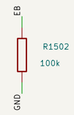
PLACE: R1503 at the block's input edge near the harness connector; C1502 at U1501A pin 1 with a short return.

ROUTE: Keep EA and EB together with a ground reference between them and away from motor bridge outputs; EA_FILT is a short local node.

2. Channel B input conditioning

EB passes through R1504 to EB_FILT; R1502 pulls the harness side to GND, C1503 shunts the filtered node to GND.

Series limit, RC 72 kHz with C1503



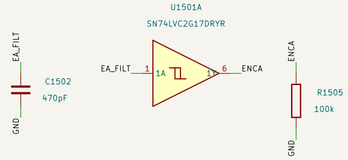
Pull-down, harness side, 100 k

PLACE: R1504 at the input edge beside R1503; C1503 at U1501B pin 3 with a short return.

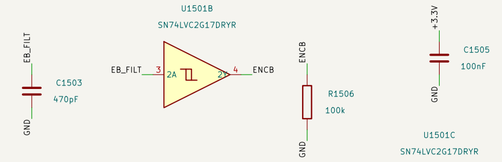
ROUTE: Same as channel A: match the two channels' routing so their delays stay equal.

3. Schmitt buffer and VCC bypass

U1501A squares and translates both channels to 3.3 V logic; C1505 bypasses VCC (pin 5) to GND (pin 2).



Unit 1: Dual Schmitt buffer, 5 V in to 3.3 V out
R1505: Pull-down, buffer output, 100 k
C1502: RC filter shunt at Schmitt input 1A, pin 1



Unit 2: Dual Schmitt buffer, 5 V in to 3.3 V out
R1506: Pull-down, buffer output, 100 k
C1503: RC filter shunt at Schmitt input 2A, pin 3

Power unit
C1505: VCC pin 5 bypass, 100 nF

PLACE: Place C1505 hard against U1501C pin 5 with its GND end at pin 2.

ROUTE: Short VCC and GND stubs; the outputs 1Y and 2Y leave toward ENCA and ENCB.

4. Output pull-downs and instrument taps

R1505 and R1506 hold ENCA and ENCB low when the buffer is unpowered; R1507 and R1508 tap them to ENCA_INST and ENCB_INST.

Instrument tap, 100 R, to ENCA_INST

Instrument tap, 100 R, to ENCB_INST

PLACE: Place the pull-downs near the buffer outputs and the taps where the instrument nets leave the block.

ROUTE: ENCA_INST and ENCB_INST carry the INSTRUMENT class; keep them off the ENCA and ENCB paths to the controller.

5. Encoder supply bypass

C1501 (4.7 uF) and C1504 (100 nF) bypass VENC, the encoder supply the board passes to the harness.

VENC bulk bypass, 4.7 uF VENC bypass, 100 nF

PLACE: Place both where VENC leaves toward the harness connector, C1504 closest to it.

ROUTE: VENC is on the Default class here; the board classes it with the encoder's supply.

INTERFACES

VENC — VENC

Encoder supply passed through to the harness; bypassed here by C1501 and C1504.

+3.3V — +3.3V

Buffer supply, U1501A VCC (pin 5); 3.3 V logic domain of the outputs; bypassed by C1505.

GND — GND

Return for the buffer, both RC shunts, all pull-downs and the supply bypass.

EA — EA

Encoder channel A, raw 5 V push-pull from the harness; R1501 to GND, R1503 in series.

EB — EB

Encoder channel B, raw 5 V push-pull from the harness; R1502 to GND, R1504 in series.

ENCA — ENCA

Channel A as 3.3 V logic from U1501A 1Y (pin 6); R1505 holds it low when unpowered.

ENCB — ENCB

Channel B as 3.3 V logic from U1501A 2Y (pin 4); R1506 holds it low when unpowered.

ENCA_INST — ENCA_INST

Instrument tap of ENCA through R1507 (100 ohm), INSTRUMENT class.

ENCB_INST — ENCB_INST

Instrument tap of ENCB through R1508 (100 ohm), INSTRUMENT class.

INTERNAL NETS

EA_FILT: Filtered channel A at the Schmitt input 1A: R1503 and C1502 form the 72 kHz corner.

EB_FILT: Filtered channel B at the Schmitt input 2A: R1504 and C1503 form the 72 kHz corner.

OPERATION

Signal path per channel: EA -> R1503 (4.7 k) -> EA_FILT -> U1501A 1A (pin 1) -> 1Y (pin 6) = ENCA; EB -> R1504 -> EB_FILT -> 2A (pin 3) -> 2Y (pin 4) = ENCB. A/B only; an index channel needs a second buffer.

Each series resistor with its 470 pF shunt (C1502, C1503) is a low-pass of tau = 4.7 k x 470 pF = 2.2 us, corner about 72 kHz; it removes harness noise and slows the edge into a Schmitt input, which has no slew-rate limit.

U1501A (SN74LVC2G17, 1.65 to 5.5 V supply) at 3.3 V: VT+ 1.3 to 2.0 V, VT- 0.8 to 1.3 V (facts at 3 V), 0.4 V minimum hysteresis; inputs are 5.5 V tolerant with no clamp to VCC, so the 5 V encoder drives them directly and Ioff (10 uA max) keeps the outputs high-impedance when +3.3V is down.

R1503 and R1504 are also the protection: a harness short to a 36 V rail is bounded to about 7.7 mA. R1501 and R1502 (100 k) define the inputs when the harness is unplugged; R1505 and R1506 (100 k) hold ENCA and ENCB low when the buffer is unpowered, so a downstream instrument never sees a floating input.

R1507 and R1508 (100 ohm) are the instrument taps to ENCA_INST and ENCB_INST (convention 14: the block owns its outputs). C1501 (4.7 uF) and C1504 (100 nF) bypass the encoder supply VENC near the harness; C1505 (100 nF) bypasses VCC at pin 5.

The placing board provides VENC and +3.3V from the same switched domain as the encoder consumer, the GND return and the harness connector; it decides ENCN handling when no index channel exists.

DESIGN CONTRACT

Single-ended 5 V quadrature encoder input: per-channel series/RC conditioning plus an SN74LVC2G17 dual Schmitt-trigger buffer that translates an encoder's 5 V push-pull A/B outputs into clean 3.3 V logic. The connector deliberately lives outside the block, the same way differential_encoder_receiver is built, so one block serves screw-terminal, IDC, JST or Molex harnesses and the parent picks the housing to suit the machine. Bring the raw encoder channels in on EA and EB and take conditioned logic out on ENCA and ENCB; ENCA_INST and ENCB_INST are their instrument taps. Use this for TTL/push-pull encoders; use differential_encoder_receiver instead for RS-422 A+/A-/B+/B- encoders.
The Schmitt input is the point of the block: a typical 5 V encoder rises in about 100 ns over a 4 V swing, roughly 25 ns/V, which violates the 8 ns/V input transition rate limit of an ordinary LVC buffer and would let noise on the slow edge double-clock the quadrature counter into permanent, silent position error. The 2G17 has no such limit and 0.4 V minimum hysteresis at 3 V, and it closes against the encoder's guaranteed worst case with 400 mV to spare on both rails: VOH >= 2.4 V versus VT+ <= 2.0 V, VOL <= 0.4 V versus VT- >= 0.8 V. Do not substitute a resistive divider into a 3.3 V input: dividing the encoder's guaranteed 2.4 V VOH by 0.66 gives 1.58 V, below the 2.31 V VINHI of a 3.3 V VCC_IO TMC5130A input, and loading the output makes it worse.
The 4.7 kohm series resistors R1503/R1504 are the protection element and the reason the block tolerates a field-wired harness: they bound a short to a 36 V rail to about 7 mA, so a miswire kills a 0.19 USD buffer instead of the motor driver. The 100 kohm resistors R1501/R1502 sit on the harness side of those series resistors rather than after them, so they define the buffer input when the harness is unplugged without forming a divider that would eat VIH margin: R1505/R1506 on the outputs cover Ioff high-Z when the buffer's supply is down, so an always-on downstream instrumentation buffer never sees a floating input.
The VENC and +3.3V ports are intentionally generic so a parent can bind them to whatever it calls its rails, but the electrical requirement is not generic: on any board where the encoder's consumer can be powered down, bind both to that board's SWITCHED domain, so the encoder, this buffer and the consumer rise and fall together. Rail sequencing between the two is a non-issue: inputs are rated 0 to 5.5 V at any valid VCC with 6.5 V absolute maximum and no clamp diode to VCC, and Ioff disables the outputs when the part is unpowered.
Size C1502/C1503 for a corner >= 10x CPR*RPM/60: 27 pF gives 1.25 MHz, 470 pF gives 72 kHz for a slow axis that needs more rejection.
This block covers A/B only. If your encoder has an index channel, add a second SN74LVC2G17 with its spare input tied to GND; if it does not, the consuming controller's index pin still needs an explicit tie: the TMC5130A datasheet requires ENCN be pulled to GND or VCC_IO when unused.
For layout: C1501 and C1504 decouple the encoder supply VENC and want to sit as close to the parent's encoder connector as placement allows; R1503 and R1504 at the block's input edge, C1502 at U1501A pin 1 and C1503 at pin 3 with short returns; C1505 hard against U1501C pin 5; route the A/B pair with a ground reference between them and well away from motor bridge outputs.

Circuit and PCB layout guidance
Migrated from the saved library sheet; circuit and PCB unchanged
Orb Weaver

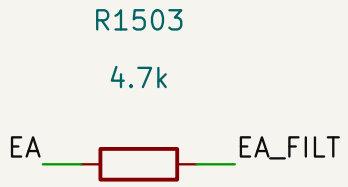
Sheet: /motor_encoder_switch/quadrature_encoder_input_5v_sn74lvc2g17/
File: quadrature_encoder_input_5v_sn74lvc2g17.kicad_sch

Title: 5 V quadrature encoder input

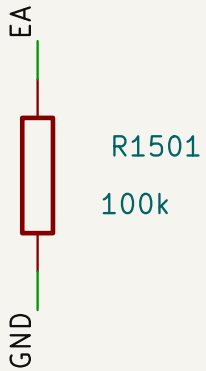
Size: A2	Date: 2026-10-05	**Rev: Source migration 1**
KiCad E.D.A. 10.0.6		Id: 15/20

1. Channel A input conditioning

EA passes through R1503 to EA_FILT; R1501 pulls the harness side to GND, C1502 shunts the filtered node to GND (72 kHz corner with R1503).



Series limit, RC 72 kHz with C1502



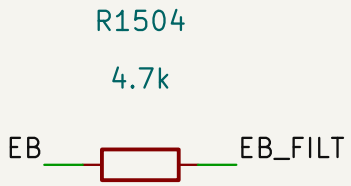
Pull−down, harness side, 100 k

PLACE: R1503 at the block's input edge near the harness connector; C1502 at U1501A pin 1 with a short return.

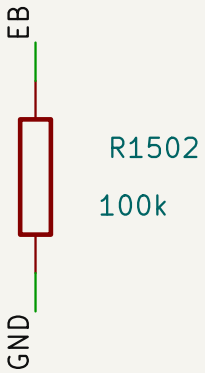
ROUTE: Keep EA and EB together with a ground reference between them and away from motor bridge outputs; EA_FILT is a short local node.

2. Channel B input conditioning

EB passes through R1504 to EB_FILT; R1502 pulls the harness side to GND, C1503 shunts the filtered node to GND.



Series limit, RC 72 kHz with C1503



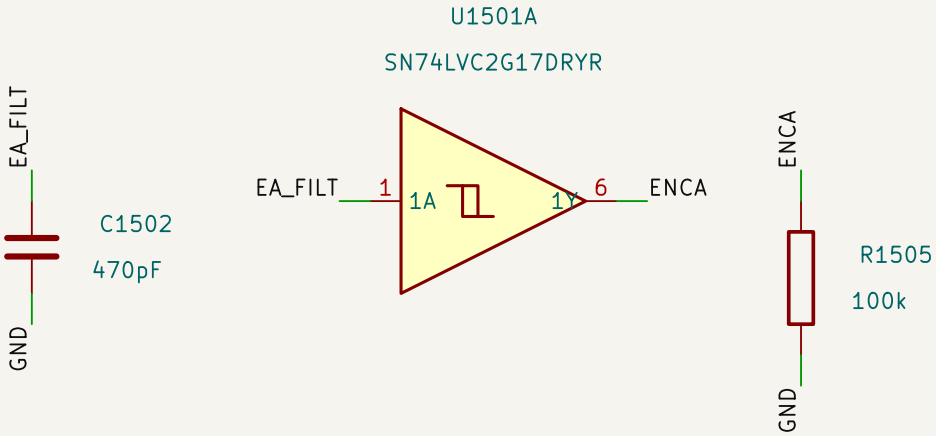
Pull-down, harness side, 100 k

PLACE: R1504 at the input edge beside R1503; C1503 at U1501B pin 3 with a short return.

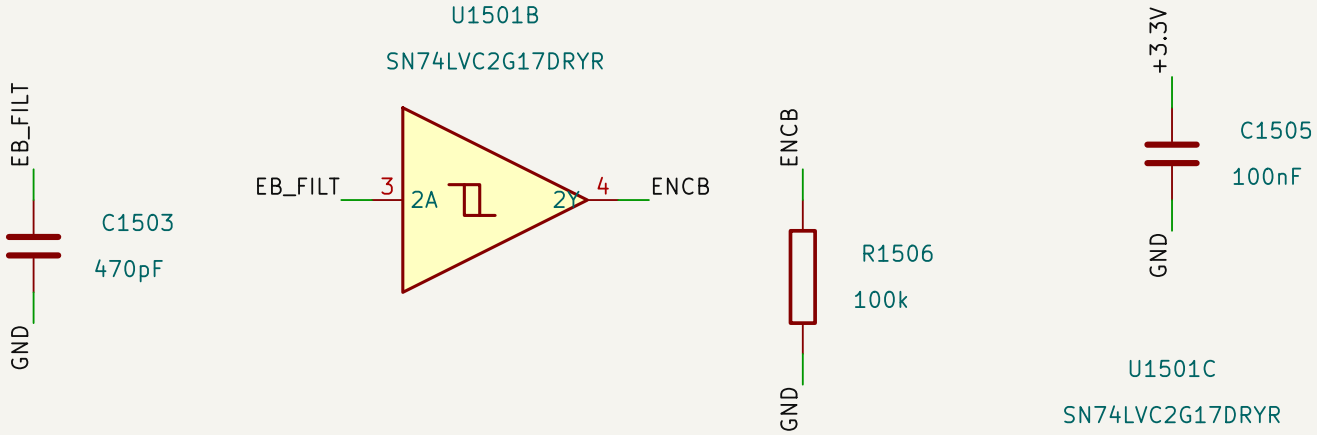
ROUTE: Same as channel A; match the two channels' routing so their delays stay equal.

3. Schmitt buffer and VCC bypass

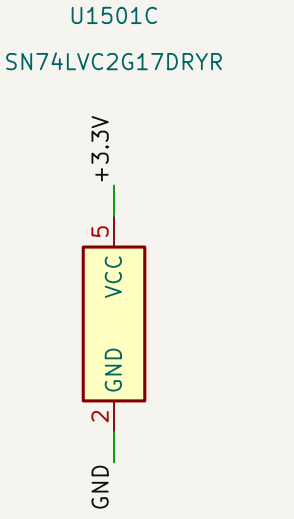
U1501A squares and translates both channels to 3.3 V logic; C1505 bypasses VCC (pin 5) to GND (pin 2).



Unit 1: Dual Schmitt buffer, 5 V in to 3.3 V out
R1505: Pull–down, buffer output, 100 k
C1502: RC filter shunt at Schmitt input 1A, pin 1



Unit 2: Dual Schmitt buffer, 5 V in to 3.3 V out
R1506: Pull–down, buffer output, 100 k
C1503: RC filter shunt at Schmitt input 2A, pin 3



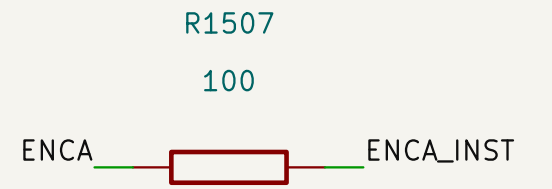
Power unit
C1505: VCC pin 5 bypass, 100 nF

PLACE: Place C1505 hard against U1501C pin 5 with its GND end at pin 2.

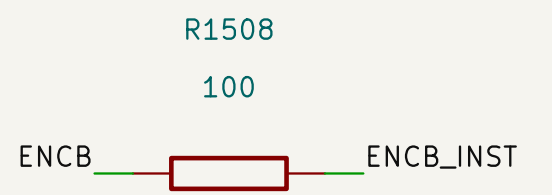
ROUTE: Short VCC and GND stubs; the outputs 1Y and 2Y leave toward ENCA and ENCB.

4. Output pull-downs and instrument taps

R1505 and R1506 hold ENCA and ENCB low when the buffer is unpowered; R1507 and R1508 tap them to ENCA_INST and ENCB_INST.



Instrument tap, 100 R, to ENCA_INST



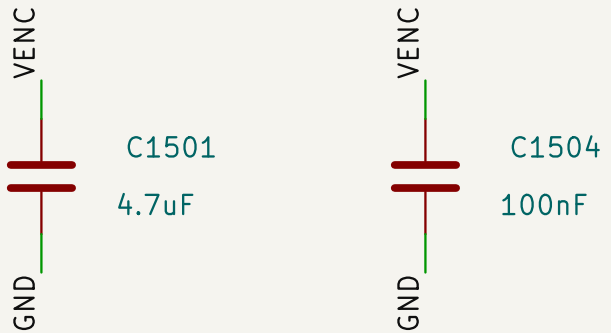
Instrument tap, 100 R, to ENCB_INST

PLACE: Place the pull-downs near the buffer outputs and the taps where the instrument nets leave the block.

ROUTE: ENCA_INST and ENCB_INST carry the INSTRUMENT class; keep them off the ENCA and ENCB paths to the controller.

5. Encoder supply bypass

C1501 (4.7 uF) and C1504 (100 nF) bypass VENC, the encoder supply the board passes to the harness.



VENC bulk bypass, 4.7 uF

VENC bypass, 100 nF

PLACE: Place both where VENC leaves toward the harness connector, C1504 closest to it.

ROUTE: VENC is on the Default class here; the board classes it with the encoder's supply.

INTERFACES

Encoder supply passed through to the harness; bypassed here by C1501 and C1504.

Buffer supply, U1501A VCC (pin 5); 3.3 V logic domain of the outputs; bypassed by C1505.

Return for the buffer, both RC shunts, all pull-downs and the supply bypass.

Encoder channel A, raw 5 V push-pull from the harness; R1501 to GND, R1503 in series.

Encoder channel B, raw 5 V push-pull from the harness; R1502 to GND, R1504 in series.

Channel A as 3.3 V logic from U1501A 1Y (pin 6); R1505 holds it low when unpowered.

Channel B as 3.3 V logic from U1501A 2Y (pin 4); R1506 holds it low when unpowered.

Instrument tap of ENCA through R1507 (100 ohm), INSTRUMENT class.

Instrument tap of ENCB through R1508 (100 ohm), INSTRUMENT class.

INTERNAL NETS

EA_FILT: Filtered channel A at the Schmitt input 1A; R1503 and C1502 form the 72 kHz corner.

EB_FILT: Filtered channel B at the Schmitt input 2A; R1504 and C1503 form the 72 kHz corner.

OPERATION

Signal path per channel: EA –> R1503 (4.7 k) –> EA_FILT –> U1501A 1A (pin 1) –> 1Y (pin 6) = ENCA; EB –> R1504 –> EB_FILT –> 2A (pin 3) –> 2Y (pin 4) = ENCB. A/B only: an index channel needs a second buffer.

Each series resistor with its 470 pF shunt (C1502, C1503) is a low–pass of tau = 4.7 k x 470 pF = 2.2 us, corner about 72 kHz; it removes harness noise and slows the edge into a Schmitt input, which has no slew–rate limit.

U1501A (SN74LVC2G17, 1.65 to 5.5 V supply) at 3.3 V: VT+ 1.3 to 2.0 V, VT– 0.8 to 1.3 V (facts at 3 V), 0.4 V minimum hysteresis; inputs are 5.5 V tolerant with no clamp to VCC, so the 5 V encoder drives them directly and Ioff (10 uA max) keeps the outputs high–impedance when +3.3V is down.

R1503 and R1504 are also the protection: a harness short to a 36 V rail is bounded to about 7.7 mA. R1501 and R1502 (100 k) define the inputs when the harness is unplugged; R1505 and R1506 (100 k) hold ENCA and ENCB low when the buffer is unpowered, so a downstream instrument never sees a floating input.

R1507 and R1508 (100 ohm) are the instrument taps to ENCA_INST and ENCB_INST (convention 14: the block owns its outputs). C1501 (4.7 uF) and C1504 (100 nF) bypass the encoder supply VENC near the harness; C1505 (100 nF) bypasses VCC at pin 5.

The placing board provides VENC and +3.3V from the same switched domain as the encoder consumer, the GND return and the harness connector; it decides ENCN handling when no index channel exists.

DESIGN CONTRACT

Single–ended 5 V quadrature encoder input: per–channel series/RC conditioning plus an SN74LVC2G17 dual Schmitt–trigger buffer that translates an encoder's 5 V push–pull A/B outputs into clean 3.3 V logic. The connector deliberately lives outside the block, the same way differential_encoder_receiver is built, so one block serves screw–terminal, IDC, JST or Molex harnesses and the parent picks the housing to suit the machine. Bring the raw encoder channels in on EA and EB and take conditioned logic out on ENCA and ENCB; ENCA_INST and ENCB_INST are their instrument taps. Use this for TTL/push–pull encoders; use differential_encoder_receiver instead for RS–422 A+/A–/B+/B– encoders.
The Schmitt input is the point of the block: a typical 5 V encoder rises in about 100 ns over a 4 V swing, roughly 25 ns/V, which violates the 8 ns/V input transition rate limit of an ordinary LVC buffer and would let noise on the slow edge double–clock the quadrature counter into permanent, silent position error. The 2G17 has no such limit and 0.4 V minimum hysteresis at 3 V, and it closes against the encoder's guaranteed worst case with 400 mV to spare on both rails: VOH >= 2.4 V versus VT+ <= 2.0 V, VOL <= 0.4 V versus VT– >= 0.8 V. Do not substitute a resistive divider into a 3.3 V input: dividing the encoder's guaranteed 2.4 V VOH by 0.66 gives 1.58 V, below the 2.31 V VINHI of a 3.3 V VCC_IO TMC5130A input, and loading the output makes it worse.
The 4.7 kohm series resistors R1503/R1504 are the protection element and the reason the block tolerates a field–wired harness: they bound a short to a 36 V rail to about 7 mA, so a miswire kills a 0.19 USD buffer instead of the motor driver. The 100 kohm resistors R1501/R1502 sit on the harness side of those series resistors rather than after them, so they define the buffer input when the harness is unplugged without forming a divider that would eat VIH margin; R1505/R1506 on the outputs cover Ioff high–Z when the buffer's supply is down, so an always–on downstream instrumentation buffer never sees a floating input.
The VENC and +3.3V ports are intentionally generic so a parent can bind them to whatever it calls its rails, but the electrical requirement is not generic: on any board where the encoder's consumer can be powered down, bind both to that board's SWITCHED domain, so the encoder, this buffer and the consumer rise and fall together. Rail sequencing between the two is a non–issue: inputs are rated 0 to 5.5 V at any valid VCC with 6.5 V absolute maximum and no clamp diode to VCC, and Ioff disables the outputs when the part is unpowered.
Size C1502/C1503 for a corner >= 10x CPR*RPM/60; 27 pF gives 1.25 MHz, 470 pF gives 72 kHz for a slow axis that needs more rejection.
This block covers A/B only. If your encoder has an index channel, add a second SN74LVC2G17 with its spare input tied to GND; if it does not, the consuming controller's index pin still needs an explicit tie: the TMC5130A datasheet requires ENCN be pulled to GND or VCC_IO when unused.
For layout: C1501 and C1504 decouple the encoder supply VENC and want to sit as close to the parent's encoder connector as placement allows; R1503 and R1504 at the block's input edge, C1502 at U1501A pin 1 and C1503 at pin 3 with short returns; C1505 hard against U1501C pin 5; route the A/B pair with a ground reference between them and well away from motor bridge outputs.

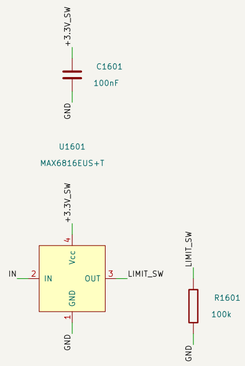
Debounced limit-switch input, vertical terminal | MAX6816, output pull-down, instrument tap

Debounced limit-switch input with its own 2-position 3.5 mm VERTICAL, top-entry pluggable screw terminal — Phoenix MCV 1.5/2-G-3.5, OW-CONN-TBH-1X02-3P5-VERT, on the local orb_weaver_tht copy of the MCV footprint — plus a MAX6816 single switch debouncer and local Vcc decoupling.

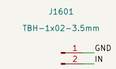
Matching net labels are connected. Group order explains function: PCB placement priorities are stated below.

1. Switch terminal and debouncer

J1601 brings the dry contact onto IN (pin 2) and GND (pin 1); U1601 debounces IN and drives LIMIT_SW from its push-pull OUT. C1601 (100 nF) bypasses Vcc (pin 4) to GND (pin 1).



Switch debouncer
C1601: Vcc bypass for U1601
R1601: Output pull-down for the unpowered state



Vertical switch terminal, pin 1
GND, pin 2 IN

PLACE: Keep U1601 next to J1601 so IN stays short; nothing else connects to IN. Leave the 4.75 mm inboard keepout of the vertical terminal free, and give the enclosure an aperture above it for the plug, the screw head and the wire loop.

PLACE: Place C1601 hard against pin 4 with a short return to pin 1.

ROUTE: The LIMIT_SW and GND runs share the corridor bounded by the IN pad on 0.5 mm centres: every track in the block is 0.3 mm, which leaves the LIMIT_SW-to-GND gap at exactly the 0.200 mm netclass rule. Move a run before widening it and re-run DRC after any change here.

ROUTE: +3.3V_SW has no reference-project class here (Default): the placing board classes the switched rail.

2. Output pull-down and instrument tap

R1601 (100 k) holds LIMIT_SW low while the debouncer is unpowered; R1602 (1 k) is the series tap from LIMIT_SW to LIMIT_SW_INST.

Instrument tap series resistor

PLACE: R1601 sits above U1601 with its LIMIT_SW pad on the OUT side, so LIMIT_SW and GND never need to cross; R1602 goes where LIMIT_SW leaves toward the instrument port.

ROUTE: LIMIT_SW and LIMIT_SW_INST leave through vias (port copper); LIMIT_SW_INST carries the INSTRUMENT class.

INTERFACES

+3.3V_SW — +3.3V_SW

Debouncer supply, 2.7 to 5.5 V; bind it to the switched domain of whatever LIMIT_SW drives, so the debouncer cannot back-power a powered-down consumer through OUT.

GND — GND

Return; terminal pin 1 (the switch's other side), the Vcc bypass and the output pull-down.

LIMIT_SW — LIMIT_SW

Debounced switch state, active low on contact closure and about 50 ms late; push-pull at Vcc levels while powered, held low by R1601 when +3.3V_SW is off.

LIMIT_SW_INST — LIMIT_SW_INST

Instrument tap of LIMIT_SW through R1602 (1 k), INSTRUMENT class; reads asserted while the switched rail is off.

OPERATION

Signal path: J1601 pin 2 -> IN -> U1601 IN (pin 2) -> OUT (pin 3) -> LIMIT_SW, tapped through R1602 to LIMIT_SW_INST; J1601 pin 1 is GND. A closed contact pulls IN low; OUT follows IN non-inverting after the debounce (20 to 80 ms, 50 ms typical), so LIMIT_SW is active low and asserts late: bound the homing approach velocity.

IN is complete inside U1601: internal pull-up 63 k typical, -25 to +25 V range, +/-15 kV air-gap ESD. No external pull-up, series resistor or capacitor on IN; a capacitor fights the debounce and degrades the ESD rating.

Supply 2.7 to 5.5 V at 6 uA typical (UVLO 1.9 to 2.6 V). R1601 (100 k) defines LIMIT_SW low while +3.3V_SW is off, since the MAX6816 has no loff; the net idles high with a normally-open contact (about 33 uA at 3.3 V), so a capture on LIMIT_SW_INST reads asserted whenever the switched rail is off.

Same circuit as limit_switch_debounced_input plus the tap. J1601 (Phoenix MCV 1.5/2-G-3.5) is pad-identical to the horizontal MC 1.5 but anchored on pin 1, with a 4.75 mm inboard courtyard and the wire leaving perpendicular to the board. Never rotate it 180 degrees to face outboard: that swaps GND and the switch node in board space.

DESIGN CONTRACT

Debounced limit-switch input with its own 2-position 3.5 mm VERTICAL, top-entry pluggable screw terminal — Phoenix MCV 1.5/2-G-3.5, OW-CONN-TBH-1X02-3P5-VERT, on the local orb_weaver_tht copy of the MCV footprint — plus a MAX6816 single switch debouncer and local Vcc decoupling. Four parts: nothing external belongs on the IN side; because the MAX6816 supplies its own IN pull-up and +/-15 kV ESD protection and needs no external pull-up, series resistor, or input capacitor — the fourth part is a 100 kohm pull-down on the OUTPUT, doing an unrelated job. Electrically identical to the horizontal limit_switch_debounced_input block, port for port and part for part including the pull-down: +3.3V_SW, GND, LIMIT_SW.
Connect a dry-contact mechanical switch across the terminal; pin 1 is GND, pin 2 is the switch node, and the contact is polarity-agnostic. OUT follows IN non-inverting after roughly 50 ms of debounce, so LIMIT_SW is ACTIVE LOW on switch closure and asserts ~50 ms late — bound homing approach velocity so that delay cannot overshoot the mechanical stop.
Supply +3.3V from the SWITCHED power domain on any board where LIMIT_SW drives a chip that can be powered down: if the debouncer stays alive while its consumer does not, OUT back-powers that chip through its input pin, by a route a GPIO bus switch cannot cover. On mouse-joystick-pcb that means +3V3_SW, and LIMIT_SW fans out to the TMC5130A REFL pin and to an always-on instrumentation buffer — it reaches no MCU GPIO in any revision, decided 2026-08-16, so nothing downstream defines this net either.
R1601, 100 kohm from LIMIT_SW to GND (OW-PASS-RC0402/R-07100KL, LCSC C106234), is what defines it while that domain is down, and it is REQUIRED, not optional: THE MAX6816 HAS NO loff. With Vcc at 0 V its push-pull OUT is undefined, and a board that taps LIMIT_SW for instrumentation must put the tap buffer on the ALWAYS-ON rail — a buffer on the switched rail cannot observe the domain it is powering down with — so without this resistor a live, non-Schmitt CMOS input sees a floating source every time the switched domain is cycled, which on that board is the normal reset path. IT BELONGS IN THE BLOCK, NOT AT BOARD LEVEL, and that does not contradict the usual rule: that rule exists because a net shared between two instances of one block gets its pull halved, and LIMIT_SW is point-to-point inside a single instance — place this block twice and you get two switches, two debouncers and two independent LIMIT_SW nets, each with its own pull-down. The same call is already made in quadrature_encoder_input_5v_sn74lvc2g17, whose R30005/R30006 cover loff high-Z on that block's outputs for exactly this reason; the case here is stronger, because the SN74LVC2G17 has loff and the MAX6816 does not.
100 kohm AND NOT 10 kohm: this net idles HIGH, since a normally-open contact plus the internal IN pull-up puts OUT high whenever the axis is away from the limit, so the pull-down conducts continuously in the normal state — 33 uA at 100 kohm against 330 uA at 10 kohm — and 100 kohm spends no meaningful VOH margin either.
KNOW THE POLARITY CONSEQUENCE BEFORE TRUSTING A CAPTURE: LIMIT_SW is active low, so this resistor makes an instrument tap read ASSERTED, limit reached, whenever the switched rail is off. Defined-but-untrue is the deliberate trade against floating, and the analysis layer must gate the channel on rail state. A pull-up is not an alternative — it would have to reference the switched rail, which is at 0 V exactly when it would be needed.
Bring REFL to a labelled test pad at board level so a jumper can force a closure during bring-up. Add no capacitor on IN — it fights the debounce and degrades the ESD rating. Keep the decoupling hard against Vcc.
ROUTING THE PULL-DOWN IS TIGHT, AND IT IS AT THE LIMIT: R1601 sits above the MAX6816 with its LIMIT_SW pad on the same side as the IC's OUT pin, so the two nets never need to cross — but they share a corridor bounded by the IN pad and silt on 0.5 mm centres. EVERY TRACK IN THIS BLOCK IS THEREFORE 0.3 mm, not the 0.4 mm it was authored at, which puts the LIMIT_SW-to-GND gap at exactly 0.200 mm against a 0.200 mm netclass rule and the GND-to-IN-pad gap at 0.225 mm: DRC-clean with ZERO MARGIN on the first of those. Do not widen either run without moving it first — 0.4 mm on these centres is a 0.100 mm gap, which sits exactly on the JLCPCB routine copper floor in .kicad_dru and errors under any 0.2 mm netclass. There is room to move: the LIMIT_SW column can go about 0.5 mm further from GND, straight up out of OUT. Re-run DRC after any change here, because design_block_tools.py check counts only unconnected items and is blind to a clearance error.
THIS BLOCK IS A FORK BY CHOICE, NOT BY GEOMETRY. Unlike usb2_vertical and pycontrol_behavior_port_rj45_boundary_vertical, whose land patterns are unrelated to their horizontal counterparts, this footprint is pad-identical to the horizontal MC 1.5/2-G-3.5: both are 1.8 x 3.6 mm pads on a 1.2 mm drill at 3.50 mm pitch, pin order ascending in +x. The copper is a drop-in; only the footprint ANCHOR moves, because the horizontal is centred on the pad array with pin 1 at (-1.75, 0) while the vertical puts pin 1 at the origin. Migrating an existing placement therefore means changing the part and then MOVING THE FOOTPRINT BY (-1.75, 0) so pad 1 returns to its old absolute position; skip that and the whole connector translates by 1.75 mm and drags every attached track with it. The two parts are genuinely interchangeable at the catalog level and belong to equiv_group conn-tbh-1x02-3p5, which docs/connector-orientation-plan.md specifies but which is not yet populated on any row — treat it as owed. Because the pads are identical, the two layouts stay transferable in either direction once the connector is shifted by (-1.75, 0).
What actually changes is the mechanical envelope, and it inverts. Relative to pad 1 the horizontal courtyard runs x -2.45 to +5.95, y -2.00 to +8.25; the vertical runs x -2.95 to +6.45, y -4.75 to +3.50. The outboard overhang collapses from 8.25 mm to 3.50 mm, so the terminal can move inboard and the board outline notes change — but the INBOARD KEEPOUT GROWS from 2.00 mm to 4.75 mm, so a swap in place can collide with whatever sits behind the connector even though no pad moved. DO NOT ROTATE 180 DEGREES to make the wire entry face outboard: pin order runs the same direction in both footprints, and rotating reverses it in board space, silently swapping GND and the switch node. The wire now leaves perpendicular to the board, so the enclosure in ../mouse-joysticks-mech needs an aperture above the terminal plus clearance for the screw head, the mating plug, and the wire loop.
Project-local pending bench verification; promotable once a second board uses it.

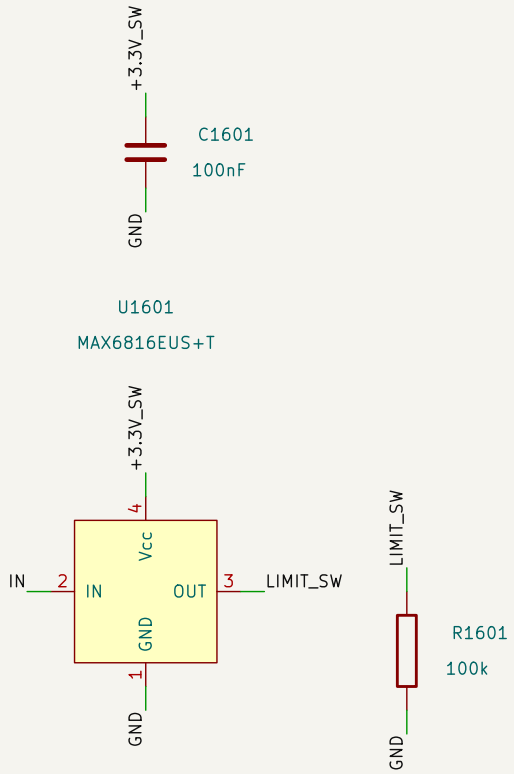
Circuit and PCB layout guidance
Migrated from the saved library sheet; circuit and PCB unchanged
Orb Weaver
Sheet: /motor_encoder_switch/limit_switch_debounced_input_vertical/
File: limit_switch_debounced_input_vertical.kicad_sch

Title: Debounced limit-switch input, vertical terminal

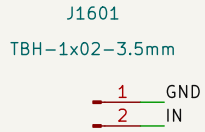
Size: A2	Date: 2026-10-04	**Rev: Source migration 1**
KiCad E.D.A. 10.0.6		Id: 16/20

1. Switch terminal and debouncer

J1601 brings the dry contact onto IN (pin 2) and GND (pin 1); U1601 debounces IN and drives LIMIT_SW from its push-pull OUT. C1601 (100 nF) bypasses Vcc (pin 4) to GND (pin 1).



Switch debouncer
C1601: Vcc bypass for U1601
R1601: Output pull-down for the unpowered state



Vertical switch terminal, pin 1
GND, pin 2 IN

PLACE: Keep U1601 next to J1601 so IN stays short; nothing else connects to IN. Leave the 4.75 mm inboard keepout of the vertical terminal free, and give the enclosure an aperture above it for the plug, the screw head and the wire loop.

PLACE: Place C1601 hard against pin 4 with a short return to pin 1.

ROUTE: The LIMIT_SW and GND runs share the corridor bounded by the IN pad on 0.5 mm centres: every track in the block is 0.3 mm, which leaves the LIMIT_SW-to-GND gap at exactly the 0.200 mm netclass rule. Move a run before widening it and re-run DRC after any change here.

ROUTE: +3.3V_SW has no reference-project class here (Default); the placing board classes the switched rail.

2. Output pull-down and ins

R1601 (100 k) holds LIMIT_SW low

Instrument tap series resistor

PLACE: R1601 sits above U1601 wit
instrument port.

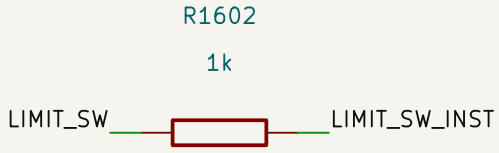
ROUTE: LIMIT_SW and LIMIT_SW_INST

5 6 7 8

on the local orb_weaver_tht copy of the MCV footprint — plus a MAX6816 single switch debouncer and local Vcc decoupling.

2. Output pull-down and instrument tap

R1601 (100 k) holds LIMIT_SW low while the debouncer is unpowered; R1602 (1 k) is the series tap from LIMIT_SW to LIMIT_SW_INST.



Instrument tap series resistor

PLACE: R1601 sits above U1601 with its LIMIT_SW pad on the OUT side, so LIMIT_SW and GND never need to cross; R1602 goes where LIMIT_SW leaves toward the instrument port.

ROUTE: LIMIT_SW and LIMIT_SW_INST leave through vias (port copper); LIMIT_SW_INST carries the INSTRUMENT class.

9 10 11

INTERFACES

+3.3V_SW — +3.3V_SW

Debouncer supply, 2.7 to 5.5 V; bind it to the switched domain of whatever LIMIT_SW drives, so the debouncer cannot back-power a powered-down consumer through OUT.

GND — GND

Return; terminal pin 1 (the switch's other side), the Vcc bypass and the output pull-down.

LIMIT_SW — LIMIT_SW

Debounced switch state, active low on contact closure and about 50 ms late; push-pull at Vcc levels while powered, held low by R1601 when +3.3V_SW is off.

LIMIT_SW_INST — LIMIT_SW_INST

Instrument tap of LIMIT_SW through R1602 (1 k), INSTRUMENT class; reads asserted while the switched rail is off.

Debounced switch state, active low on contact closure and about 50 ms late; push-pull at Vcc levels while powered, held low by R1601 when +3.3V_SW is off.

LIMIT_SW_INST LIMIT_SW_INST

Instrument tap of LIMIT_SW through R1602 (1 k), INSTRUMENT class; reads asserted while the switched rail is off.

OPERATION

Signal path: J1601 pin 2 -> IN -> U1601 IN (pin 2) -> OUT (pin 3) -> LIMIT_SW, tapped through R1602 to LIMIT_SW_INST; J1601 pin 1 is GND. A closed contact pulls IN low; OUT follows IN non-inverting after the debounce (20 to 80 ms, 50 ms typical), so LIMIT_SW is active low and asserts late: bound the homing approach velocity.

IN is complete inside U1601: internal pull-up 63 k typical, -25 to +25 V range, +/-15 kV air-gap ESD. No external pull-up, series resistor or capacitor on IN; a capacitor fights the debounce and degrades the ESD rating.

Supply 2.7 to 5.5 V at 6 uA typical (UVLO 1.9 to 2.6 V). R1601 (100 k) defines LIMIT_SW low while +3.3V_SW is off, since the MAX6816 has no Ioff; the net idles high with a normally-open contact (about 33 uA at 3.3 V), so a capture on LIMIT_SW_INST reads asserted whenever the switched rail is off.

Same circuit as limit_switch_debounced_input plus the tap. J1601 (Phoenix MCV 1,5/2-G-3,5) is pad-identical to the horizontal MC 1,5 but anchored on pin 1, with a 4.75 mm inboard courtyard and the wire leaving perpendicular to the board. Never rotate it 180 degrees to face outboard: that swaps GND and the switch node in board space.

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ROUTING THE PULL-DOWN IS TIGHT, AND IT IS AT THE LIMIT: R1601 sits above the MAX6816 with its LIMIT_SW pad on the same side as the IC's OUT pin, so the two nets never need to cross — but they share a corridor bounded by the IN pad and sit on 0.5 mm centres. EVERY TRACK IN THIS BLOCK IS THEREFORE 0.3 mm, not the 0.4 mm it was authored at, which puts the LIMIT_SW-to-GND gap at exactly 0.200 mm against a 0.200 mm netclass rule and the GND-to-IN-pad gap at 0.225 mm: DRC-clean with ZERO MARGIN on the first of those. Do not widen either run without moving it first — 0.4 mm on these centres is a 0.100 mm gap, which sits exactly on the JLCPCB routine copper floor in .kicad_dru and errors under any 0.2 mm netclass. There is room to move: the LIMIT_SW column can go about 0.5 mm further from GND, straight up out of OUT. Re-run DRC after any change here, because design_block_tools.py check counts only unconnected items and is blind to a clearance error.
THIS BLOCK IS A FORK BY CHOICE, NOT BY GEOMETRY. Unlike usb2_vertical and pycontrol_behavior_port_rj45_boundary_vertical, whose land patterns are unrelated to their horizontal counterparts, this footprint is pad-identical to the horizontal MC 1,5/2-G-3,5: both are 1.8 x 3.6 mm pads on a 1.2 mm drill at 3.50 mm pitch, pin order ascending in +x. The copper is a drop-in; only the footprint ANCHOR moves, because the horizontal is centred on the pad array with pin 1 at (-1.75, 0) while the vertical puts pin 1 at the origin. Migrating an existing placement therefore means changing the part and then MOVING THE FOOTPRINT BY (-1.75, 0) so pad 1 returns to its old absolute position; skip that and the whole connector translates by 1.75 mm and drags every attached track with it. The two parts are genuinely interchangeable at the catalog level and belong to equiv_group conn-tbh-1x02-3p5, which docs/connector-orientation-plan.md specifies but which is not yet populated on any row — treat it as owed. Because the pads are identical, the two layouts stay transferable in either direction once the connector is shifted by (-1.75, 0).
What actually changes is the mechanical envelope, and it inverts. Relative to pad 1 the horizontal courtyard runs x -2.45 to +5.95, y -2.00 to +8.25; the vertical runs x -2.95 to +6.45, y -4.75 to +3.50. The outboard overhang collapses from 8.25 mm to 3.50 mm, so the terminal can move inboard and the board outline notes change — but the INBOARD KEEPOUT GROWS from 2.00 mm to 4.75 mm, so a swap in place can collide with whatever sits behind the connector even though no pad moved. DO NOT ROTATE 180 DEGREES to make the wire entry face outboard: pin order runs the same direction in both footprints, and rotating reverses it in board space, silently swapping GND and the switch node. The wire now leaves perpendicular to the board, so the enclosure in ../mouse-joysticks-mech needs an aperture above the terminal plus clearance for the screw head, the mating plug, and the wire loop.
Project-local pending bench verification; promotable once a second board uses it.

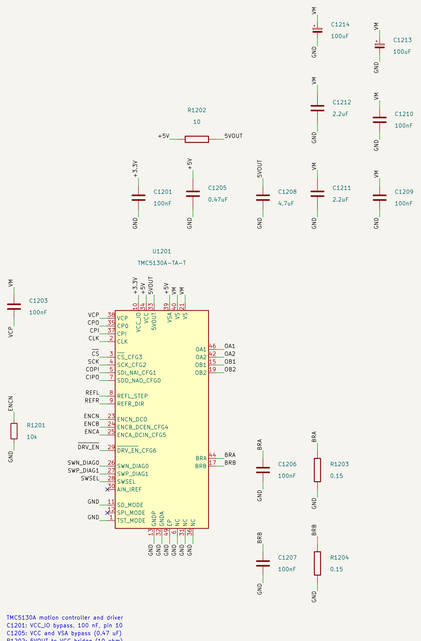
TMC5130A motion-controller core | paired sense shunts by variant, SPI or UART profile

TMC5130A motion-controller core with paired external current-sense resistors

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Driver core

U1201, the TMC5130A: SPI or UART in, encoder and reference switches in, two full bridges out on OA1/OA2 and OB1/OB2, diagnostics on SWP/SWN. R1203 and R1204 (the variant's shunts) return BRA and BRB to GND; C1206 and C1207 (100 nF) filter the sense nodes. R1202 (10 ohm) bridges 5VOUT to VCC and +5V; C1208 (4.7 uF) is the regulator's output capacitor, C1205 (0.47 uF) the VCC/VSA bypass. C1213 and C1214 (100 uF) hold VM: C1211 and C1212 (2.2 uF 100 V) and C1209, C1210 (100 nF) bypass VS at the package. C1201 and C1204 (100 nF) bypass VCC_IO and the oscillator's +3.3V. R1201 (10 k) pulls ENCN down.



TMC5130A motion controller and driver
C1201: VCC_IO bypass, 100 nF, pin 10
C1205: VCC and VSA bypass (0.47 uF)
R1202: 5VOUT to VCC bridge (10 ohm)
R1201: ENCN pull-down, 10 k
C1206: BRA sense filter, 100 nF
R1203: phase_a_shunt
C1207: BRB sense filter, 100 nF
R1204: phase_b_shunt
C1208: 5VOUT regulator output capacitor, 4.7 uF
C1209, C1210: VS bypass, 100 nF, pins 21/40
C1213, C1214: VM bulk (100 uF electrolytic)
C1211, C1212: VM bypass (2.2 uF 100 V)
C1203: VCP reservoir to VM, 100 nF

PLACE: The package centre is the family anchor driver_center; the exposed pad (49) takes the thermal vias of the footprint into the GND pour.

PLACE: Place each shunt right at its BR pin (44, 17) with the filter capacitor beside it; the sense loops set the current accuracy.

PLACE: Place C1208 at pin 33 and C1205 at pins 34/39 with short returns to GNDA (32); R1202 between them.

PLACE: Place the 100 nF and 2.2 uF parts at VS pins 21 and 40, the electrolytics behind them on the VM entry.

PLACE: Place C1201 at pin 10 and C1204 at X1201's VDD; R1201 near pin 23.

ROUTE: Keep the bridge outputs (MOTOR_2A) and the BRA/BRB shunt loops short and on the component side; logic on the other side of the package.

ROUTE: Kelvin-style short returns from the shunts to GNDP; no shared copper with the bulk capacitors' ripple current.

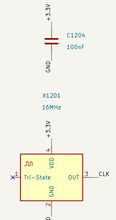
ROUTE: +5V is the board's rail (PWR_5V); 5VOUT stays inside the block.

ROUTE: VM is PWR_HV_BUS: wide copper from the bulk capacitors to the VS pins; the ripple-current return to GNDP, not through the sense shunts.

ROUTE: +3.3V is the board's rail (PWR_3V3); ENCN is a logic input.

2. Clock

X1201 (16 MHz oscillator on +3.3V) drives CLK (pin 2); its Tri-State input is open. C1201 and C1204 (100 nF) bypass VCC_IO and the oscillator's +3.3V; R1201 (10 k) pulls ENCN down.



16 MHz oscillator for CLK
C1204: Oscillator VDD bypass, 100 nF

PLACE: Place X1201 close to U1201 pin 2 (CLK) with its GND at the package's ground.

PLACE: Place C1201 at pin 10 and C1204 at X1201's VDD; R1201 near pin 23.

ROUTE: CLK is a 16 MHz single-ended line: short, no stubs.

ROUTE: +3.3V is the board's rail (PWR_3V3); ENCN is a logic input.

3. Charge pump

C1202 (22 nF 100 V) is the flying capacitor between CPO and CPI; C1203 (100 nF) holds VCP above VM.

Charge pump flying capacitor (22 nF 100 V)

PLACE: Place both at pins 35 to 38 with the shortest loops: C1203's far end goes to the VM copper.

ROUTE: BOOTSTRAP class: the charge pump switches at the chopper frequency, keep it away from the sense nodes.

4. Instrument taps

100 ohm taps R1205 to R1208 on $\overline{CS}$, SCK, COPI and CIPO; 1 k taps R1209 to R1211 on SWN_DIAG0, SWP_DIAG1 and $\overline{DRV_EN}$; each to its _INST port.

PLACE: A row toward the instrument-port side of the block.

ROUTE: INSTRUMENT class to the instrument port; see the note on the shared-line taps.

INTERFACES

VM — VM

Bridge supply VS (pins 21, 40), 5.5 to 46 V. PWR_HV_BUS: bulk C1213/C1214.

+5VO — +5V

VCC (pin 34) and VSA (pin 39), 4.6 to 5.25 V: bridged to 5VOUT through R1202; C1205 bypass.

+3.3VO — +3.3V

I/O supply VCC_IO (pin 10) and the oscillator, 3.0 to 5.25 V; C1201 and C1204 bypass.

GNDO — GND

Return: GNDP (13, 48), GNDA (32), the pad (49), TST_MODE (1) and SD_MODE (11) tied low.

CIPOO — CIPO

SPI data out SDO (pin 7; NAO in the UART profile), tapped by R1208.

COPIO — COPI

SPI data in SDI (pin 5; NAI in the UART profile), tapped by R1207.

ENCAO — ENCA

Encoder A input (pin 25), 3.3 V logic.

ENCBO — ENCB

Encoder B input (pin 24), 3.3 V logic.

ENCNO — ENCN

Encoder index N input (pin 23), pulled down by R1201 (10 k).

OA1O — OA1

Motor phase A output 1 (pin 46), MOTOR_2A class.

OA2O — OA2

Motor phase A output 2 (pin 42), MOTOR_2A class.

OB1O — OB1

Motor phase B output 1 (pin 15), MOTOR_2A class.

OB2O — OB2

Motor phase B output 2 (pin 19), MOTOR_2A class.

REFLO — REFL

REFL_STEP (pin 8): left reference switch, or STEP in step/dir mode.

REFRO — REFR

REFR_DIR (pin 9): right reference switch, or DIR: the SPI profile ties it to GND.

SCKO — SCK

SPI clock SCK_CFG2 (pin 4): 4 MHz max on the internal clock, 8 MHz with the 16 MHz oscillator.

SWN_DIAG0O — SWN_DIAG0

SWN_DIAG0 (pin 26): DIAG0 output in SPI, SWDN of the single-wire UART pair.

SWP_DIAG1O — SWP_DIAG1

SWP_DIAG1 (pin 27): DIAG1 output in SPI, SWDP of the UART pair.

SWSELO — SWSEL

SWSEL (pin 28): low (internal pull-down) selects SPI, high selects the UART.

$\overline{CS}$O — $\overline{CS}$

SPI chip select $\overline{CS}$_CFG3 (pin 3), active low, tapped by R1205.

$\overline{DRV_EN}$O — $\overline{DRV_EN}$

$\overline{DRV_EN}$_CFG6 (pin 29): low enables the driver stage, tapped by R1211.

CIPO_INSTO — CIPO_INST

100 ohm tap on CIPO for the instrument port.

COPI_INSTO — COPI_INST

100 ohm tap on COPI for the instrument port.

SCK_INSTO — SCK_INST

100 ohm tap on SCK for the instrument port.

SWN_DIAG0_INSTO — SWN_DIAG0_INST

1 k tap on SWN_DIAG0 for the instrument port.

SWP_DIAG1_INSTO — SWP_DIAG1_INST

1 k tap on SWP_DIAG1 for the instrument port.

$\overline{CS}$_INSTO — $\overline{CS}$_INST

100 ohm tap on $\overline{CS}$ for the instrument port.

$\overline{DRV_EN}$_INSTO — $\overline{DRV_EN}$_INST

1 k tap on $\overline{DRV_EN}$ for the instrument port.

INTERNAL NETS

5VOUT: Internal 5 V regulator output (pin 33), C1208 (4.7 uF): bridged to VCC and +5V through R1202 (10 ohm).

BRA: Phase A bridge return (pin 44) through shunt R1203 to GND: C1206 (100 nF) filters it.

BRB: Phase B bridge return (pin 17) through shunt R1204 to GND: C1207 (100 nF) filters it.

CLK: 16 MHz from X1201 OUT into CLK (pin 2).

CPI: Charge pump flying capacitor C1202 (22 nF 100 V), CPI side (pin 37).

CPO: Charge pump flying capacitor C1202, CPO side (pin 35).

VCP: Charge pump output (pin 38), C1203 (100 nF) to VM.

OPERATION

Supplies: VM (5.5 to 46 V, PWR_HV_BUS) on VS (pins 21, 40) with C1213 and C1214 (100 uF) bulk, C1211 and C1212 (2.2 uF 100 V) and C1209, C1210 (100 nF) bypass: +5V on VSA (39) and VCC (34), so the internal 5 V regulator is bridged: 5VOUT (33) feeds VCC through R1202 (10 ohm) with C1208 (4.7 uF) and C1205 (0.47 uF) as its capacitors (facts: 4.7 to 5.4 V with the regulator bridged, VCC 4.6 to 5.25 V); +3.3V on VCC_IO (10) and the oscillator (3.0 to 5.25 V). Supply current about 15 mA at 16 MHz with the driver disabled.

Clock and modes: X1201 (16 MHz oscillator, Tri-State pin 1 open) drives CLK (pin 2), which lets SCK run to 8 MHz (4 MHz on the internal clock). TST_MODE (1) and SD_MODE (11) are tied to GND: motion-controller mode with the internal ramp generator, not step/dir. SPI_MODE (12) is left open (internal pull-up, high) and AIN_IREF (30) open (internal reference, no analog current scaling): ENCN is pulled down by R1201 (10 k); $\overline{DRV_EN}$ low enables the bridges.

Current sense and variants (family.json): external sensing on BRA (44) and BRB (17) through R1203 and R1204; the variant selects both shunts together, rS0 = OW-PASS-RLH12FTCR150 (0.15 ohm, 1 W) and rS20 = OW-PASS-KRL1632E-W-R120-F-T5 (0.12 ohm, 0.75 W). I_RMS = ((CS + 1) / 32) x V_FS / (R + 0.02 ohm) / sqrt(2) with V_FS 0.325 V (vsense 0) or 0.180 V (vsense 1): at CS = 31 about 1.35 / 0.75 A RMS for 0.15 ohm and 1.64 / 0.91 A for 0.12 ohm against the 1.4 A RMS design guideline; the shunt_pair_inventory qualification judges stock and dissipation at publication (release.json). Firmware sets vsense, IRUN and IHOLD; the KiCad variant does not.

Profiles (family.json): the SPI blocks are placed with SWSEL and REFR to GND (SPI_MODE high by its pull-up, SD_MODE low) and talk on SCK, COPI (SDI), CIPO (SDO) and $\overline{CS}$, each tapped by 100 ohm into an instrument port; the UART blocks are placed with SWSEL to +3.3V, SCK to GND and $\overline{CS}$ to +3.3V, SWP_DIAG1 as SWIOP and SWN_DIAG0 as SWION (the single-wire pair, RS-485-like differential or single wire). COPI and CIPO as NAI and NAO for the address chain: BN1, sync 0x05, CRC8, 9000 baud minimum at 20 MHz CLK, fCLK / 16 maximum. SPI and UART blocks share one copper; they differ in description and Profile field only.

Charge pump: C1202 (22 nF 100 V) between CPO (35) and CPI (37) and C1203 (100 nF) from VCP (38) to VM supply the high-side gates; the undervoltage threshold is VCP - VS of about 3.6 V. Motor outputs OA1/OA2 (46, 42) and OB1/OB2 (15, 19) carry the MOTOR_2A class, 1.4 A RMS per coil as the design guideline, 2 A peak.

What the board provides and an inherited deviation: the motor connector and the VM entry on their own classes; the bus pulls, the mode-pin ties of the chosen profile and the instrument port behind the taps. This core carries taps on the shared SPI lines SCK, COPI and CIPO (R1206 to R1208) as well as on its own $\overline{CS}$, SWP/SWN and $\overline{DRV_EN}$: a board that places two cores on one bus gets two taps per shared line, a deviation from layout convention 14 (shared lines are tapped once, by the board) that the migration preserves rather than corrects.

DESIGN NOTES

TMC5130 Rsense options in stock, approx full-scale current at CS=31:
360m 1206 250mW: vsense=0 0.60A RMS / 0.86A peak vsense=1 0.35A RMS / 0.47A peak OW-PASS-RL1206FR-070R36L 150m 1206 1W: vsense=0 1.35A RMS / 1.91A peak vsense=1 0.75A RMS / 1.06A peak OW-PASS-RLH12FTCR150 120m 1206 750mW: vsense=0 1.64A RMS / 2.32A peak vsense=1 0.91A RMS / 1.29A peak OW-PASS-KRL1632E-W-R120-F-T5 Set lower current in firmware; choose Rsense so normal IRUN is ~16-31.
TMC5130 TQFP thermal behavior needs validation above ~1.2A RMS continuous.

SWSEL (pin 28): tie HIGH for the UART profile; its level does not matter for SPI (the SPI profile ties it to GND; left open, the internal pull-down reads low).

DESIGN CONTRACT

TMC5130A motion-controller core with paired external current-sense resistors

Circuit and PCB layout guidance
Migrated from the saved family core: circuit, variants and PCB unchanged
Orb Weaver

Sheet: /motor_encoder_switch/tmc5130/
File: tmc5130.kicad_sch

Title: TMC5130 motion-controller core family

Size: A1	Date: 2026-10-04	**Rev: Source migration 1**
KiCad E.D.A. 10.0.6		Id: 12/20

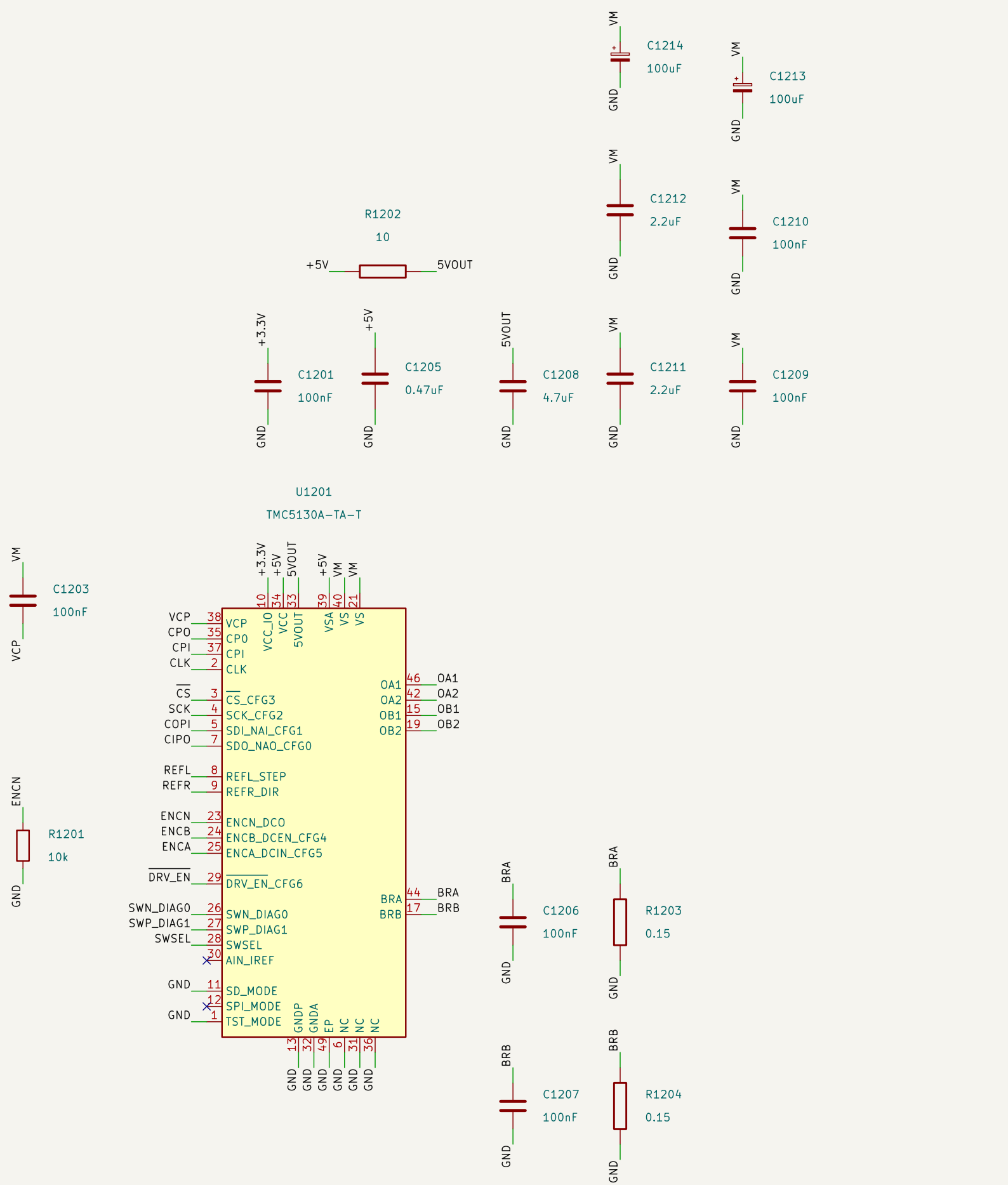
TMC5130A motion–controller core | paired sense shunts by variant, SPI or UART profile

TMC5130A motion–controller core with paired external current–sense resistors

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Driver core

U1201, the TMC5130A: SPI or UART in, encoder and reference switches in, two full bridges out on OA1/OA2 and OB1/OB2, diagnostics on SWP/SWN. R1203 and R1204 (the variant's shunts) return BRA and BRB to GND; C1206 and C1207 (100 nF) filter the sense nodes. R1202 (10 ohm) bridges 5VOUT to VCC and +5V; C1208 (4.7 uF) is the regulator's output capacitor, C1205 (0.47 uF) the VCC/VSA bypass. C1213 and C1214 (100 uF) hold VM; C1211 and C1212 (2.2 uF 100 V) and C1209, C1210 (100 nF) bypass VS at the package. C1201 and C1204 (100 nF) bypass VCC_IO and the oscillator's +3.3V; R1201 (10 k) pulls ENCN down.



TMC5130A motion controller and driver
C1201: VCC_IO bypass, 100 nF, pin 10
C1205: VCC and VSA bypass (0.47 uF)
R1202: 5VOUT to VCC bridge (10 ohm)
R1201: ENCN pull-down, 10 k
C1206: BRA sense filter, 100 nF
R1203: phase_a_shunt
C1207: BRB sense filter, 100 nF
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C1208: 5VOUT regulator output capacitor, 4.7 uF
C1209, C1210: VS bypass, 100 nF, pins 21/40
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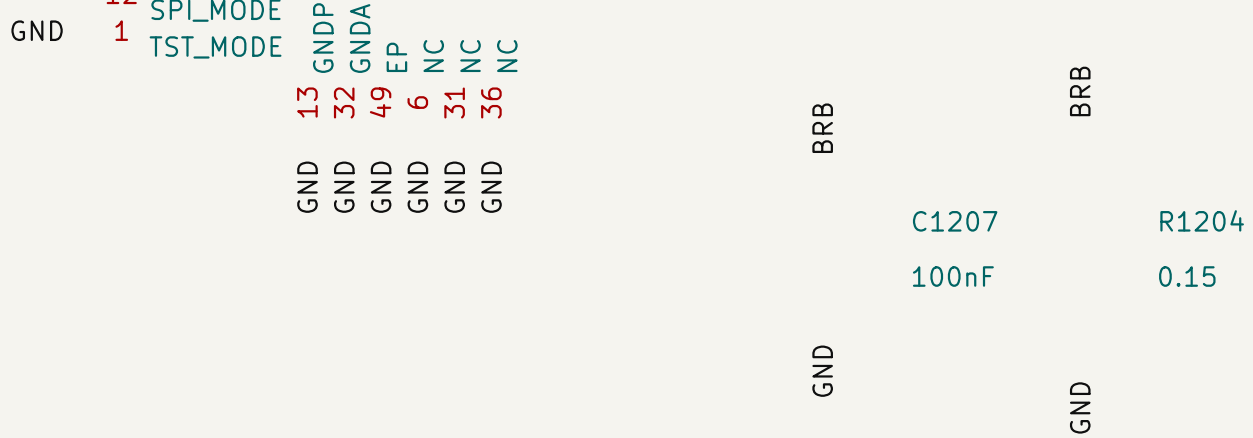
C1203: VCP reservoir to VM, 100 nF



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PLACE: The package centre is the family anchor driver_center; the exposed pad (49) takes the thermal vias of the footprint into the GND pour.

PLACE: Place each shunt right at its BR pin (44, 17) with the filter capacitor beside it; the sense loops set the current accuracy.

PLACE: Place C1208 at pin 33 and C1205 at pins 34/39 with short returns to GNDA (32); R1202 between them.

PLACE: Place the 100 nF and 2.2 uF parts at VS pins 21 and 40, the electrolytics behind them on the VM entry.

PLACE: Place C1201 at pin 10 and C1204 at X1201's VDD; R1201 near pin 23.

ROUTE: Keep the bridge outputs (MOTOR_2A) and the BRA/BRB shunt loops short and on the component side; logic on the other side of the package.

ROUTE: Kelvin-style short returns from the shunts to GNDP; no shared copper with the bulk capacitors' ripple current.

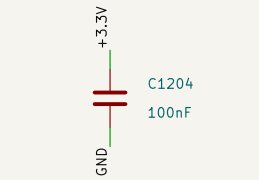
ROUTE: +5V is the board's rail (PWR_5V); 5VOUT stays inside the block.

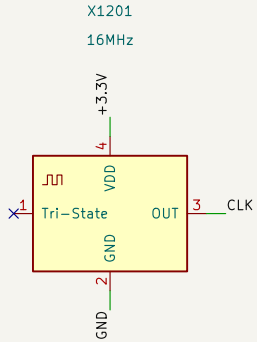
ROUTE: VM is PWR_HV_BUS: wide copper from the bulk capacitors to the VS pins; the ripple-current return to GNDP, not through the sense shunts.

ROUTE: +3.3V is the board's rail (PWR_3V3); ENCN is a logic input.

2. Clock

X1201 (16 MHz oscillator on +3.3V) drives CLK (pin 2); its Tri-State input is open. C1201 and C1204 (100 nF) bypass VCC_IO and the oscillator's +3.3V; R1201 (10 k) pulls ENCN down.





16 MHz oscillator for CLK
C1204: Oscillator VDD bypass,
100 nF

PLACE: Place X1201 close to U1201 pin 2 (CLK) with its GND at the package's ground.

PLACE: Place C1201 at pin 10 and C1204 at X1201's VDD; R1201 near pin 23.

ROUTE: CLK is a 16 MHz single-ended line: short, no stubs.

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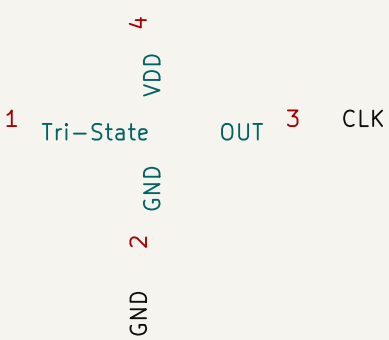

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3. Charge pump

C1202 (22 nF 100 V) is the flying capacitor between CPO and CPI; C1203 (100 nF) holds VCP above VM.

Charge pump flying
capacitor (22 nF 100
V)

PLACE: Place both at pins 35 to 38 with the shortest loops; C1203's far end goes to the VM copper.

ROUTE: BOOTSTRAP class; the charge pump switches at the chopper frequency, keep it away from the sense nodes.

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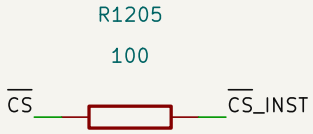
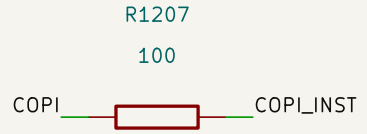
4. Instrument taps

100 ohm taps R1205 to R1208 on $\overline{CS}$, SCK, COPI and CIPO; 1 k taps R1209 to R1211 on SWN_DIAG0, SWP_DIAG1 and $\overline{DRV_EN}$; each to its _INST port.

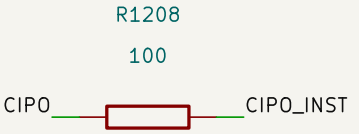


Instrument tap, 100 R, $\overline{CS}$

Instrument tap, 100 R, SCK



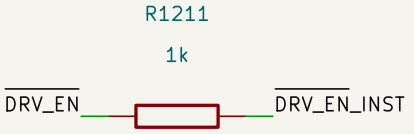
Instrument tap, 100 R, COPI



Instrument tap, 100 R, CIPO

Instrument tap, 1 k, SWN_DIAG0

Instrument tap, 1 k, SWP_DIAG1



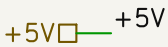
Instrument tap, 1 k, $\overline{DRV_EN}$

PLACE: A row toward the instrument–port side of the block.

ROUTE: INSTRUMENT class to the instrument port; see the note on the shared–line taps.

INTERFACES

Bridge supply VS (pins 21, 40), 5.5 to 46 V, PWR_HV_BUS; bulk C1213/C1214.

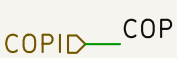


VCC (pin 34) and VSA (pin 39), 4.6 to 5.25 V; bridged to 5VOUT through R1202; C1205 bypass.

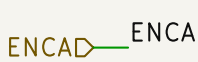
I/O supply VCC_IO (pin 10) and the oscillator, 3.0 to 5.25 V; C1201 and C1204 bypass.

Return: GNDP (13, 48), GNDA (32), the pad (49), TST_MODE (1) and SD_MODE (11) tied low.

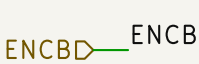
SPI data out SDO (pin 7; NAO in the UART profile), tapped by R1208.



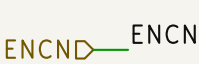
SPI data in SDI (pin 5; NAI in the UART profile), tapped by R1207.



Encoder A input (pin 25), 3.3 V logic.



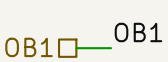
Encoder B input (pin 24), 3.3 V logic.



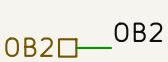
Encoder index N input (pin 23), pulled down by R1201 (10 k).

Motor phase A output 1 (pin 46), MOTOR_2A class.

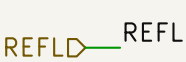
Motor phase A output 2 (pin 42), MOTOR_2A class.



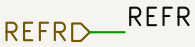
Motor phase B output 1 (pin 15), MOTOR_2A class.



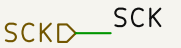
Motor phase B output 2 (pin 19), MOTOR_2A class.



REFL_STEP (pin 8): left reference switch, or STEP in step/dir mode.



REFR_DIR (pin 9): right reference switch, or DIR; the SPI profile ties it to GND.

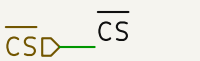


SPI clock SCK_CFG2 (pin 4): 4 MHz max on the internal clock, 8 MHz with the 16 MHz oscillator.

SWN_DIAG0 (pin 26): DIAG0 output in SPI, SWION of the single-wire UART pair.

SWP_DIAG1 (pin 27): DIAG1 output in SPI, SWIOP of the UART pair.

SWSEL (pin 28): low (internal pull-down) selects SPI, high selects the UART.



SPI chip select $\overline{\text{CS}}$_CFG3 (pin 3), active low, tapped by R1205.

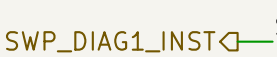
$\overline{\text{DRV_EN}}$_CFG6 (pin 29): low enables the driver stage, tapped by R1211.

100 ohm tap on CIPO for the instrument port.

100 ohm tap on COPI for the instrument port.

100 ohm tap on SCK for the instrument port.

1 k tap on SWN_DIAG0 for the instrument port.



1 k tap on SWP_DIAG1 for the instrument port.

100 ohm tap on $\overline{\text{CS}}$ for the instrument port.

1 k tap on $\overline{\text{DRV_EN}}$ for the instrument port.

SWP_DIAG1_INST SWP_DIAG1_INST

1 k tap on SWP_DIAG1 for the instrument port.

CS_INST CS_INST

100 ohm tap on CS for the instrument port.

DRV_EN_INST DRV_EN_INST

1 k tap on DRV_EN for the instrument port.

INTERNAL NETS

5VOUT: Internal 5 V regulator output (pin 33), C1208 (4.7 uF); bridged to VCC and +5V through R1202 (10 ohm).

BRA: Phase A bridge return (pin 44) through shunt R1203 to GND; C1206 (100 nF) filters it.

BRB: Phase B bridge return (pin 17) through shunt R1204 to GND; C1207 (100 nF) filters it.

CLK: 16 MHz from X1201 OUT into CLK (pin 2).

CPI: Charge pump flying capacitor C1202 (22 nF 100 V), CPI side (pin 37).

CPO: Charge pump flying capacitor C1202, CPO side (pin 35).

VCP: Charge pump output (pin 38), C1203 (100 nF) to VM.

OPERATION

Supplies: VM (5.5 to 46 V, PWR_HV_BUS) on VS (pins 21, 40) with C1213 and C1214 (100 uF) bulk, C1211 and C1212 (2.2 uF 100 V) and C1209, C1210 (100 nF) bypass; +5V on VSA (39) and VCC (34), so the internal 5 V regulator is bridged: 5VOUT (33) feeds VCC through R1202 (10 ohm) with C1208 (4.7 uF) and C1205 (0.47 uF) as its capacitors (facts: 4.7 to 5.4 V with the regulator bridged, VCC 4.6 to 5.25 V); +3.3V on VCC_IO (10) and the oscillator (3.0 to 5.25 V). Supply current about 15 mA at 16 MHz with the driver disabled.

Clock and modes: X1201 (16 MHz oscillator, Tri-State pin 1 open) drives CLK (pin 2), which lets SCK run to 8 MHz (4 MHz on the internal clock). TST_MODE (1) and SD_MODE (11) are tied to GND: motion-controller mode with the internal ramp generator, not step/dir; SPI_MODE (12) is left open (internal pull-up, high) and AIN_IREF (30) open (internal reference, no analog current scaling); ENCN is pulled down by R1201 (10 k); $\overline{\text{DRV_EN}}$ low enables the bridges.

Current sense and variants (family.json): external sensing on BRA (44) and BRB (17) through R1203 and R1204; the variant selects both shunts together, r150 = OW-PASS-RLH12FTCR150 (0.15 ohm, 1 W) and r120 = OW-PASS-KRL1632E-M-R120-F-T5 (0.12 ohm, 0.75 W). I_RMS = ((CS + 1) / 32) x V_FS / (R + 0.02 ohm) / sqrt(2) with V_FS 0.325 V (vsense 0) or 0.180 V (vsense 1): at CS = 31 about 1.35 / 0.75 A RMS for 0.15 ohm and 1.64 / 0.91 A for 0.12 ohm against the 1.4 A RMS design guideline; the shunt_pair_inventory qualification judges stock and dissipation at publication (release.json). Firmware sets vsense, IRUN and IHOLD; the KiCad variant does not.

Profiles (family.json): the SPI blocks are placed with SWSEL and REFR to GND (SPI_MODE high by its pull-up, SD_MODE low) and talk on SCK, COPI (SDI), CIPO (SDO) and $\overline{\text{CS}}$, each tapped by 100 ohm into an instrument port; the UART blocks are placed with SWSEL to +3.3V, SCK to GND and $\overline{\text{CS}}$ to +3.3V, SWP_DIAG1 as SWIOP and SWN_DIAG0 as SWION (the single-wire pair, RS-485-like differential or single wire), COPI and CIPO as NAI and NAO for the address chain; 8N1, sync 0x05, CRC8, 9000 baud minimum at 20 MHz CLK, fCLK / 16 maximum. SPI and UART blocks share one copper; they differ in description and Profile field only.

Charge pump: C1202 (22 nF 100 V) between CPO (35) and CPI (37) and C1203 (100 nF) from VCP (38) to VM supply the high-side gates; the undervoltage threshold is VCP - VS of about 3.6 V. Motor outputs OA1/OA2 (46, 42) and OB1/OB2 (15, 19) carry the MOTOR_2A class, 1.4 A RMS per coil as the design guideline, 2 A peak.

What the board provides and an inherited deviation: the motor connector and the VM entry on their own classes, the bus pulls, the mode-pin ties of the chosen profile and the instrument port behind the taps. This core carries taps on the shared SPI lines SCK, COPI and CIPO (R1206 to R1208) as well as on its own $\overline{\text{CS}}$, SWP/SWN and $\overline{\text{DRV_EN}}$; a board that places two cores on one bus gets two taps per shared line, a deviation from layout convention 14 (shared lines are tapped once, by the board) that the migration preserves rather than corrects.

DESIGN NOTES

TMC5130 Rsense options in stock, approx full-scale current at CS=31:
360m 1206 250mW: vsense=0 0.60A RMS / 0.86A peak; vsense=1 0.33A RMS / 0.47A peak OW-PASS-RL1206FR-070R36L 150m 1206 1W: vsense=0 1.35A RMS / 1.91A peak; vsense=1 0.75A RMS / 1.06A peak OW-PASS-RLH12FTCR150 120m 1206 750mW: vsense=0 1.64A RMS / 2.32A peak; vsense=1 0.91A RMS / 1.29A peak OW-PASS-KRL1632E-M-R120-F-T5 Set lower current in firmware; choose Rsense so normal IRUN is ~16-31. TMC5130 TQFP thermal behavior needs validation above ~1.2A RMS continuous.

SWSEL (pin 28): tie HIGH for the UART profile; its level does not matter for SPI (the SPI profile ties it to GND; left open, the internal pull-down reads low).

DESIGN CONTRACT

TMC5130A motion-controller core with paired external current-sense resistors

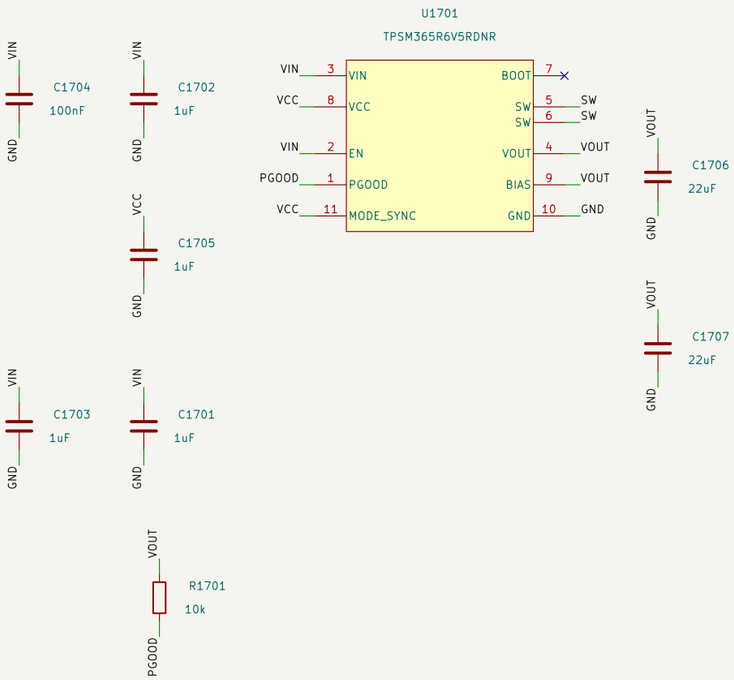
TPSM365R6 fixed-output buck | 5 V or 3.3 V variant, 600 mA, PGOOD to VOUT

High-voltage input to a fixed 5 V or 3.3 V rail: TI TPSM365R6V5 or V3 600 mA buck module, one family source with the regulator part and the second output capacitor as the variant

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Buck module and output capacitors

U1701 converts VIN to the fixed VOUT; C1706 and C1707 (22 uF) hold the output. C1707 is unpopulated on the 3v3 variant. Three 1 uF 100 V capacitors and a 100 nF high-frequency bypass across VIN to GND at the module's input. C1705 (1 uF) bypasses the internal LDO output VCC (pin 8), which also sets MODE/SYNC to forced PWM. R1701 (10 k) pulls the open-drain PGOOD (pin 1) up to VOUT.



regulator
C1706: cout_a
C1707: cout_b
C1701: cin_a
C1703: cin_c
C1702: cin_b
C1704: cin_hf
C1705: cvcc
R1701: pgood_pullup

PLACE: Place C1706 and C1707 at VOUT (pin 4) with their GND ends at pin 10; keep the output loop short and on one layer.

PLACE: Place C1704 (100 nF) closest to VIN (pin 3) and GND (pin 10), the 1 uF parts beside it; the input current loop is the noisiest on the block.

PLACE: Place C1705 at pin 8 with a short return to pin 10.

PLACE: Anywhere between VOUT and the PGOOD port; a low-current node.

ROUTE: VOUT is block-local copper (PWR_5V_LOCAL); the board names and classes the net on its side of the sheet pin.

ROUTE: Wide, short VIN copper from the capacitors into pin 3; no via between C1704 and the module if the layer allows it.

ROUTE: VCC stays inside the block; nothing else loads it.

ROUTE: PGOOD is a logic flag on the Default class; its high level equals VOUT.

INTERFACES

VIN — VIN

3.6 to 65 V input on VIN (pin 3) and EN (pin 2, tied: always enabled).

VOUT — VOUT

Fixed 5 V or 3.3 V output by variant, 600 mA; FB/BIAS (pin 9) tied here.

GND — GND

Return for the module (pin 10) and every input and output capacitor.

PGOOD — PGOOD

Open-drain power good, pulled up to VOUT by R1701 (10 k); high level is VOUT.

INTERNAL NETS

VCC: Internal LDO output (pin 8), bypassed by C1705; MODE/SYNC (pin 11) tied here selects forced PWM.

SW: Switch node of the module's integrated inductor: pins 5 and 6 tied to each other, nothing external.

OPERATION

Signal path: VIN (3.6 to 65 V after start-up, UVLO rising 3.4 V typical) enters VIN (pin 3) and EN (pin 2, tied to VIN, so the module runs whenever input is present); the integrated-inductor module delivers VOUT (pin 4), 600 mA maximum; FB/BIAS (pin 9) is tied to VOUT for the fixed output; GND is pin 10.

Variants (family.json): 5v fits U1701 = OW-PWR-TPSM365R6V5RDNR with both 22 uF output capacitors; 3v3 fits OW-PWR-TPSM365R6V3RDNR and leaves C1707 unpopulated. One schematic and one copper; the publisher writes each variant's part and DNP into its block and judges the output voltage and capacitor ratings from the facts (release.json). Output accuracy is +/-1.5 % in forced PWM (5 V facts).

MODE/SYNC (pin 11) is tied to VCC (the internal LDO output, pin 8, bypassed by C1705 1 uF), which selects forced PWM. BOOT (pin 7) is left open and the two SW pins (5, 6) are tied only to each other, as the block was drawn and built: the module integrates its inductor and nothing external connects there.

PGOOD (pin 1) is the module's open-drain window comparator: high once VOUT is inside the window (rising at about 107 %, falling at about 94 % of the set point, 25 us deglitch, about 2 ms delay after regulation), pulled up to VOUT by R1701 (10 k), so its high level is the output voltage itself (5 V or 3.3 V) and a 3.3 V host reads the 5 V variant's PGOOD only through a 5 V-tolerant input.

Bypass: three 1 uF 100 V 1206 capacitors (C1701 to C1703) and a 100 nF 0603 (C1704) at VIN; the 22 uF output capacitors sit at about 50 % (5 V) and 33 % (3.3 V) of their rating, inside the family's 0.6 planning fraction. Current limits from the facts: high-side short-circuit 1 A typical, low-side 0.7 A typical.

The placing board provides the VIN entry on its own class (the block's PWR_HV_LOCAL copper is block-local), a load of at most 600 mA, its own name for the VOUT net (the port is VOUT because the variant sets the voltage) and the thermal path: RthJA 56.3 C/W on a JEDEC 4-layer board, so give the module's pad a ground pour and vias.

DESIGN CONTRACT

High-voltage input to a fixed 5 V or 3.3 V rail: TI TPSM365R6V5 or V3 600 mA buck module, one family source with the regulator part and the second output capacitor as the variant

Circuit and PCB layout guidance
Migrated from the saved family core; circuit, variants and PCB unchanged
Orb Weaver

Sheet: /hv_to_5v_tpsm365r6/
File: hv_to_5v_tpsm365r6.kicad_sch

Title: TPSM365R6 fixed-output buck family

Size: A3	Date: 2026-10-04	**Rev: Source migration 1**
KiCad E.D.A. 10.0.6		Id: 17/20

1. Buck module and output capacitors

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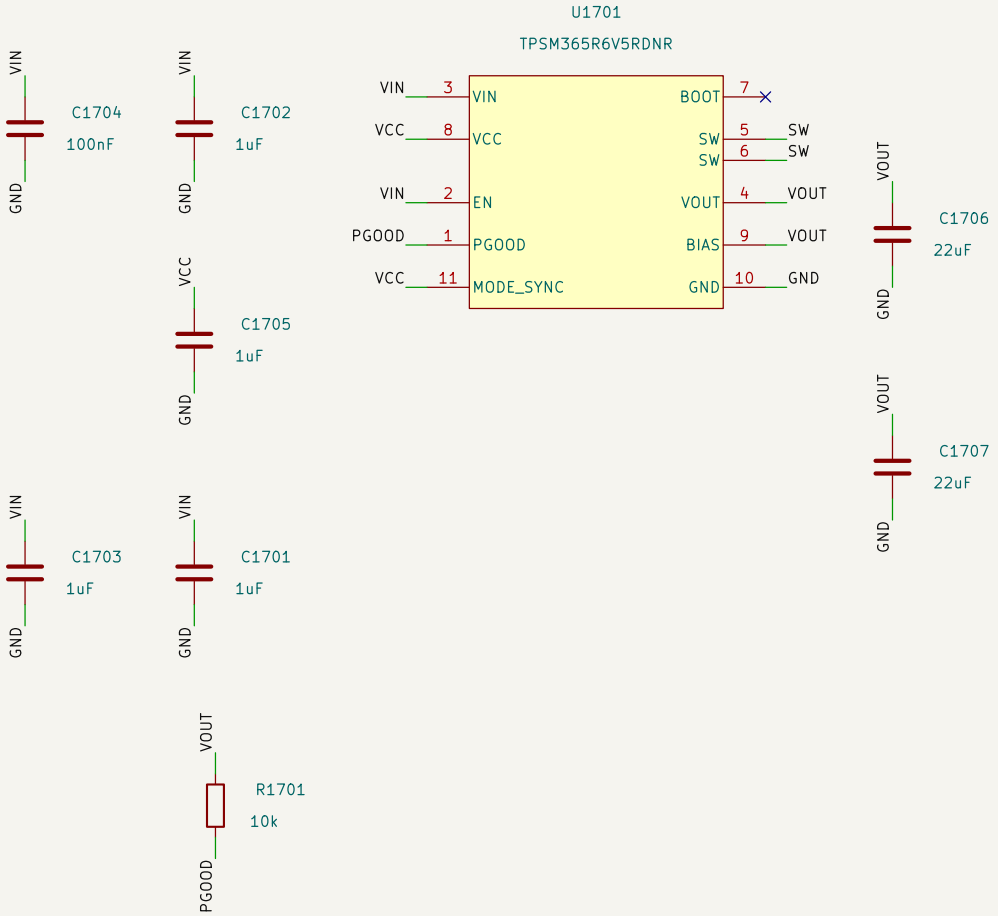

regulator
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INTERFACES

3.6 to 65 V input on VIN (pin 3) and EN (pin 2, tied: always enabled).

Fixed 5 V or 3.3 V output by variant, 600 mA; FB/BIAS (pin 9) tied here.

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Open-drain power good, pulled up to VOUT by R1701 (10 k); high level is VOUT.

INTERNAL NETS

VCC: Internal LDO output (pin 8), bypassed by C1705; MODE/SYNC (pin 11) tied here selects forced PWM.

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MODE/SYNC (pin 11) is tied to VCC (the internal LDO output, pin 8, bypassed by C1705 1 uF), which selects forced PWM. BOOT (pin 7) is left open and the two SW pins (5, 6) are tied only to each other, as the block was drawn and built: the module integrates its inductor and nothing external connects there.

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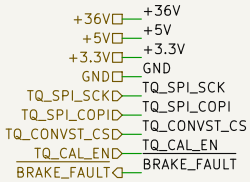
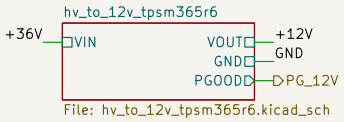
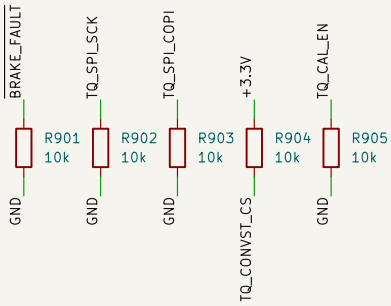
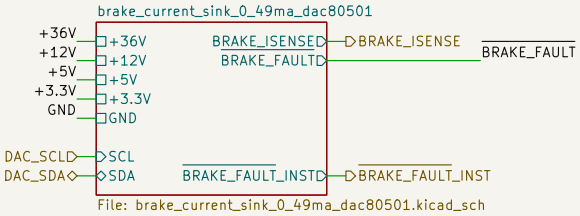
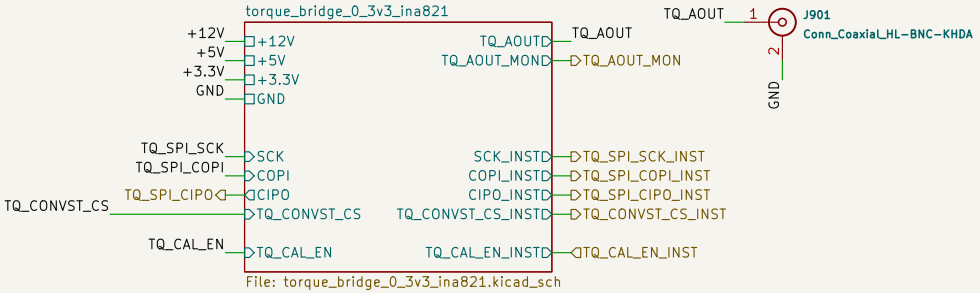
High-voltage input to a fixed 5 V or 3.3 V rail: TI TPSM365R6V5 or V3 600 mA buck module, one family source with the regulator part and the second output capacitor as the variant











Janelia Research Campus		
Sheet: /brake_torque_sensor/		
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Title: mouse-joystick-pcb		
Size: A4	Date: 2026-09-19	**Rev: 1.0**
KiCad E.D.A. 10.0.6		Id: 9/20

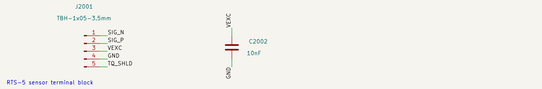
Torque bridge | circuit, review points and PCB guidance

RTS-5 bridge front end: 10 V excitation, INA821 gain 191.734, filtered full-scale ADC path and separate half-scale analog output.

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Sensor connector and calibration review

Actual J2001 pinout: 1 SIG_N (white), 2 SIG_P (green), 3 VEXC (red), 4 GND (black), 5 shield. R2009 is the fitted 0 ohm shield tie. R2003/Q2001 are intended to shunt a bridge arm for calibration. CRITICAL REVIEW: Q2001 source is SIG_N, about 5 V. A ground-referenced 3.3 V gate gives Vgs about −1.7 V, so it cannot enable this N-channel FET as documented. No gate pull-down exists in this netlist.



RTS-5 sensor terminal block

VEXC input filter, 10 nF C0G

Shunt-calibration resistor, 75 k

TQ_CAL_EN_INST instrument tap, 1 k

Shunt-calibration switch FET

Shield tie to GND, 0 R

PLACE: Put input filtering beside J2001. Keep the shield tie at its ground pin.

ROUTE: Route SIG_P/SIG_N together with symmetric exposure to interference. Bring bridge −EXC back separately from noisy load returns.

2. 10 V reference and excitation servo

REF5010 supplies VREF10. U2003 drives Q2002 through R2013; the emitter feeds VEXC through 10 ohm R2014. Feedback senses VEXC after that resistor. A 350 ohm bridge draws 28.6 mA (286 mW). R2019 pulls an open reference low.

REF5010 Vin bypass, 100 nF

Error amp U2003 V+ bypass, 100 nF

REF5010 10 V reference

Excitation error amplifier

Q2002 base resistor, 1 k

Excitation pass transistor

Reference output capacitor, 1 uF

VREF10 open-reference pull-down

Excitation isolation, 10 R

PLACE: Keep reference / error amp together; separate pass-device heat from precision ratios. C2010 bypasses U2004; C2007 bypasses U2003.

ROUTE: Kelvin-route U2003.4 to VEXC at J2001.3. Sensing VEXC_DRV would leave the approximately 286 mV bridge-current drop uncompensated.

ROUTE: VEXC_B is the base node after R2013; VEXC_BASE is the op-amp output. Check loop stability with the actual cable and bypass load.

3. Differential input filter and instrumentation gain

Matched 1k input legs with 470 pF shunts and 10 nF differential C2008 reject cable pickup. INA821 gain is 1 + 49.4k/(249+10) = 191.734. VMID sets the zero-torque output to 5 V.

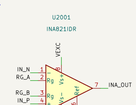
SIG_N input filter leg, 1 k

IN_N shunt, 470 pF C0G

INA821 gain resistor, 249 R 0.1%

INA821 V+ bypass (VEXC), 100 nF

IN_P to IN_N differential, 10 nF C0G



INA821 Instrumentation amplifier

SIG_P input filter leg, 1 k

IN_P shunt, 470 pF C0G

INA821 gain trim, 10 R

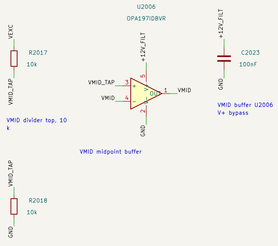
PLACE: Keep paired filter parts symmetric and close to the INA inputs; put R2001/R2002 beside gain pins 2/3. C2001 bypasses U2001.8.

ROUTE: U2001.8 must remain on VEXC. Moving it to +12V_FILT changes the output ceiling while passing ERC.

ROUTE: Keep IN_P/IN_N and the gain loop short, away from clocks, pass-translator current and switching nodes; use C0G for the signal capacitors.

4. Ratiometric 5 V midpoint

The equal 10k divider generates VMID_TAP = VEXC/2; U2006 buffers it onto VMID and the INA821 reference pin. C2023 bypasses the buffer supply.



VMID divider top, 10 k

VMID midpoint buffer

VMID divider bottom, 10 k

VMID buffer U2006 V+ bypass

PLACE: Use R2017/R2018 from the same precision-resistor reel as R2006/R2007/R2008; keep matched resistors at similar temperature.

PLACE: Put C2023 at U2006.5 (V+) with its GND end at pin 2 (V−).

ROUTE: Keep VMID_TAP local and clean. Route buffered VMID directly to U2001.6; avoid load and shield return currents at the divider ground.

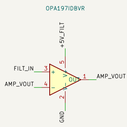
5. One-third attenuation, low-pass filter and buffer

Two series 10k resistors above ATT_TAP and one 10k below give DC gain 1/3. C2004 and C2006 are 10 nF C0G; R2010 is 13k. U2005 buffers FILT_IN onto AMP_VOUT: R2015 discharges its output. Ideal filter: −3 dB about 690 Hz, DC group delay about 263 us. Retune both capacitors together; resistor changes also change the mapping.

ADC /3 divider top, INA_OUT side, 10 k

ADC /3 divider top, ATT_TAP side, 10 k

Low-pass filter series, 13 k



Filter output buffer

ADC /3 divider bottom, 10 k

ATT_TAP filter shunt, 10 nF C0G

FILT_IN filter shunt, 10 nF C0G

AMP_VOUT discharge, 100 k

PLACE: Cluster the divider and filter beside U2005. Keep the three precision 10k parts thermally close. Put C2009 at U2005.5.

ROUTE: Keep ATT_TAP/FILT_IN copper short and free of digital coupling. Limit stray capacitance under these high-impedance nodes.

6. Half-scale analog output and monitor

Matched 3.2k R2016/R2020 divide AMP_VOUT by two. C2022 is 470 pF C0G (about 0.75 us added RC delay). TQ_AOUT leaves through 249 ohm R2021; the monitor leaves through 1k R2022.

Output /2 divider top, 3.2 k

TQ_AOUT series resistor, 249 R

TQ_AOUT_MON monitor tap, 1 k

Output /2 divider bottom, 3.2 k

TQ_AOUT_DIV midpoint shunt, 470 pF

TQ_AOUT ESD clamp

PLACE: Place the matched pair together. Put D2001 at the external-output entry/connector with a short return to its ground; the BNC is outside this block.

ROUTE: D2001 must share TQ_AOUT with the BNC pin, after R2021. The ESD return must not cross sensitive analog ground paths.

ROUTE: Output source resistance is 1.6k + 249 = 1.849 kohm; a 1 Mohm load costs about 0.185% gain. Leave ADC_IN on AMP_VOUT, not this divider midpoint.

7. Full-amplitude ADC and its references

ADS8689 AIN_P reads AMP_VOUT through 249 ohm R2023. Its approximately 1 Mohm, range-dependent input resistance would disturb the half-scale divider if connected there. R2011 pulls reset high; R2012 is the inherited CIPO pull-down.

ADC_IN series resistor, 249 R

ADS8689 16-bit SAR ADC

RST pull-up, 10 k

CIPO pull-down, 10 k (inherited)

ADC REFIO capacitor, 10 uF

ADC REFCAP capacitor, 10 uF

ADC REFCAP bypass, 1 uF, nearest pin

PLACE: Put C2018 at AVDD and C2019/C2020 at DVDD. Put C2011 at REFIO; C2014/C2017 at REFCAP, with C2017 nearest the pin.

ROUTE: Use short reference-capacitor return loops and a continuous low-impedance local ground. Keep serial edges away from ADC_IN and both reference nodes.

ROUTE: REFIO/REFCAP serve this ADC only. Pins 14/15 are intentionally no-connect. CONVST_CS rising edge samples; falling edge starts the serial frame.

ADC AVDD bypass, 100 nF

ADC DVDD bypass, 1 uF

ADC DVDD bypass, 100 nF

8. Digital observation taps and bus ownership

100 ohm resistors isolate the SCK, CIPO, COPI and TQ_CONVST_CS monitor branches. The current circuit has no TQ_CONVST_CS pull-up. R2028 in group 1 similarly isolates the calibration-gate tap with 1k. INHERITED REVIEW: the shared SCK/CIPO/COPI taps and the CIPO pull-down belong once on the placing board: multiple copies parallel these loads. Keep this issue visible when reusing the block.

SCK Instrument tap, 100 R

CIPO Instrument tap, 100 R

COPI Instrument tap, 100 R

CONVST_CS Instrument tap, 100 R

PLACE: Place each tap resistor at its branch origin. Keep the main serial path direct; route observation branches toward the instrument connector.

9. Filtered analog rails

FB2001 feeds +12V_FILT for the reference, excitation servo and midpoint buffer. FB2002 feeds +5V_FILT for the ADC and output buffer. Each filtered rail has 10 uF bulk plus 100 nF; per-IC bypass stays with its functional group.

+12V rail ferrite

+12V_FILT rail bulk, 10 uF

+12V_FILT rail bypass, 100 nF

+5V rail ferrite

+5V_FILT rail bulk, 10 uF

+5V_FILT rail bypass, 100 nF

Output buffer U2005 V+ bypass

PLACE: Place bulk/bypass immediately after each ferrite at the block supply entry; keep high-current switching circuitry remote.

ROUTE: Keep the loop from each ferrite through its 10 uF and 100 nF to GND short.

10. Power drive declarations

These nets have an explicit ERC power source declaration.

Power driven: +12V_FILT

Power driven: +5V_FILT

Power driven: VEXC

INTERFACES

+12VD — +12V

Switched excitation / reference supply; keep above 10.75 V.

+5VD — +5V

Switched ADC analog / output-buffer supply.

+3.3VD — +3.3V

Switched ADC digital supply; also biases reset high.

GNDD — GND

Common return; keep bridge and shield currents out of input returns.

TQ_CAL_ENO — TQ_CAL_EN

Calibration FET gate; drive needs review (see group 1). No gate pull-down fitted.

SCKD — SCK

Host serial clock to ADC.

COPIO — COPI

Host serial data input to ADC.

CIPOI — CIPO

ADC serial data output; inherited 10k pull-down present.

TQ_CONVST_CSO — TQ_CONVST_CS

ADC conversion / chip select; board must define idle state.

TQ_AOUTO — TQ_AOUT

Half-scale analog output to external BNC; load >=1 Mohm, no 50 ohm termination.

TQ_AOUT_MONO — TQ_AOUT_MON

Half-scale divider monitor through 1k; high-impedance probe.

SCK_INSTO — SCK_INST

100 ohm isolated clock monitor; shared-bus ownership issue.

COPI_INSTO — COPI_INST

100 ohm isolated data-in monitor; shared-bus ownership issue.

CIPO_INSTO — CIPO_INST

100 ohm isolated data-out monitor; shared-bus ownership issue.

TQ_CONVST_CS_INSTO — TQ_CONVST_CS_INST

100 ohm isolated conversion / chip-select monitor.

TQ_CAL_EN_INSTO — TQ_CAL_EN_INST

1k isolated calibration-gate monitor.

OPERATION

Signal path: SIG_P/SIG_N -> IN_P/IN_N -> INA_OUT -> ATT_TAP -> FILT_IN -> AMP_VOUT. ADC_IN reads full amplitude; TQ_AOUT and TQ_AOUT_MON read half amplitude.

Ideal DC: INA_OUT = VEXC/2 + 191.734 x (SIG_P − SIG_N); AMP_VOUT = INA_OUT/3; unloaded TQ_AOUT = AMP_VOUT/2.

At 10 V excitation, zero torque is 1.6667 V at AMP_VOUT and 0.8333 V at TQ_AOUT. Nominal +/−1.5 mV/V rated bridge output gives 0.3540−1.3127 V at TQ_AOUT.

With the 1.577 mV/V sensor certificate, ideal +/−150% overload gives 0.0774−1.5892 V at TQ_AOUT. These are calculated values before tolerances and loading.

Configure ADS8689 for 0−5.12 V: allow 20 ms for its reference, then allow bridge thermal settling. Fit ADC and analog-output calibration separately for each sensor / board / cable: tare before trials.

The 1.642 V level is the documented upstream INA-limited ceiling, not a universal fault clamp. A buffer output short to a +5 V rail at +2% gives about 2.55 V after division; the ESD diode does not limit DC faults.

PCB PLACEMENT / ROUTING

Place sensor connector -> input filter / INA821 -> RC filter / buffer -> analog output along a quiet edge. Place the ADC toward the digital side.

Keep motor/brake copper and the 12 V switching loop remote. Return bridge excitation and shield at the connector; do not share their current paths with input/filter returns.

VERIFY

As-drawn issues: no calibration gate pull-down or chip-select pull-up. R2012 and R2024/R2025/R2026 load or tap shared SPI lines: resolve board ownership before reuse.

Verify harness pinout against J2001 on this sheet. Historical pin tables and GPIO calibration claims do not match this circuit.

Bench-check excitation-loop stability with the real cable, switcher pickup, calibration switching, polarity and output loading. Connectivity checks do not establish analog performance.

Declare supply drive for +12V, +5V and +3.3V at the board/harness boundary for ERC: the ferrites and Q2002 interrupt driver propagation, so the block flags +12V_FILT, +5V_FILT and VEXC itself. Put separate block instances on separate hierarchical sheets so their local nets do not merge.

DESIGN NOTES

Source migration preserves the existing circuit and routed PCB. Review the calibration-drive and SPI ownership limitations before reuse.

Original connector notes: −SIG (WHITE); +SIG (GREEN); +EXC (RED); −EXC (BLACK); SHIELD. J2001 pin mapping is documented in section 1.

DESIGN CONTRACT

Single-channel torque sensor front end for a Transducer Techniques RTS-5 reaction bridge (350 ohm, 1.5 mV/V, 5 lb-oz), giving a nominal 0.3540−1.3127 V ground-referenced rated-range analog output for a Neuropixels OneBox ADC channel, plus an on-board ADS8689 that streams the same conditioned signal at FULL amplitude. At the BNC, zero torque is nominally 0.8333 V; the fitted 259 ohm gain resistance gives INA821 gain 191.734. At 1.5 mV/V, +/−rated spans 0.3540−1.3127 V. The 1.577 mV/V sensor certificate at +/−150% overload predicts 0.0774−1.5892 V before tolerances. The ADC sees twice the unloaded BNC amplitude.
FULL DERIVATION, VALUES, LAYOUT RULES AND OPEN ITEMS ARE IN kicad-libs docs/torque-sensor-interface-design.md. This note carries only what breaks silently without it. Designators have changed across annotations; so the invariants below are also identified by NET.
1. EVERYTHING THAT LEAVES THE BOARD IS HALVED: THE ON-BOARD ADC IS NOT. A /2 divider (two 3.2k 0.1% 25ppm/C plus a 470 pF C0G midpoint shunt) sits in the TQ_AOUT leg only, between AMP_VOUT and the 249 ohm BNC resistor. TQ_AOUT_MON taps the divider midpoint so the scope trace reads what the BNC delivers. ADC_IN taps AMP_VOUT, so the MCU record and the OneBox record differ by exactly 2 and need TWO calibration constants. AMP_VOUT is the single reference node for both.
2. THE ADC's TAP MUST NOT MOVE TO THE MIDPOINT, and this is not obvious. The ADS8689's AIN_P is a RESISTIVE input, 1 Mohm +/−15% and range-programmable between 1 MOhm and 1.2 MOhm — not a buffered high-Z input. On the midpoint it parallels the 3.2k bottom leg and becomes part of the ratio: BNC loading goes from −0.185% to −0.344%; the converter's input bias puts about +2.6 mV on the BNC (0.018 N.cm, ten times the sensor's 0.0018 N.cm nonrepeatability); and a firmware write changing the ADC's input range silently re-scales the OneBox reading. The bound the divider exists for does not apply to ADC_IN anyway: it never leaves the board, the ADC's range is 0−5.12 V, and its input protection is +/−20 V powered.
3. THE INA821's +VS BINDS TO VEXC, NOT +12V_FILT. That limits the INA821-driven pre-divider ceiling to about 3.283 V, or 1.642 V after division. It is NOT a universal output fault clamp: a downstream +5 V buffer rail fault at +2% can give about 2.55 V after division, and the ESD device does not clamp DC. Check the receiving input limits independently. Both nets are 10−12 V, both 'work', and ERC passes either way.
4. THE EXCITATION LOOP FEEDS BACK FROM VEXC AT THE CONNECTOR PIN, not from the emitter or the base node. From the emitter the 10 ohm isolation resistor's 286 mV drop goes uncorrected, a 2.9% sensitivity error. The 100k pull-down on VREF10 is what makes an open reference fail LOW instead of driving the ceiling to the 12 V rail.
5. TQ_AOUT, TQ_AOUT_MON AND ADC_IN ARE THREE DIFFERENT NETS AT TWO DIFFERENT SCALES. TQ_AOUT is the delivered output and carries the 249 ohm source resistor and the ESD clamp; verify on the netlist that the clamp shares a net with the connector pin. This was got wrong once already, on mouse-joystick-pcb.
6. TQ_AOUT HAS AN INA821-LIMITED CEILING OF ABOUT 1.642 V FROM A 1.849 kohm SOURCE AND NEEDS A >=1 Mohm LOAD. The source is the 249 ohm series resistor PLUS the divider's 1.6 kohm, not 249 ohm alone — against the OneBox A07616-P's 1 Mohm that is −0.185% of gain, systematic and absorbed by per-board calibration, but a 100 kohm load costs −1.82% and a 50 ohm terminated input reads a fraction of the correct value. The 249 ohm bounds a short of TQ_AOUT to ground at 6.6 mA and 11 mW inside a 62.5 mW 0402. The ESD clamp is a transient device and does NOT bound a DC fault.
7. THE RATIO RESISTORS ARE TWO SEPARATE MATCHED SETS AND THE BLOCK ALSO CONTAINS DECOYS. FIVE 10.0k ERA2AEB103X from one reel -- two for the /2 VMID midpoint, two in series for the /3 ADC divider top, one for its bottom. TWO 3.2k RT0402BRD073K2L from one reel for the output /2 divider. The block's two generic 10k pulls (R2011 reset pull-up, R2012 CIPO pull-down) are also 10k, and there are THREE 249 ohm parts -- the BNC series resistor, the ADC series resistor, and the 0.1% RG gain resistor. Identify every one of them by NET, never by value or by designator adjacency.
8. THE FILTER CAPACITORS MUST BE C0G, AND SO MUST THE 470 pF DIVIDER MIDPOINT SHUNT. Retune the filter by scaling BOTH capacitors by the same factor; the resistors set the DC gain and the whole magpiing. Its 263 us group delay is deliberately matched to analog_output_0_3v3_dac80501 v 266 us. The midpoint shunt is 470 pF because it adds only 0.75 us against that budget; 10 nF would add 16 us. Class-2 dielectric is piezoelectric. this board is coupled to a stepper and a hand-driven joystick, and on the divider midpoint that pickup becomes signal. A mechanically generated torque artifact in a torque measurement cannot be filtered out.
9. SPI: the saved circuit has a 10k pull-down on CIPO (SDO) and no fitted pull-up on TQ_CONVST_CS. Shared-bus idle termination belongs to the BOARD; repeated blocks duplicate the inherited CIPO pull and SCK/CIPO/COPI instrument taps. Resolve this ownership issue before reuse. The placing board defines SCK and COPI on the peripheral side of the default-open SN74CB3Q3245; the RP2040 end uses its own pad pull-downs.
10. SHUNT CALIBRATION IS NOT VERIFIED: TQ_CAL_EN drives the Q2001 gate directly, with no fitted gate pull-down: the only series part on that port is the 1k R2028 feeding the TQ_CAL_EN_INST tap. Its source is SIG_N, nominally near 5 V, so a 3.3 V GPIO cannot provide positive VGS. Arrange an appropriate drive and reset-safe gate bias in a separately reviewed circuit revision before relying on shunt calibration. It is a static enable, not an edge worth a logic-analyzer channel.
11. PWR_FLAG on +12V_FILT, +5V_FILT and VEXC is required, because ferrites and a pass translator break driver propagation. GND is flagged once at board level, not here. Expect ERC to want one on the ADC's REFCAP and REFIO too: the official-derived symbol types REFCAP as power_in, matching upstream. Not a defect.
12. Bind +12V, +5V and +3.3V all to the SWITCHED domain. 0 V and the INA821-limited 1.642 V ceiling are out-of-band fault indications: other faults can exceed that ceiling. Two instances need separate sheets or their local nets merge.
13. CALIBRATION IS PER SENSOR AND PER BOARD, and the two channels are NOT interchangeable -- pair each sensor with a board serial and move its certificate constant with it. Fit the BNC and the ADC paths separately: do not derive one from the other by a factor of 2, because the divider's own 0.1% tolerance is part of the BNC gain. The sensor is the limit either way: 0.05% nonrepeatability is 0.001765 N.cm, which is 249 uV at the BNC after the divider (1.6 OneBox codes) and 6.4 LSB at the ADC's 78.125 uV.

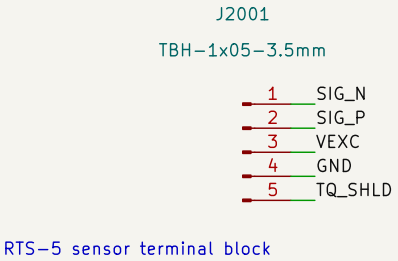
Circuit and PCB layout guidance
RTS-5 / INA821 / ADS8689
Orb Weaver
Sheet: /brake_torque_sensor/torque_bridge_0_3v3_ina821/
File: torque_bridge_0_3v3_ina821.kicad_sch

Title: Torque bridge Interface

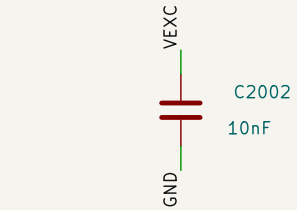
Size: A1	Date: 2026-10-04	Rev: Source migration 1
KiCad E.D.A. 10.0.6		Id: 20/20

1. Sensor connector and calibration review

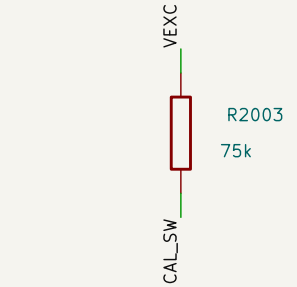
Actual J2001 pinout: 1 SIG_N (white), 2 SIG_P (green), 3 VEXC (red), 4 GND (black), 5 shield. R2009 is the fitted 0 ohm shield tie. R2003/Q2001 are intended to shunt a bridge arm for calibration. CRITICAL REVIEW: Q2001 source is SIG_N, about 5 V. A ground-referenced 3.3 V gate gives Vgs about −1.7 V, so it cannot enable this N-channel FET as documented. No gate pull-down exists in this netlist.



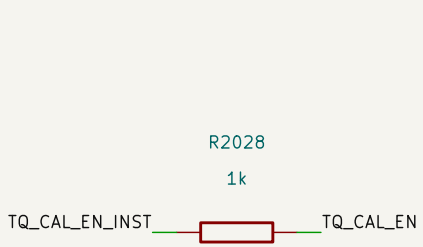
RTS-5 sensor terminal block



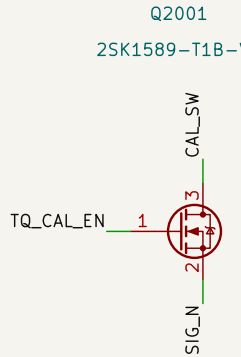
VEXC input filter, 10 nF C0G



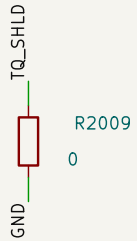
Shunt-calibration resistor, 75 k



TQ_CAL_EN_INST instrument tap, 1 k



Shunt-calibration switch FET



Shield tie to GND, 0 R

PLACE: Put input filtering beside J2001. Keep the shield tie at its ground pin.

ROUTE: Route SIG_P/SIG_N together with symmetric exposure to interference. Bring bridge −EXC back separately from noisy load returns.

2. 10 V refere

REF5010 supplies
mA (286 mW). R2

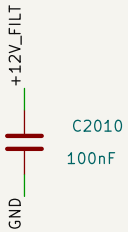
REF5010 Vin

REF5010 10

Reference ou

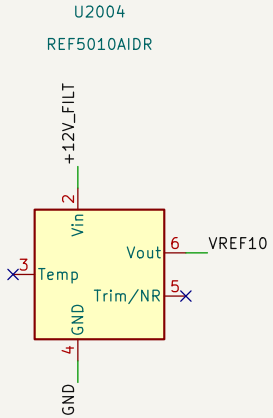
2. 10 V reference and excitation servo

REF5010 supplies VREF10. U2003 drives Q2002 through R2013; the emitter feeds VEXC through 10 ohm R2014. Feedback senses VEXC after that resistor. A 350 ohm bridge draws 28.6 mA (286 mW). R2019 pulls an open reference low.

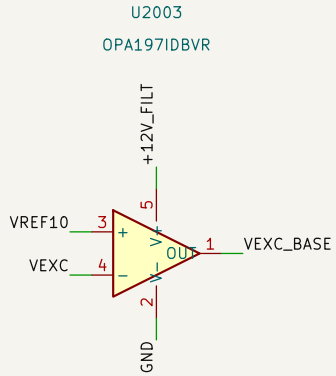


REF5010 Vin bypass, 100 nF

Error amp U2003 V+ bypass, 100 nF

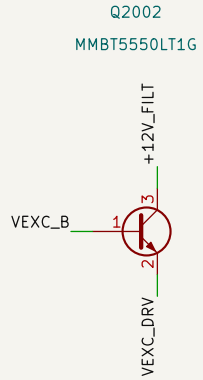


REF5010 10 V reference

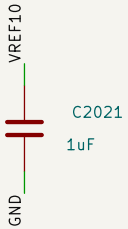


Excitation error amplifier

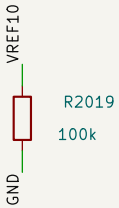
Q2002 base resistor, 1 k



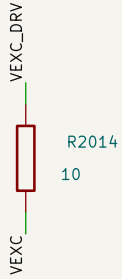
Excitation pass transistor



Reference output capacitor, 1 uF



VREF10
open−reference
pull−down



Excitation isolation, 10 R

PLACE: Keep reference / error amp together; separate pass−device heat from precision ratios. C2010 bypasses U2004; C2007 bypasses U2003.

ROUTE: Kelvin−route U2003.4 to VEXC at J2001.3. Sensing VEXC_DRV would leave the approximately 286 mV bridge−current drop uncompensated.

ROUTE: VEXC_B is the base node after R2013; VEXC_BASE is the op−amp output. Check loop stability with the actual cable and bypass load.

3. Differential input filter and instru

Matched 1k input legs with 470 pF shunts ar
output to 5 V.

SIG_N input filter leg, 1 k

SIG_P input filter leg, 1 k

PLACE: Keep paired filter parts symmetric an

ROUTE: U2001.8 must remain on VEXC. Movin

ROUTE: Keep IN_P/IN_N and the gain loop sh

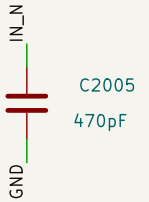
5. One−third attenuation, low−pass

Two series 10k resistors above ATT_TAP and

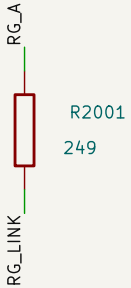
3. Differential input filter and instrumentation gain

Matched 1k input legs with 470 pF shunts and 10 nF differential C2008 reject cable pickup. INA821 gain is 1 + 49.4k/(249+10) = 191.734. VMID sets the zero-torque output to 5 V.

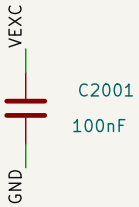
SIG_N input filter leg, 1 k



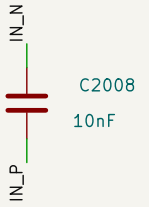
IN_N shunt, 470 pF C0G



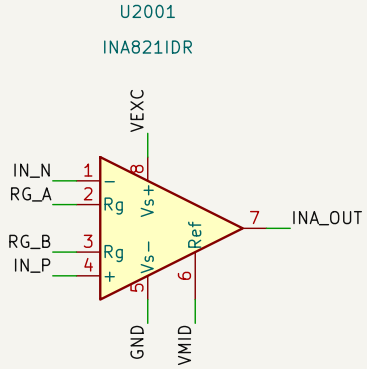
INA821 gain resistor, 249 R 0.1%



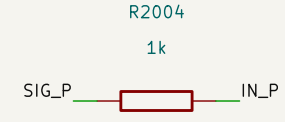
INA821 Vs+ bypass (VEXC), 100 nF



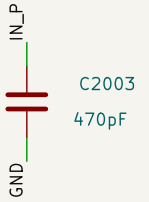
IN_P to IN_N differential, 10 nF C0G



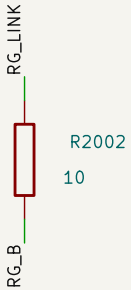
INA821 instrumentation amplifier



SIG_P input filter leg, 1 k



IN_P shunt, 470 pF C0G



INA821 gain trim, 10 R

PLACE: Keep paired filter parts symmetric and close to the INA inputs; put R2001/R2002 beside gain pins 2/3. C2001 bypasses U2001.8.

ROUTE: U2001.8 must remain on VEXC. Moving it to +12V_FILT changes the output ceiling while passing ERC.

ROUTE: Keep IN_P/IN_N and the gain loop short, away from clocks, pass-transistor current and switching nodes; use C0G for the signal capacitors.

INTERFACES

+12V +12V

Switched excitation /

+5V +5V

Switched ADC analog

+3.3V +3.3V

Switched ADC digital

GND GND

Common return; keep

TQ_CAL_EN TQ_

Calibration FET gate;

SCK SCK

Host serial clock to

COPI COPI

Host serial data inpu

CIPO CIPO

ADC serial data outp

TQ_CONVST_CS

ADC conversion / ch

TQ_AOUT TQ_

Half-scale analog ou

TQ_AOUT_MON

Half-scale divider m

SCK_INST SCI

100 ohm isolated clo

COPI_INST CO

100 ohm isolated da

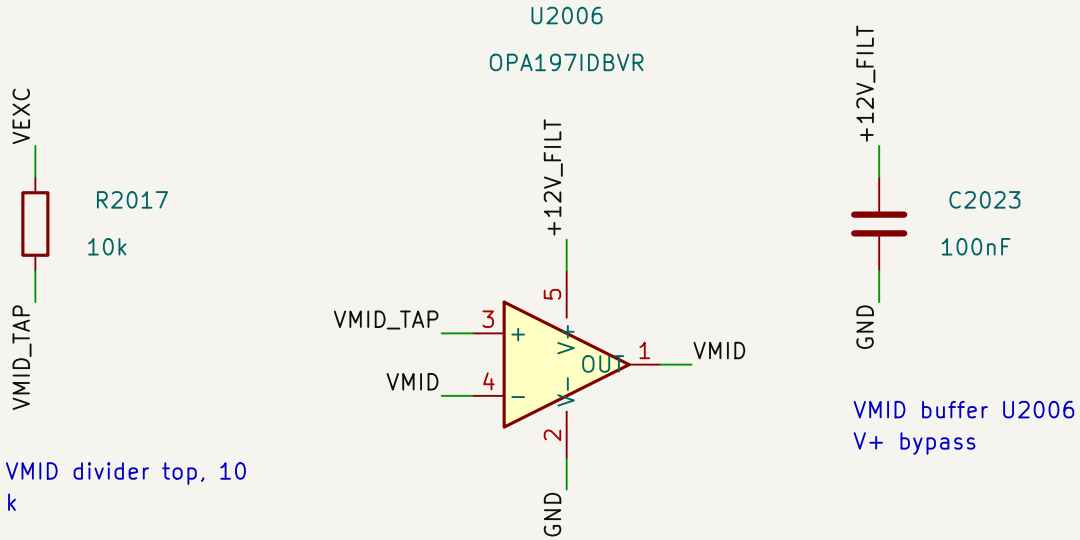
CIPO_INST CIP

100 ohm isolated da

TQ_CONVST_CS_I

4. Ratiometric 5 V midpoint

The equal 10k divider generates VMID_TAP = VEXC/2; U2006 buffers it onto VMID and the INA821 reference pin. C2023 bypasses the buffer supply.



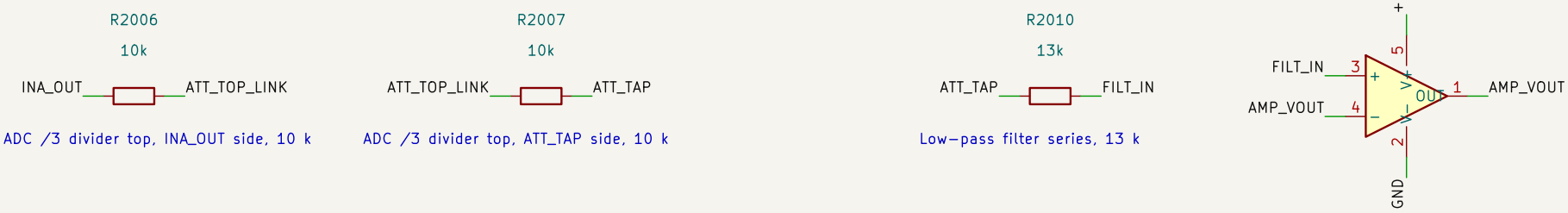
PLACE: Use R2017/R2018 from the same precision−resistor reel as R2006/R2007/R2008; keep matched resistors at similar temperature.

PLACE: Put C2023 at U2006.5 (V+) with its GND end at pin 2 (V−).

ROUTE: Keep VMID_TAP local and clean. Route buffered VMID directly to U2001.6; avoid load and shield return currents at the divider ground.

5. One-third attenuation, low-pass filter and buffer

Two series 10k resistors above ATT_TAP and one 10k below give DC gain 1/3. C2004 and C2006 are 10 nF C0G; R2010 is 13k. U2005 buffers FILT_IN onto AMP_VOUT; R2015 discharges its output. Ideal filter: −3 dB about 690 Hz, DC group delay about 263 us. Retune both capacitors together; resistor changes also change the mapping.

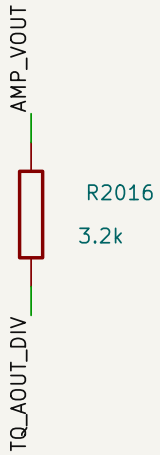


PLACE: Cluster the divider and filter beside U2005. Keep the three precision 10k parts thermally close. Put C2009 at U2005.5.

ROUTE: Keep ATT_TAP/FILT_IN copper short and free of digital coupling. Limit stray capacitance under these high-impedance nodes.

6. Half-scale analog output and monitor

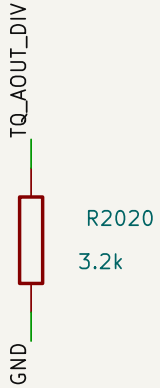
Matched 3.2k R2016/R2020 divide AMP_VOUT by two. C2022 is 470 pF C0G (about 0.75 us added RC delay). TQ_AOUT leaves through 249 ohm R2021; the monitor leaves through 1k R2022.



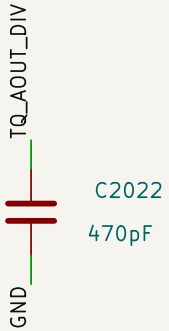
Output /2 divider top, 3.2 k

TQ_AOUT series resistor, 249 R

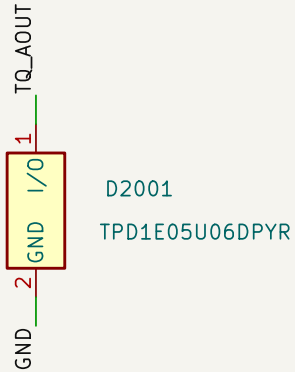
TQ_AOUT_MON monitor tap, 1 k



Output /2 divider bottom, 3.2 k



TQ_AOUT_DIV midpoint shunt, 470 pF



TQ_AOUT ESD clamp

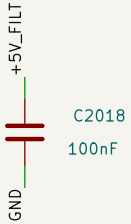
PLACE: Place the matched pair together. Put D2001 at the external-output entry/connector with a short return to its ground; the BNC is outside this block.

ROUTE: D2001 must share TQ_AOUT with the BNC pin, after R2021. The ESD return must not cross sensitive analog ground paths.

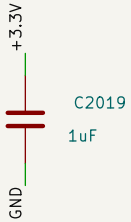
ROUTE: Output source resistance is 1.6k + 249 = 1.849 kohm: a 1 Mohm load costs about 0.185% gain. Leave ADC_IN on AMP_VOUT, not this divider midpoint.

7. Full-amplitude ADC and its references

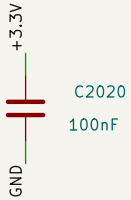
ADS8689 AIN_P reads AMP_VOUT through 249 ohm R2023. Its approximately 1 Mohm, range-dependent input resistance would disturb the half-scale divider if connected there. R2011 pulls reset high; R2012 is the inherited CIPO pull-down.



ADC AVDD bypass, 100 nF

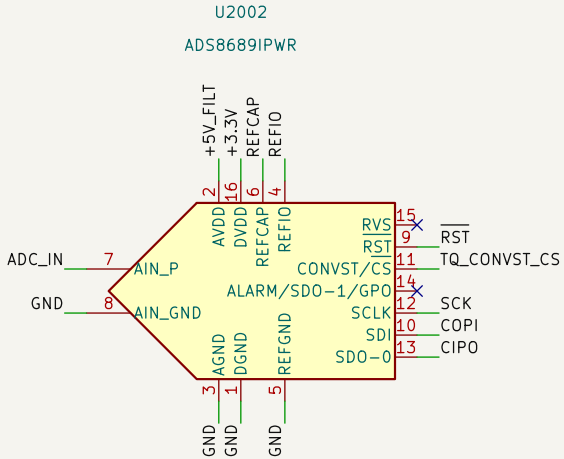


ADC DVDD bypass, 1 uF



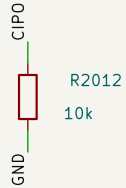
ADC DVDD bypass, 100 nF

ADC_IN series resistor, 249 R

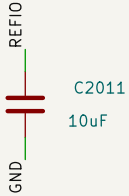


ADS8689 16-bit SAR ADC

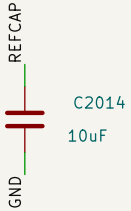
$\overline{\text{RST}}$ pull-up, 10 k



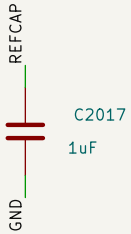
CIPO pull-down, 10 k (inherited)



ADC REFIO capacitor, 10 uF



ADC REFCAP capacitor, 10 uF



ADC REFCAP bypass, 1 uF, nearest pin

PLACE: Put C2018 at AVDD and C2019/C2020 at DVDD. Put C2011 at REFIO; C2014/C2017 at REFCAP, with C2017 nearest the pin.

ROUTE: Use short reference-capacitor return loops and a continuous low-impedance local ground. Keep serial edges away from ADC_IN and both reference nodes.

ROUTE: REFIO/REFCAP serve this ADC only. Pins 14/15 are intentionally no-connect. CONVST_CS rising edge samples; falling edge starts the serial frame.

Output /2 divider bottom, 3.2 k

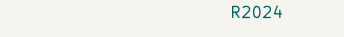
PLACE: Place the matched pair together

ROUTE: D2001 must share TQ_AOUT with

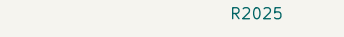
ROUTE: Output source resistance is 1.6k

8. Digital observation taps and

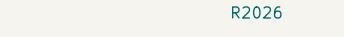
100 ohm resistors isolate the SCK, CIPO the calibration-gate tap with 1k. INHER loads. Keep this issue visible when reus



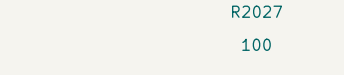
SCK instrument tap, 100 R



CIPO instrument tap, 100 R



COPI instrument tap, 100 R



CONVST_CS instrument tap, 100 R

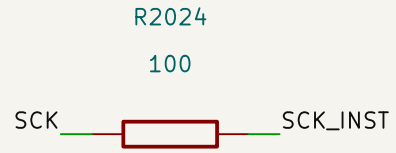
PLACE: Place each tap resistor at its br

10. Power drive declarations

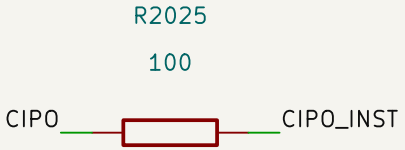
These nets have an explicit ERC power

8. Digital observation taps and bus ownership

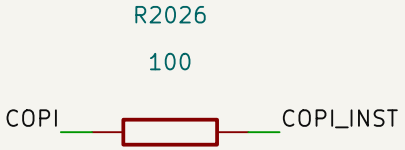
100 ohm resistors isolate the SCK, CIPO, COPI and TQ_CONVST_CS monitor branches. The current circuit has no TQ_CONVST_CS pull-up. R2028 in group 1 similarly isolates the calibration-gate tap with 1k. INHERITED REVIEW: the shared SCK/CIPO/COPI taps and the CIPO pull-down belong once on the placing board; multiple copies parallel these loads. Keep this issue visible when reusing the block.



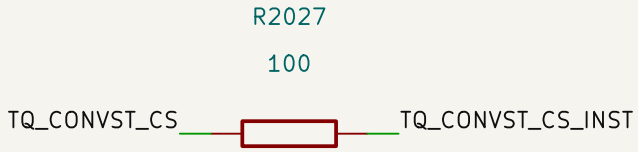
SCK instrument tap, 100 R



CIPO instrument tap, 100 R



COPI instrument tap, 100 R



CONVST_CS instrument tap, 100 R

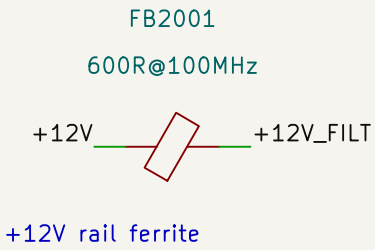
PLACE: Place each tap resistor at its branch origin. Keep the main serial path direct; route observation branches toward the instrument connector.

PLACE: Cluster the divider and filter beside U2005. Keep the three precision 10k parts thermally close. Put C2009 at U2005.5.

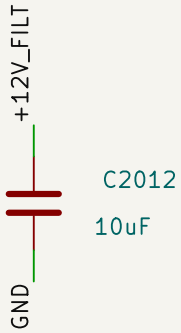
ROUTE: Keep ATT_TAP/FILT_IN copper short and free of digital coupling. Limit stray capacitance under these high−impedance nodes.

9. Filtered analog rails

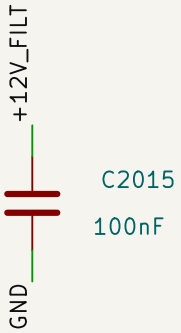
FB2001 feeds +12V_FILT for the reference, excitation servo and midpoint buffer. FB2002 feeds +5V_FILT for the ADC and output buffer. Each filtered rail has 10 uF bulk plus 100 nF; per−IC bypass stays with its functional group.



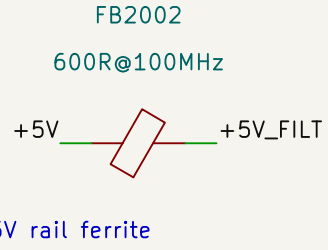
+12V rail ferrite



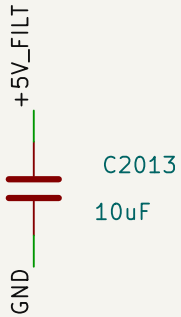
+12V_FILT rail bulk, 10 uF



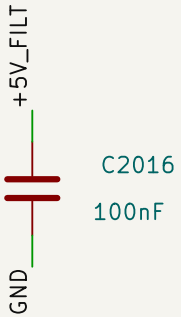
+12V_FILT rail bypass, 100 nF



+5V rail ferrite



+5V_FILT rail bulk, 10 uF



+5V_FILT rail bypass, 100 nF

PLACE: Place bulk/bypass immediately after each ferrite at the block supply entry; keep high−current switching circuitry remote.

ROUTE: Keep the loop from each ferrite through its 10 uF and 100 nF to GND short.

CIPO CIPO_INST

CIPO instrument tap, 100 R

R2026
100

COPI COPI_INST

COPI instrument tap, 100 R

R2027
100

TQ_CONVST_CS TQ_CONVST_CS_INST

CONVST_CS instrument tap, 100 R

PLACE: Place each tap resistor at its branch origin. Keep the main serial path direct; route observation branches toward the instrument connector.

---

10. Power drive declarations

These nets have an explicit ERC power source declaration.

#FLG02001
PWR_FLAG

Power driven:
+12V_FILT

#FLG02002
PWR_FLAG

Power driven:
+5V_FILT

#FLG02003
PWR_FLAG

Power driven: VEXC

INTERFACES

+12V — +12V

Switched excitation / reference supply; keep above 10.75 V.

+5V — +5V

Switched ADC analog / output-buffer supply.

+3.3V — +3.3V

Switched ADC digital supply; also biases reset high.

GND — GND

Common return; keep bridge and shield currents out of input returns.

TQ_CAL_EN — TQ_CAL_EN

Calibration FET gate; drive needs review (see group 1). No gate pull-down fitted.

SCK — SCK

Host serial clock to ADC.

COPI — COPI

Host serial data input to ADC.

CIPO — CIPO

ADC serial data output; inherited 10k pull-down present.

TQ_CONVST_CS — TQ_CONVST_CS

ADC conversion / chip select; board must define idle state.

TQ_AOUT — TQ_AOUT

Half-scale analog output to external BNC; load >=1 Mohm, no 50 ohm termination.

TQ_AOUT_MON — TQ_AOUT_MON

Half-scale divider monitor through 1k; high-impedance probe.

SCK_INST — SCK_INST

100 ohm isolated clock monitor; shared-bus ownership issue.

COPI_INST — COPI_INST

100 ohm isolated data-in monitor; shared-bus ownership issue.

CIPO_INST — CIPO_INST

100 ohm isolated data-out monitor; shared-bus ownership issue.

TQ_CONVST_CS_INST — TQ_CONVST_CS_INST

100 ohm isolated conversion / chip-select monitor.

TQ_CAL_EN_INST — TQ_CAL_EN_INST

1k isolated calibration-gate monitor.

OPERATION

Signal path: SIG_P/SIG_N –> IN_P/IN_N –> INA_OUT –> ATT_TAP –> FILT_IN –> AMP_VOUT. ADC_IN reads full amplitude; TQ_AOUT and TQ_AOUT_MON read half amplitude.

Ideal DC: INA_OUT = VEXC/2 + 191.734 x (SIG_P − SIG_N); AMP_VOUT = INA_OUT/3; unloaded TQ_AOUT = AMP_VOUT/2.

At 10 V excitation, zero torque is 1.6667 V at AMP_VOUT and 0.8333 V at TQ_AOUT. Nominal +/−1.5 mV/V rated bridge output gives 0.3540–1.3127 V at TQ_AOUT.

With the 1.577 mV/V sensor certificate, ideal +/−150% overload gives 0.0774–1.5892 V at TQ_AOUT. These are calculated values before tolerances and loading.

Configure ADS8689 for 0–5.12 V; allow 20 ms for its reference, then allow bridge thermal settling. Fit ADC and analog–output calibration separately for each sensor / board / cable; tare before trials.

The 1.642 V level is the documented upstream INA–limited ceiling, not a universal fault clamp. A buffer output short to a +5 V rail at +2% gives about 2.55 V after division; the ESD diode does not limit DC faults.

PCB PLACEMENT / ROUTING

Place sensor connector –> input filter / INA821 –> RC filter / buffer –> analog output along a quiet edge. Place the ADC toward the digital side.

Keep motor/brake copper and the 12 V switching loop remote. Return bridge excitation and shield at the connector; do not share their current paths with input/filter returns.

VERIFY

As–drawn issues: no calibration gate pull–down or chip–select pull–up. R2012 and R2024/R2025/R2026 load or tap shared SPI lines; resolve board ownership before reuse.

Verify harness pinout against J2001 on this sheet. Historical pin tables and GPIO calibration claims do not match this circuit.

Bench–check excitation–loop stability with the real cable, switcher pickup, calibration switching, polarity and output loading. Connectivity checks do not establish analog performance.

Declare supply drive for +12V, +5V and +3.3V at the board/harness boundary for ERC; the ferrites and Q2002 interrupt driver propagation, so the block flags +12V_FILT, +5V_FILT and VEXC itself. Put separate block instances on separate hierarchical sheets so their local nets do not merge.

DESIGN NOTES

Source migration preserves the existing circuit and routed PCB. Review the calibration–drive and SPI ownership limitations before reuse.

Original connector notes: −SIG (WHITE); +SIG (GREEN); +EXC (RED); −EXC (BLACK); SHIELD. J2001 pin mapping is documented in section 1.

DESIGN CONTRACT

Single–channel torque sensor front end for a Transducer Techniques RTS–5 reaction bridge (350 ohm, 1.5 mV/V, 5 in–oz), giving a nominal 0.3540–1.3127 V ground–referenced rated–range analog output for a Neuropixels OneBox ADC channel, plus an on–board ADS8689 that streams the same conditioned signal at FULL amplitude. At the BNC, zero torque is nominally 0.8333 V; the fitted 259 ohm gain resistance gives INA821 gain 191.734. At 1.5 mV/V, +/−rated spans 0.3540–1.3127 V. The 1.577 mV/V sensor certificate at +/−150% overload predicts 0.0774–1.5892 V before tolerances. The ADC sees twice the unloaded BNC amplitude.
FULL DERIVATION, VALUES, LAYOUT RULES AND OPEN ITEMS ARE IN kicad–libs docs/torque–sensor–interface–design.md. This note carries only what breaks silently without it. Designators have changed across annotations, so the invariants below are also identified by NET.
1. EVERYTHING THAT LEAVES THE BOARD IS HALVED; THE ON–BOARD ADC IS NOT. A /2 divider (two 3.2k 0.1% 25ppm/C plus a 470 pF C0G midpoint shunt) sits in the TQ_AOUT leg only, between AMP_VOUT and the 249 ohm BNC resistor. TQ_AOUT_MON taps the divider midpoint so the scope tap reads what the BNC delivers. ADC_IN taps AMP_VOUT, so the MCU record and the OneBox record differ by exactly 2 and need TWO calibration constants. AMP_VOUT is the single reference node for both.
2. THE ADC's TAP MUST NOT MOVE TO THE MIDPOINT, and this is not obvious. The ADS8689's AIN_P is a RESISTIVE input, 1 MOhm +/−15% and range–programmable between 1 MOhm and 1.2 MOhm –– not a buffered high–Z input. On the midpoint it parallels the 3.2k bottom leg and becomes part of the ratio: BNC loading goes from −0.185% to −0.344%, the converter's input bias puts about +2.6 mV on the BNC (0.018 N.cm, ten times the sensor's 0.0018 N.cm nonrepeatability), and a firmware write changing the ADC's input range silently re–scales the OneBox reading. The bound the divider exists for does not apply to ADC_IN anyway: it never leaves the board, the ADC's range is 0–5.12 V, and its input protection is +/−20 V powered.
3. THE INA821's +VS BINDS TO VEXC, NOT +12V_FILT. That limits the INA821–driven pre–divider ceiling to about 3.283 V, or 1.642 V after division. It is NOT a universal output fault clamp: a downstream +5 V buffer rail fault at +2% can give about 2.55 V after division, and the ESD device does not clamp DC. Check the receiving input limits independently. Both nets are 10–12 V, both 'work', and ERC passes either way.
4. THE EXCITATION LOOP FEEDS BACK FROM VEXC AT THE CONNECTOR PIN, not from the emitter or the base node. From the emitter the 10 ohm isolation resistor's 286 mV drop goes uncorrected, a 2.9% sensitivity error. The 100k pull–down on VREF10 is what makes an open reference fail LOW instead of driving the ceiling to the 12 V rail.
5. TQ_AOUT, TQ_AOUT_MON AND ADC_IN ARE THREE DIFFERENT NETS AT TWO DIFFERENT SCALES. TQ_AOUT is the delivered output and carries the 249 ohm source resistor and the ESD clamp; verify on the netlist that the clamp shares a net with the connector pin. This was got wrong once already, on mouse–joystick–pcb.
6. TQ_AOUT HAS AN INA821–LIMITED CEILING OF ABOUT 1.642 V FROM A 1.849 kohm SOURCE AND NEEDS A >=1 Mohm LOAD. The source is the 249 ohm series resistor PLUS the divider's 1.6 kohm, not 249 ohm alone –– against the OneBox AD7616–P's 1 Mohm that is −0.185% of gain, systematic and absorbed by per–board calibration, but a 100 kohm load costs −1.82% and a 50 ohm terminated input reads a fraction of the correct value. The 249 ohm bounds a short of TQ_AOUT to ground at 6.6 mA and 11 mW inside a 62.5 mW 0402. The ESD clamp is a transient device and does NOT bound a DC fault.
7. THE RATIO RESISTORS ARE TWO SEPARATE MATCHED SETS AND THE BLOCK ALSO CONTAINS DECOYS. FIVE 10.0k ERA2AEB103X from one reel –– two for the /2 VMID midpoint, two in series for the /3 ADC divider top, one for its bottom. TWO 3.2k RT0402BRD073K2L from one reel for the output /2 divider. The block's two generic 10k pulls (R2011 reset pull–up, R2012 CIPO pull–down) are also 10k, and there are THREE 249 ohm parts –– the BNC series resistor, the ADC series resistor, and the 0.1% RG gain resistor. Identify every one of them by NET, never by value or by designator adjacency.
8. THE FILTER CAPACITORS MUST BE C0G, AND SO MUST THE 470 pF DIVIDER MIDPOINT SHUNT. Retune the filter by scaling BOTH capacitors by the same factor; the resistors set the DC gain and the whole mapping. Its 263 us group delay is deliberately matched to analog_output_0_3v3_dac80501's 266 us. The midpoint shunt is 470 pF because it adds only 0.75 us against that budget; 10 nF would add 16 us. Class–2 dielectric is piezoelectric, this board is coupled to a stepper and a hand–driven joystick, and on the divider midpoint that pickup becomes signal. A mechanically generated torque artifact in a torque measurement cannot be filtered out.
9. SPI: the saved circuit has a 10k pull–down on CIPO (SDO) and no fitted pull–up on TQ_CONVST_CS. Shared–bus idle termination belongs to the BOARD; repeated blocks duplicate the inherited CIPO pull and SCK/CIPO/COPI instrument taps. Resolve this ownership issue before reuse. The placing board defines SCK and COPI on the peripheral side of the default–open SN74CB3Q3245; the RP2040 end uses its own pad pull–downs.
10. SHUNT CALIBRATION IS NOT VERIFIED: TQ_CAL_EN drives the Q2001 gate directly, with no fitted gate pull–down; the only series part on that port is the 1k R2028 feeding the TQ_CAL_EN_INST tap. Its source is SIG_N, nominally near 5 V, so a 3.3 V GPIO cannot provide positive VGS. Arrange an appropriate drive and reset–safe gate bias in a separately reviewed circuit revision before relying on shunt calibration. It is a static enable, not an edge worth a logic–analyzer channel.
11. PWR_FLAG on +12V_FILT, +5V_FILT and VEXC is required, because ferrites and a pass transistor break driver propagation. GND is flagged once at board level, not here. Expect ERC to want one on the ADC's REFCAP and REFIO too: the official–derived symbol types REFCAP as power_in, matching upstream. Not a defect.
12. Bind +12V, +5V and +3.3V all to the SWITCHED domain. 0 V and the INA821–limited 1.642 V ceiling are out–of–band fault indications; other faults can exceed that ceiling. Two instances need separate sheets or their local nets merge.
13. CALIBRATION IS PER SENSOR AND PER BOARD, and the two channels are NOT interchangeable –– pair each sensor with a board serial and move its certificate constant with it. Fit the BNC and the ADC paths separately; do not derive one from the other by a factor of 2, because the divider's own 0.1% tolerance is part of the BNC gain. The sensor is the limit either way: 0.05% nonrepeatability is 0.001765 N.cm, which is 249 uV at the BNC after the divider (1.6 OneBox codes) and 6.4 LSB at the ADC's 78.125 uV.

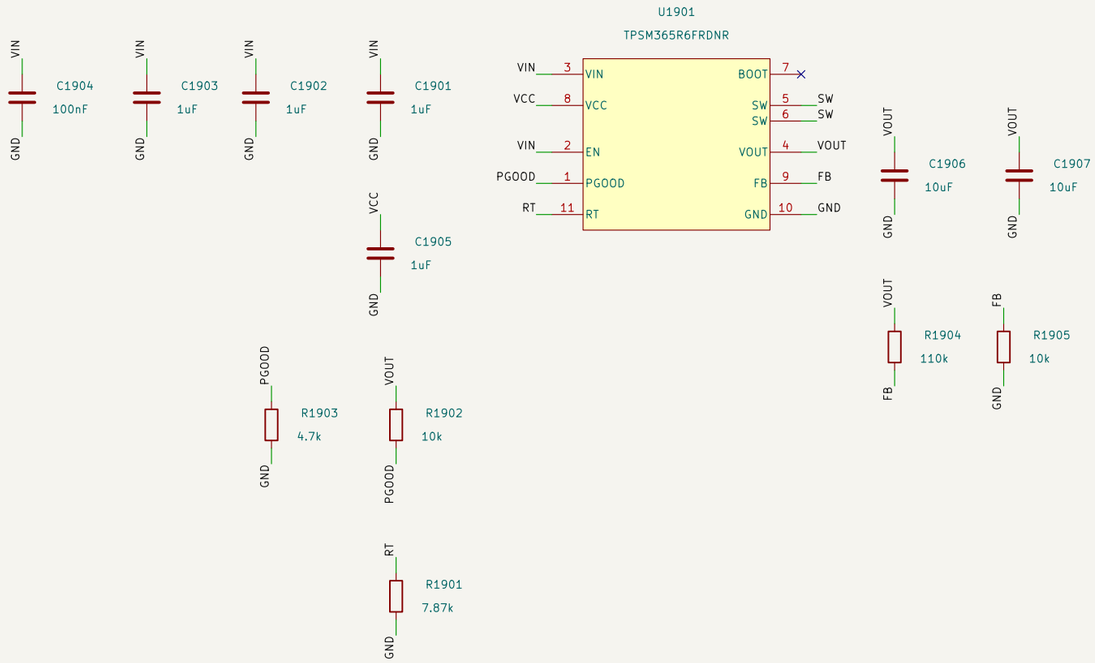
TPSM365R6 adjustable buck | 12 V or 7.04 V variant, 600 mA, PGOOD divider

High-voltage input to an adjustable 12 V or 7 V rail: TI TPSM365R6F 600 mA buck module, one family source with the FB top leg, the PGOOD bottom leg and the second output capacitor as the variant.

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Buck module, input bypass and output capacitors

U1901 converts VIN to the adjustable VOUT. Three 1 uF 100 V capacitors (C1901 to C1903) and the 100 nF C1904 bypass VIN (pin 3) to GND at the module input; C1905 (1 uF) bypasses the internal LDO output VCC (pin 8); C1906 and C1907 (10 uF) hold the output. C1907 is unpopulated on the 7v variant. R1904 (variant: 110 k or 60.4 k) from VOUT and R1905 (10 k) to GND set FB to the 1.000 V reference. R1902 (10 k) from VOUT and R1903 (variant: 4.7 k or 10 k) to GND pull the open-drain PGOOD up and set its high level. R1901 (7.87 k) from RT (pin 11) to GND programs the switching frequency.



Buck module, integrated inductor
C1901, C1902, C1903: VIN bulk, 1 uF 100 V; C1904: VIN HF bypass, 100 nF
C1906: Output capacitor, 10 uF
C1907: Output capacitor, 10 uF; DNP on 7v
C1905: VCC LDO bypass, 1 uF
R1901: RT frequency-set resistor, 7.87 k
R1902: PGOOD pull-up, 10 k
R1903: PGOOD bottom leg (variant)
R1904: FB top leg (variant)
R1905: FB bottom leg, 10 k

PLACE: Place C1904 (100 nF) closest to VIN (pin 3) and GND (pin 10), the 1 uF parts beside it; the input current loop is the noisiest on the block.

PLACE: Place C1905 at VCC (pin 8) with a short return to pin 10.

PLACE: Place C1906 and C1907 at VOUT (pin 4) with their GND ends at pin 10; keep the output loop short and on one layer.

PLACE: Place R1905 at FB (pin 9) and GND, R1904 beside it; the FB node must stay short and away from the switch node.

PLACE: Anywhere between VOUT, pin 1 and the PGOOD port; low-current nodes.

PLACE: Place R1901 at pin 11 with a short return to pin 10.

ROUTE: Wide, short VIN copper from the capacitors into pin 3; no via between C1904 and the module if the layer allows it.

ROUTE: VCC stays inside the block; nothing else loads it.

ROUTE: VOUT is block-local copper (PWR_12V_LOCAL); the board names and classes the net on its side of the sheet pin.

ROUTE: FB is a high-impedance node: no via stitching under it, no parallel run with VIN or VOUT copper.

ROUTE: PGOOD is a logic flag on the Default class; its high level is the divider's, 3.84 V or 3.52 V.

ROUTE: RT is a sensitive analog node; keep it short and away from the switch node.

INTERFACES

VIN — VIN

3.6 to 65 V input on VIN (pin 3) and EN (pin 2, tied: always enabled).

VOUT — VOUT

Adjustable output set by the FB divider: 12.0 V (12v) or 7.04 V (7v); 600 mA.

GND — GND

Return for the module (pin 10), the dividers and every capacitor.

PGOOD — PGOOD

PGOOD divider midpoint (R1902 10 k over R1903): 3.84 V high on 12v, 3.52 V on 7v.

INTERNAL NETS

FB: Feedback (pin 9) against the 1.000 V reference: R1904 from VOUT over R1905 (10 k) to GND.

RT: RT (pin 11) to GND through R1901 (7.87 k), which programs the switching frequency.

VCC: Internal LDO output (pin 8), bypassed by C1905 (1 uF).

SW: Switch node of the module's integrated inductor: pins 5 and 6 tied to each other, nothing external.

OPERATION

Signal path: VIN (3.6 to 65 V after start-up, UVLO rising 3.4 V typical) enters VIN (pin 3) and EN (pin 2, tied to VIN, so the module runs whenever input is present); the integrated-inductor module delivers VOUT (pin 4), 600 mA maximum, regulated so that FB (pin 9) sits at the 1.000 V reference (0.985 to 1.010 V): VOUT = 1 V x (1 + R1904 / R1905).

Variants: 12v fits R1904 = 110 k (OW-PASS-FRC0402F1103TS) and R1903 = 4.7 k with both 10 uF output capacitors, 12.0 V; 7v fits R1904 = 60.4 k (OW-PASS-0402WGF6042TCE) and R1903 = 10 k and leaves C1907 unpopulated, 7.04 V. One schematic and one copper serve both variants; only those three parts differ, and each set point must stay inside the reference-tolerance window (12.000 V nominal, 11.82 to 12.12 V; 7.04 V nominal, 6.93 to 7.11 V).

PGOOD (pin 1) is the module's open-drain window comparator (high inside the window, rising at about 107 % and falling at about 94 % of the set point, 25 us deglitch); the port is the divider midpoint, R1902 (10 k) from VOUT over R1903 to GND, so its high level is about 3.84 V on the 12 V variant and 3.52 V on the 7 V variant. 3.84 V is above a 3.3 V logic input's absolute maximum: a 3.3 V host needs a 5 V-tolerant input or its own divider.

RT (pin 11) to GND through R1901 (7.87 k) programs the switching frequency; it is a block value, not a variant (the datasheet gives the two pin-strap frequencies, 2.2 MHz with RT at GND and 1 MHz with RT at VCC; a resistor sets a frequency in between). VCC (pin 8) is the internal LDO output, bypassed by C1905. BOOT (pin 7) is left open and the SW pins (5, 6) are tied only to each other, as the block was drawn and built.

Bypass: three 1 uF 100 V 1206 capacitors (C1901 to C1903) and a 100 nF 0603 (C1904) at VIN; the 10 uF 25 V output capacitors sit at about 48 % (12 V) and 28 % (7 V) of their rating, inside the family's 60 % voltage-derating rule. Current limits from the datasheet: high-side short-circuit 1 A typical, low-side 0.7 A typical.

The placing board provides the VIN entry on its own class (the block's PWR_HV_LOCAL copper is block-local), a load of at most 600 mA, its own name for the VOUT net (the port is VOUT because the variant sets the voltage; its copper is PWR_12V_LOCAL) and the thermal path: RthJA 56.3 C/W on a JEDEC 4-layer board, so give the module's pad a ground pour and vias.

DESIGN CONTRACT

High-voltage input to an adjustable 12 V or 7 V rail: TI TPSM365R6F 600 mA buck module, one family source with the FB top leg, the PGOOD bottom leg and the second output capacitor as the variant.

Circuit and PCB layout guidance
Migrated from the saved family core; circuit, variants and PCB unchanged
Orb Weaver

Sheet: /brake_torque_sensor/hv_to_12v_tpsm365r6/
File: hv_to_12v_tpsm365r6.kicad_sch

Title: TPSM365R6 adjustable buck family

Size: A3	Date: 2026-10-04	**Rev: Source migration 1**
KiCad E.D.A. 10.0.6		Id: 19/20

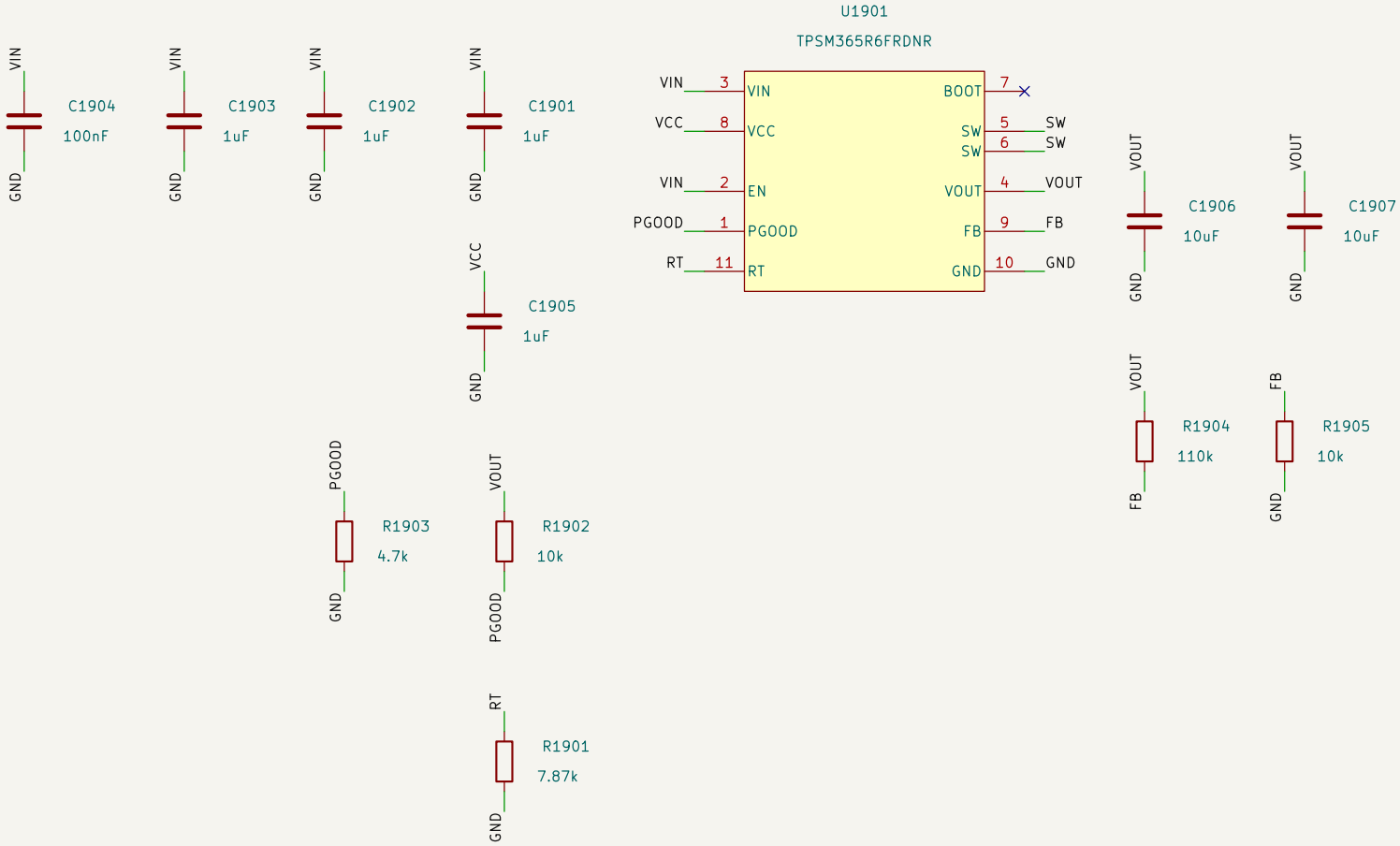
TPSM365R6 adjustable buck | 12 V or 7.04 V variant, 600 mA, PGOOD divider

High−voltage input to an adjustable 12 V or 7 V rail: TI TPSM365R6F 600 mA buck module, one family source with the FB top leg, the PGOOD bottom leg and the second output capacitor as the variant.

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Buck module, input bypass and output capacitors

U1901 converts VIN to the adjustable VOUT. Three 1 uF 100 V capacitors (C1901 to C1903) and the 100 nF C1904 bypass VIN (pin 3) to GND at the module input; C1905 (1 uF) bypasses the internal LDO output VCC (pin 8); C1906 and C1907 (10 uF) hold the output. C1907 is unpopulated on the 7v variant. R1904 (variant: 110 k or 60.4 k) from VOUT and R1905 (10 k) to GND set FB to the 1.000 V reference. R1902 (10 k) from VOUT and R1903 (variant: 4.7 k or 10 k) to GND pull the open−drain PGOOD up and set its high level. R1901 (7.87 k) from RT (pin 11) to GND programs the switching frequency.



Buck module, integrated inductor
C1901, C1902, C1903: VIN bulk, 1 uF 100 V; C1904: VIN HF bypass, 100 nF
C1906: Output capacitor, 10 uF
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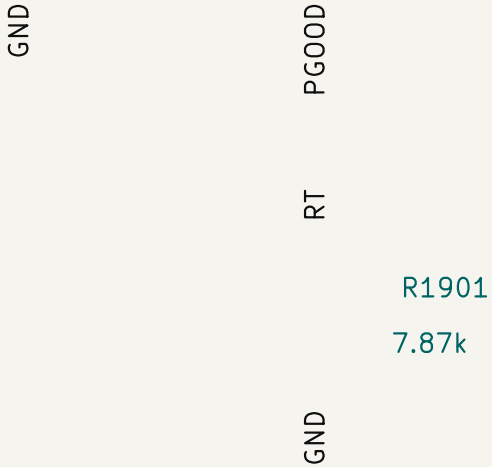
R1903: PGOOD bottom leg (variant)
R1904: FB top leg (variant)
R1905: FB bottom leg, 10 k



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R1902: PGOOD pull–up, 10 k
R1903: PGOOD bottom leg (variant)
R1904: FB top leg (variant)
R1905: FB bottom leg, 10 k

PLACE: Place C1904 (100 nF) closest to VIN (pin 3) and GND (pin 10), the 1 uF parts beside it; the input current loop is the noisiest on the block.

PLACE: Place C1905 at VCC (pin 8) with a short return to pin 10.

PLACE: Place C1906 and C1907 at VOUT (pin 4) with their GND ends at pin 10; keep the output loop short and on one layer.

PLACE: Place R1905 at FB (pin 9) and GND, R1904 beside it; the FB node must stay short and away from the switch node.

PLACE: Anywhere between VOUT, pin 1 and the PGOOD port; low–current nodes.

PLACE: Place R1901 at pin 11 with a short return to pin 10.

ROUTE: Wide, short VIN copper from the capacitors into pin 3; no via between C1904 and the module if the layer allows it.

ROUTE: VCC stays inside the block; nothing else loads it.

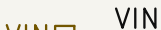
ROUTE: VOUT is block–local copper (PWR_12V_LOCAL); the board names and classes the net on its side of the sheet pin.

ROUTE: FB is a high–impedance node: no via stitching under it, no parallel run with VIN or VOUT copper.

ROUTE: PGOOD is a logic flag on the Default class; its high level is the divider's, 3.84 V or 3.52 V.

ROUTE: RT is a sensitive analog node; keep it short and away from the switch node.

INTERFACES



3.6 to 65 V input on VIN (pin 3) and EN (pin 2, tied: always enabled).

Adjustable output set by the FB divider: 12.0 V (12v) or 7.04 V (7v); 600 mA.

Return for the module (pin 10), the dividers and every capacitor.

PGOOD divider midpoint (R1902 10 k over R1903): 3.84 V high on 12v, 3.52 V on 7v.

Adjustable output set by the FB divider: 12.0 V (12v) or 7.04 V (7v); 600 mA.

GND GND

Return for the module (pin 10), the dividers and every capacitor.

PGOOD PGOOD

PGOOD divider midpoint (R1902 10 k over R1903): 3.84 V high on 12v, 3.52 V on 7v.

INTERNAL NETS

FB: Feedback (pin 9) against the 1.000 V reference: R1904 from VOUT over R1905 (10 k) to GND.

RT: RT (pin 11) to GND through R1901 (7.87 k), which programs the switching frequency.

VCC: Internal LDO output (pin 8), bypassed by C1905 (1 uF).

SW: Switch node of the module's integrated inductor: pins 5 and 6 tied to each other, nothing external.

OPERATION

Signal path: VIN (3.6 to 65 V after start-up, UVLO rising 3.4 V typical) enters VIN (pin 3) and EN (pin 2, tied to VIN, so the module runs whenever input is present); the integrated-inductor module delivers VOUT (pin 4), 600 mA maximum, regulated so that FB (pin 9) sits at the 1.000 V reference (0.985 to 1.010 V): VOUT = 1 V x (1 + R1904 / R1905).

Variants: 12v fits R1904 = 110 k (OW-PASS-FRC0402F1103TS) and R1903 = 4.7 k with both 10 uF output capacitors, 12.0 V; 7v fits R1904 = 60.4 k (OW-PASS-0402WGF6042TCE) and R1903 = 10 k and leaves C1907 unpopulated, 7.04 V. One schematic and one copper serve both variants; only those three parts differ, and each set point must stay inside the reference-tolerance window (12.000 V nominal, 11.82 to 12.12 V; 7.04 V nominal, 6.93 to 7.11 V).

PGOOD (pin 1) is the module's open-drain window comparator (high inside the window, rising at about 107 % and falling at about 94 % of the set point, 25 us deglitch); the port is the divider midpoint, R1902 (10 k) from VOUT over R1903 to GND, so its high level is about 3.84 V on the 12 V variant and 3.52 V on the 7 V variant. 3.84 V is above a 3.3 V logic input's absolute maximum: a 3.3 V host needs a 5 V-tolerant input or its own divider.

RT (pin 11) to GND through R1901 (7.87 k) programs the switching frequency; it is a block value, not a variant (the datasheet gives the two pin-strap frequencies, 2.2 MHz with RT at GND and 1 MHz with RT at VCC; a resistor sets a frequency in between). VCC (pin 8) is the internal LDO output, bypassed by C1905. BOOT (pin 7) is left open and the SW pins (5, 6) are tied only to each other, as the block was drawn and built.

Bypass: three 1 uF 100 V 1206 capacitors (C1901 to C1903) and a 100 nF 0603 (C1904) at VIN; the 10 uF 25 V output capacitors sit at about 48 % (12 V) and 28 % (7 V) of their rating, inside the family's 60 % voltage-derating rule. Current limits from the datasheet: high-side short-circuit 1 A typical, low-side 0.7 A typical.

The placing board provides the VIN entry on its own class (the block's PWR_HV_LOCAL copper is block-local), a load of at most 600 mA, its own name for the VOUT net (the port is VOUT because the variant sets the voltage; its copper is PWR_12V_LOCAL) and the thermal path: RthJA 56.3 C/W on a JEDEC 4-layer board, so give the module's pad a ground pour and vias.

DESIGN CONTRACT

High-voltage input to an adjustable 12 V or 7 V rail: TI TPSM365R6F 600 mA buck module, one family source with the FB top leg, the PGOOD bottom leg and the second output capacitor as the variant.

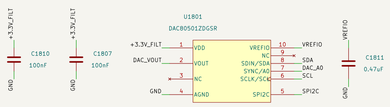
Brake current sink 0–48.78 mA | DAC80501 on I2C, OPA197 loop, BUK7D36-60EX, 10 ohm Kelvin shunt, 56.4 mA ceiling

DAC-programmed linear constant-current sink delivering 0–48.78 mA into a 24 V magnetic particle brake coil from a 36 V rail: a DAC80501ZDGSR at 3.3 V on I2C feeding a 0.19512 precision divider, an OPA197 integrating error amplifier on a ferrite-filtered 12 V rail driving a BUK7D36-60EX pass device over a 10 ohm Kelvin shunt, a second OPA197 as an independent 56.4 mA current ceiling that clamps the gate through a Schottky, a third as a 0–1.006 V ground-referenced current monitor behind a /2 output divider, an SN74LVC2G17 buffering the ceiling event out as active-low BRAKE_FAULT, and an S115Q flyback across the in-block 2-position 3.5 mm vertical coil terminal.

Matching net labels are connected. Group order explains function: PCB placement priorities are stated below.

1. DAC and address straps

U1801 generates 0–2.5 V on its internal reference; R1809 selects I2C, R1807 sets the address 0x49, C1811 bypasses VREFIO.



16-bit I2C DAC. Internal 2.5 V reference
R1807: A0 strap to VDD, address 0x49
R1809: SPI2C strap to VDD, I2C mode
C1811: VREFIO reference bypass
C1807, C1810: U1801 VDD pin 1 bypass

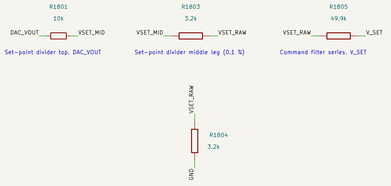
PLACE: C1811 (0.47 uF; 150 nF or more is required) hard against pin 10 with the shortest return to pin 4 (AGND).

PLACE: Both straps reference +3.3V_FILT, the potential the DAC calls VDD; silkscreen the address next to R1807.

ROUTE: SCL and SDA run straight from the ports to pins 6 and 8; no termination or tap inside the block (conventions 10 and 14).

2. Set-point divider and command filter

R1801, R1803 and R1804 scale DAC_VOUT by 0.19512 to V_SET_RAW: R1805 and C1808 filter it at 303 Hz to V_SET.



Set-point divider top, DAC_VOUT

Set-point divider middle leg (0.1 %)

Command filter series, V_SET

Set-point divider bottom leg (0.1 %)

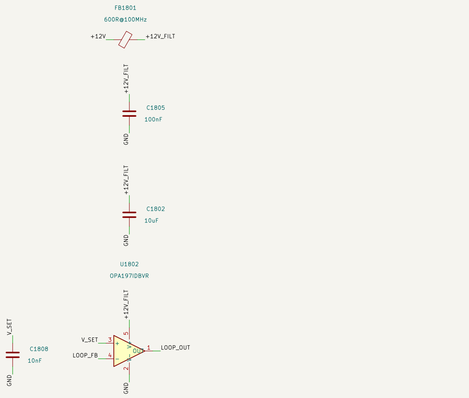
PLACE: The three divider resistors are the 0.1 %, 25 ppm set; keep them together.

PLACE: C1808 sits after R1805, never on the DAC output (DAC80501 C_LOAD maximum 2 nF); the 16.4 kohm divider is far above its 0.5 kohm minimum load.

ROUTE: V_SET is the loop's reference; short, guarded by analog ground, its own netclass.

3. Loop amplifier and gate drive

U1802 integrates V_SET minus V_SENSE (R1806, C1812) into LOOP_OUT and drives GATE through R1813; R1814 pulls the gate down; D1801 lets the ceiling amplifier clamp it.



Loop error integrator, gate drive
C1802: Rail bulk bypass
C1805: U1802 V+ pin 5 bypass
FB1801: Rail ferrites
C1808: Command filter, V_SET (C0G)

Loop Integrator Input, V_SENSE

Loop Integrator, U1802 (C0G)

Gate series, LOOP_OUT to GATE

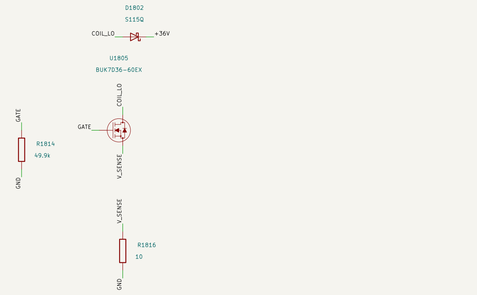
Gate clamp steering diode

PLACE: R1813 (1 k) is required: U1802 drives 1 nF maximum and must see the resistor, not U1805's input capacitance; put R1813 and R1814 at the gate.

ROUTE: LOOP_FB and GATE are the loop's nodes: keep digital return currents and the BRAKE_ISENSE trace away from LOOP_FB.

4. Pass device, Kelvin shunt, coil terminal and flyback

U1805 sinks the coil current from COIL_LO through R1816 to GND; J1801 carries the coil between +36V and COIL_LO with D1802 as its flyback; C1817 and C1818 bypass the coil rail.



Linear pass MOSFET, coil current sink
R1816: Kelvin current shunt, 10 ohm: one per S pins 4, 8
D1802: Coil flyback Schottky: one per D pins 1, 2, 5, 6, 7
R1814: GATE pull-down

Brake coil terminal, +36V and COIL_LO

+36V coil rail bypass

+36V coil rail HF bypass

PLACE: Give U1805's drain pad as close to 6 cm2 of copper as the brake zone allows, on the far side from the torque front end, never spreading toward it.

PLACE: D1802 directly across J1801's pins: C1817 and C1818 at pin 2.

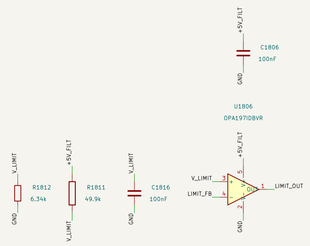
PLACE: Kelvin-tap V_SENSE once at R1816 and fan out to the loop, ceiling and monitor inputs.

ROUTE: The coil current path (J1801 pin 1, U1805 drain to source, R1816, GND) is sized for 50 mA at 36 V and stays out of the torque analog zone: the brake return joins board ground once at the power-stage return point.

ROUTE: Place the block at the 36 V entry and the brake connector, opposite the bridge, PGA/ADC and reference.

5. Current ceiling

R1811 and R1812 derive V_LIMIT (564 mV) from +5V_FILT, bypassed by C1816; U1806 integrates V_SENSE against it (R1815, C1820) and clamps the gate through D1801 when 56.4 mA is reached.



Current ceiling amplifier, 56.4 mA
C1816: V_LIMIT reference bypass
R1811: V_LIMIT divider top
R1812: V_LIMIT divider bottom
C1806: U1806 V+ pin 5 bypass

Ceiling Integrator Input, V_SENSE

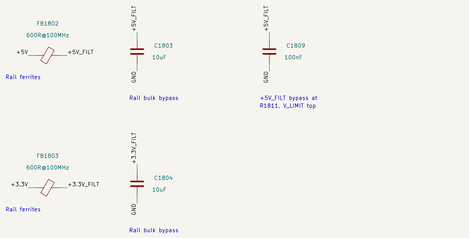
Ceiling Integrator, U1806 (C0G)

PLACE: R1811, R1812 and C1816 at U1806 pin 3; C1820 tight between pins 4 and 1.

ROUTE: V_LIMIT is a reference node: short and guarded; LIMIT_OUT runs to D1801 and to U1803A pin 1.

8. Supply ferrites and bypass

FB1801 filters +12V to +12V_FILT for U1802 (C1802, C1805); FB1802 filters +5V to +5V_FILT for U1804, U1806 and V_LIMIT (C1803, C1806, C1809, C1813); FB1803 filters +3.3V to +3.3V_FILT for U1801 and U1803A (C1804, C1807, C1810, C1814).

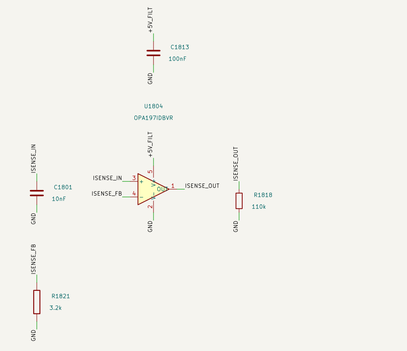


PLACE: One 100 nF at each supply pin it serves: C1805 at U1802 pin 5, C1813 at U1804 pin 5, C1806 at U1806 pin 5, C1809 at R1811 (the V_LIMIT divider top), C1807 and C1810 at U1801 pin 1, C1814 at U1803C pin 5; the 10 uF parts beside their ferrites.

ROUTE: +12V, +5V and +3.3V arrive at the ferrites' pad 1 (PWR_12V_LOCAL, PWR_5V_LOCAL and PWR_3V3_LOCAL vias, convention 1); the filtered rails stay inside the block.

6. Current monitor and output divider

U1804 amplifies the filtered V_SENSE (R1802, C1801) by 4.125 (R1817, R1821, C1819) to ISENSE_OUT; R1818 defines it unpowered: R1808 and R1810 halve it to ISENSE_DIV with C1815 shunting pickup; R1819 delivers BRAKE_ISENSE and D1803 clamps it.



Current monitor amplifier, gain 4.125
C1801: Monitor input filter, ISENSE_IN (C0G)
R1821: Monitor gain-set, ISENSE_FB to GND (0.1 %)
R1818: ISENSE_OUT pull-down, unpowered 0 V
C1813: U1804 V+ pin 5 bypass

Monitor input series, V_SENSE

Monitor gain feedback, U1804

Monitor amplifier compensation

Monitor /2 divider top (0.1 %)

Monitor /2 divider bottom (0.1 %)

ISENSE_DIV midpoint shunt (C0G)

Series output resistor

ESD clamp on BRAKE_ISENSE

PLACE: R1817, R1821 and C1819 tight to U1804 pins 1 and 4; pull the ground pour back from under ISENSE_FB (plane capacitance changes the 10 pF compensation).

PLACE: C1815 at ISENSE_DIV with a short return: R1808 and R1810 side by side (0.1 %, 25 ppm pair).

PLACE: D1803's ground via on the connector ground that BRAKE_ISENSE leaves through.

ROUTE: BRAKE_ISENSE toward the MCU must not touch LOOP_FB or V_SENSE: the buffer exists to keep digital return currents off them.

7. Fault buffer

U1803A buffers LIMIT_OUT to the active-low BRAKE_FAULT; R1820 taps it for the Instrument port. 2A is grounded and 2Y is open.

Unit 1: Schmitt buffer, LIMIT_OUT to BRAKE_FAULT

Unit 2: Schmitt buffer, LIMIT_OUT to BRAKE_FAULT

Power unit C1814: U1803C VCC pin 5 bypass

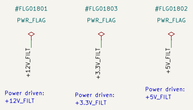
Instrument tap, BRAKE_FAULT

PLACE: U1803A near U1806 with its bypass C1814 at pin 5.

ROUTE: BRAKE_FAULT is a switched-domain output with loft: the placing board terminates it with 10 k to GND on the MCU side.

9. Power drive declarations

These nets have an explicit ERC power source declaration.



Power driven: +12V_FILT

Power driven: +3.3V_FILT

Power driven: +5V_FILT

INTERFACES

+36V — +36V

Coil supply, switched domain: J1801 pin 2 and the flyback cathode of D1802, bypassed by C1817 and C1818; the pass device drops what the coil does not.

+12V — +12V

Gate-drive supply of the loop amplifier U1802, through FB1801 to +12V_FILT.

+5V — +5V

Regulated 5.0 V for the ceiling and monitor amplifiers and the V_LIMIT divider, through FB1802 to +5V_FILT (OPA197 minimum 4.5 V).

+3.3V — +3.3V

Switched 3.3 V: DAC and fault-buffer supply through FB1803 to +3.3V_FILT; the reference of both mode straps.

GND — GND

Return of the shunt R1816, the amplifiers, the DAC and the bypass; the brake return joins board ground once, at the power-stage return point.

SCL — SCL

I2C clock to U1801 pin 6 (SCLK/SCL); single-pin net, the board fits the pull-up.

SDA — SDA

I2C data, U1801 pin 8 (SDIN/SDA), address 0x49; single-pin net, the board fits the pull-up.

BRAKE_ISENSE — BRAKE_ISENSE

Current monitor, 0–1.006 V for 0–48.78 mA from a 1.849 kohm source: needs a >= 1 Mohm load; a ceiling event reads 1.163 V; 0 V means unpowered.

BRAKE_FAULT — BRAKE_FAULT

Active-low continuous limiter indication from U1803A 1Y; high-Z (loft) whenever +3.3V_FILT is down, so the board owes a 10 k pull-down to GND.

BRAKE_FAULT_INST — BRAKE_FAULT_INST

Instrument tap of BRAKE_FAULT through R1820 (1 k); INSTRUMENT class.

OPERATION

Signal path: U1801 VOUT (pin 2, 0–2.5 V) -> R1801 (10 k), R1803 and R1804 (3.2 k each): ratio 3.2/16.4 = 0.19512, so VSET_RAW is 0–0.4878 V -> R1805 (49.9 k) and C1808 (10 nF), the 303 Hz command filter (tau about 525 us with the divider's 2.58 kohm) -> V_SET -> U1802 + (pin 3). U1802 integrates the error against V_SENSE (R1806 49.9 k, C1812 10 nF) and drives GATE through R1813 (1 k); U1805 sources through R1816 (10 ohm), so V_SENSE follows V_SET and the coil current is 0–48.78 mA at 10 mV per mA. loop crossover about 295 Hz. R1814 (49.9 k) holds the gate off when nothing drives it.

Coil and pass device: the coil hangs from +36V at J1801 pin 2 to COIL_LO (pin 1); the drain of U1805: D1802 (S115Q, 150 V 1 A Schottky) is the flyback across the terminal. At 48.8 mA with a hot 605 ohm coil and the rail 5 % low the pass device keeps 4.2 V; with a cold 467 ohm coil and the rail 5 % high it drops 14.5 V and dissipates about 0.71 W. The 36 V rail is required: a 24 V rail cannot reach rated current.

Independent ceiling: U1806 integrates V_SENSE (R1815 49.9 k, C1820 10 nF) against V_LIMIT = 5 V x 6.34/(49.9 + 6.34) = 564 mV from +5V_FILT (R1811, R1812; C1816): 56.4 mA, 115 % of rated. Above it LIMIT_OUT falls and pulls GATE down through D1801; U1803A (Schmitt, 5.5 V-tolerant input) buffers LIMIT_OUT, near 4.96 V idle and about 0.4 V while limiting, to BRAKE_FAULT, a continuous indication, not a latch. V_LIMIT comes from +5V_FILT, not VREFIO, so the ceiling is independent of the DAC and the loop and a sagging rail lowers it.

Monitor: U1804 at gain 1 + 10/3.2 = 4.125 (R1817, R1821, C1819 10 pF) reads V_SENSE through R1802 (49.9 k) and C1801 (10 nF) -> ISENSE_OUT 0–2.012 V: R1808 and R1810 (3.2 k each) halve it to ISENSE_DIV, 0–1.006 V; R1819 (249 ohm) delivers BRAKE_ISENSE and D1803 clamps ESD. The load must be >= 1 Mohm; the divider bounds any single fault. Including U1804 stuck at its 5 V rail, to 2.48 V at the pin: a ceiling event reads 1.163 V, above full scale. R1818 (110 k) stays on ISENSE_OUT, not the midpoint, where it would shift the ratio by ~1.43 %.

I2C, address 0x49: R1809 (1 k to +3.3V_FILT) selects I2C and R1807 (1 k to +3.3V_FILT) sets A0 to 0x49 (the analog output block takes 0x48); A0 is re-sampled during the first byte of every frame: never lift R1807 without re-wiring it in the same operation. No bus termination inside: SCL and SDA leave as single-pin nets and the board fits one 2.2 k pull-up pair per segment. Firmware writes GAIN (4h) = 0x0101 before any DATA write; until then the reference alarm holds VOUT at 0 V, readable in STATUS.

Supplies and rules: +12V, +5V and +3.3V are filtered by FB1801, FB1802 and FB1803 to +12V_FILT, +5V_FILT and +3.3V_FILT, each carrying a PWR_FLAG; +36V blinds to the same switched domain. The five 10 nF capacitors C1801, C1808, C1812, C1815 and C1820 are C0G: 1 mV of piezoelectric charge on V_SET is 0.1 mA of coil current. V_LIMIT stays 5 V-derived and the gate drive stays 12 V. BRAKE_FAULT reads asserted whenever the switched rail is off. Two instances need separate sheets.

DESIGN NOTES

A0=VDD 0x49

DESIGN CONTRACT

DAC-programmed linear constant-current sink delivering 0–48.78 mA into a 24 V magnetic particle brake coil from a 36 V rail: a DAC80501ZDGSR at 3.3 V on I2C feeding a 0.19512 precision divider, an OPA197 integrating error amplifier on a ferrite-filtered 12 V rail driving a BUK7D36-60EX pass device over a 10 ohm Kelvin shunt, a second OPA197 as an independent 56.4 mA current ceiling that clamps the gate through a Schottky, a third as a 0–1.006 V ground-referenced current monitor behind a /2 output divider, an SN74LVC2G17 buffering the ceiling event out as active-low BRAKE_FAULT, and an S115Q flyback across the in-block 2-position 3.5 mm vertical coil terminal. The full derivation, connection table, BOM and open items are in kicad-libs docs/brake-current-sink-design.md; this note carries only what breaks silently without it. Designators are not stable (KiCad auto-annotation orders by sheet position), so everything below is named by net.

1. I2C, NOT SPI, AND THE ADDRESS IS ONE RESISTOR. SPI2C is strapped to +3.3V_FILT through 1k for I2C mode; A0 is strapped to +3.3V_FILT through 1k for 0x49, and analog_output_0_3v3_dac80501 takes 0x48, A0 is a FOUR-STATE pin (AGND 0x48, VDD 0x49, SDA 0x4A, SCL 0x4B), so a rail strap reaches only the first two. A0 is re-sampled during the first byte of EVERY frame, so a floating A0 gives an address that changes between frames rather than a clean failure: never lift that resistor without re-wiring it in the same operation.
2. THIS BLOCK OWNS NO BUS TERMINATIONS and must not gain any. SCL and SDA leave as single-pin nets. The board fits ONE 2.2k pull-up pair PER BUS SEGMENT: the DAC-side pair on the SWITCHED 3.3 V rail, because an always-on pull-up reaching a DAC whose VDD is at 0 V exceeds the VDD+0.3 V digital-input absolute maximum and back-feeds +3.3V_FILT through the internal clamps; the MCU-side pair on the ALWAYS-ON rail, because the SN74CB3Q3245 is open by default. Two instances each carrying pull-ups would halve the resistance.
3. THE 110k OUTPUT PULL-DOWN STAYS ON ISENSE_OUT, upstream of the /2 divider. On the midpoint it parallels the bottom leg (110k||3.2k = 3.1096k, ratio 0.49283, −1.43%) and it is a 1% 100ppm/°C thick film against the divider's 0.1% 25ppm/°C pair, so it would dominate the ratio's whole error budget. General rule: anything whose job is to define a node when the amplifier is dead belongs on the AMP side of a divider; anything in parallel with a divider leg becomes part of the RATIO.
4. BRAKE_ISENSE IS 0–1.006 V FROM A 1.849 kohm SOURCE AND NEEDS A >=1 Mohm LOAD. The /2 divider is what bounds a single fault. Including the monitor amp stuck at its own +5V_FILT rail, to 2.48 V on a connector pin: the 249 ohm series resistor's input and its on ISENSE_DIV, downstream of the divider, never on ISENSE_OUT. A ceiling event reads 1.163 V, deliberately ABOVE full scale, so a limit event stays visible. 0 V means unpowered or dead, not zero current.
5. BRAKE_FAULT IS A SWITCHED-DOMAIN OUTPUT WITH loft, so it is high-Z whenever +3.3V_FILT is down and THE PLACING BOARD OWES THE MCU-SIDE TERMINATION, a 10k pull-down to GND, which means the line reads ASSERTED whenever the switched rail is off. Firmware must only interpret it while the rail is known up. It is a continuous limiter indication, not a latch. Do not substitute the 2G14: it is the inverter.
6. FIRMWARE MUST WRITE GAIN (4h) = 0x0101 BEFORE ANY DATA WRITE. At 3.3 V the reset default 0x0001 is out of spec against the 2.5 V internal reference, so the reference alarm holds the output at 0 V until that write lands. That is a safety property, not a bug, and over I2C the alarm is READABLE in STATUS, which is why this block is on I2C at all.
7. THE FOUR 10 nF FILTER AND COMPENSATION CAPACITORS MUST BE C0G, not X7R or X5R, and so must the divider midpoint's 10 nF. Class-2 dielectric is piezoelectric: this board is mechanically coupled to a stepper and a hand-driven joystick, and 1 mV on V_SET is 0.1 mA of coil current. A mechanically generated torque artifact in a torque measurement cannot be filtered out. C0G at 10 nF forces an 0805 body; take the area.
8. V_LIMIT STAYS 5 V-DERIVED AND THE GATE DRIVE STAYS 12 V. Moving V_LIMIT to 12 V rescales the 564 mV ceiling threshold; moving the loop amp back to 5 V leaves 90 mV of worst-corner gate-drive margin with a −7.5 mV/degC tempco.
9. PWR_FLAG on +12V_FILT, +5V_FILT and +3.3V_FILT is required: the ferrites break driver propagation, GND is flagged once at board level, not here.
10. TWO INSTANCES NEED SEPARATE SHEETS or their local nets merge: +12V_FILT, +5V_FILT, +3.3V_FILT, V_SET, V_SENSE, V_LIMIT, ISENSE_DIV, GATE, SPI2C and DAC_A0. The ferrites parallel, the PWR_FLAGs conflict, and DAC_A0 merging would silently put both DACs on one address.

Circuit and PCB layout guidance
Migrated from the saved library sheet; circuit and PCB unchanged
Orb Weaver

Sheet: /brake_torque_sensor/brake_current_sink_0_49ma_dac80501/
File: brake_current_sink_0_49ma_dac80501.kicad_sch

Title: Brake current sink 0–48.78 mA, DAC80501 and OPA197

Size: A1	Date: 2026-10-04	**Rev: Source migration 1**
KiCad E.D.A. 10.0.6		Id: 18/20

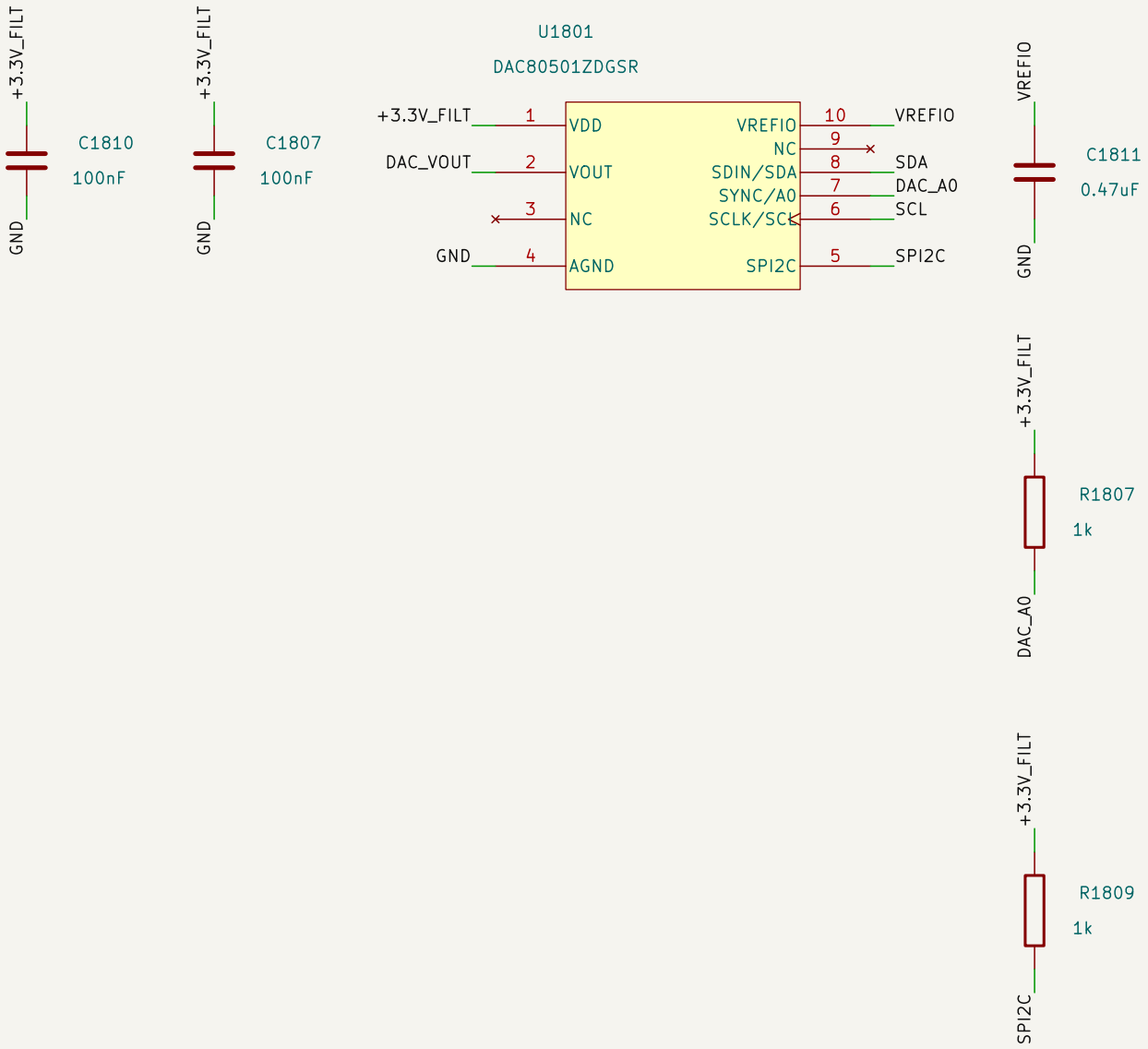
Brake current sink 0–48.78 mA | DAC80501 on I2C, OPA197 loop, BUK7D36-60

DAC-programmed linear constant-current sink delivering 0–48.78 mA into a 24 V magnetic particle brake coil from a 36 V rail: a DAC
vertical coil terminal.

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. DAC and address straps

U1801 generates 0–2.5 V on its internal reference; R1809 selects I2C, R1807 sets the address 0x49, C1811 bypasses VREFIO.



16-bit I2C DAC, internal 2.5 V reference
R1807: A0 strap to VDD, address 0x49
R1809: SPI2C strap to VDD, I2C mode
C1811: VREFIO reference bypass
C1807, C1810: U1801 VDD pin 1 bypass

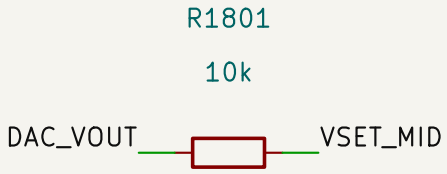
PLACE: C1811 (0.47 uF; 150 nF or more is required) hard against pin 10 with the shortest return to pin 4 (AGND).

PLACE: Both straps reference +3.3V_FILT, the potential the DAC calls VDD; silkscreen the address next to R1807.

ROUTE: SCL and SDA run straight from the ports to pins 6 and 8; no termination or tap inside the block (conventions 10 and 14).

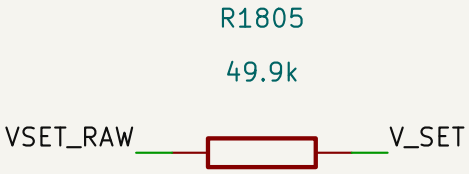
2. Set–point divider and command filter

R1801, R1803 and R1804 scale DAC_VOUT by 0.19512 to VSET_RAW; R1805 and C1808 filter it at 303 Hz to V_SET.

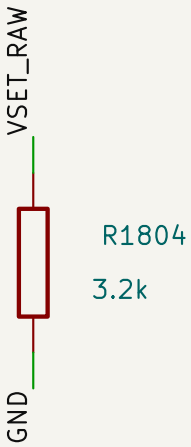


Set–point divider top, DAC_VOUT

Set–point divider middle leg (0.1 %)



Command filter series, V_SET



Set–point divider bottom leg (0.1 %)

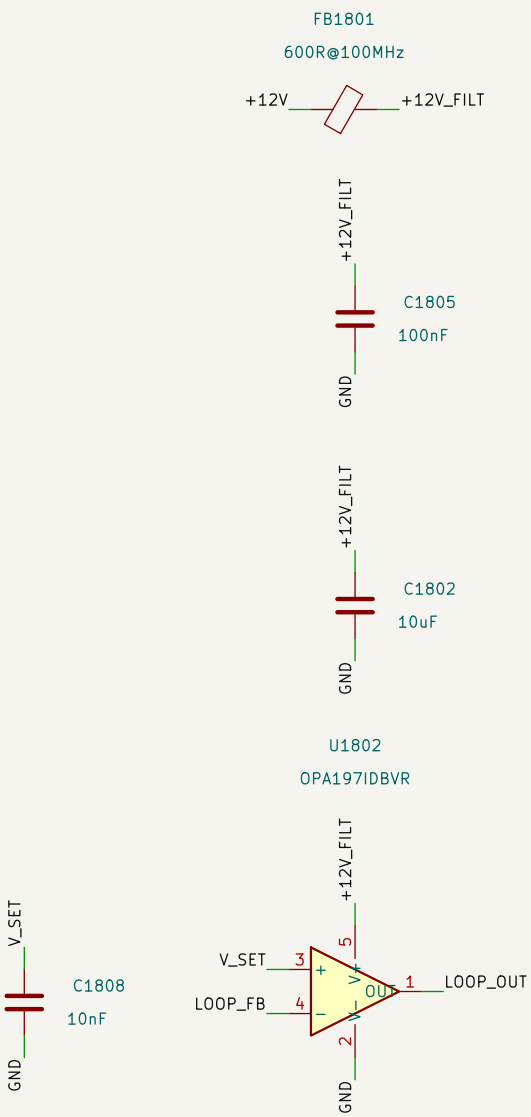
PLACE: The three divider resistors are the 0.1 %, 25 ppm set; keep them together.

PLACE: C1808 sits after R1805, never on the DAC output (DAC80501 C_LOAD maximum 2 nF); the 16.4 kohm divider is far above its 0.5 kohm minimum load.

ROUTE: V_SET is the loop's reference: short, guarded by analog ground, its own netclass.

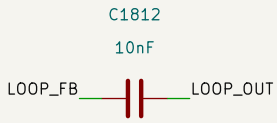
3. Loop amplifier and gate drive

U1802 integrates V_SET minus V_SENSE (R1806, C1812) into LOOP_OUT and drives GATE through R1813; R1814 pulls the gate down; D1801 lets the ceiling amplifier clamp it.

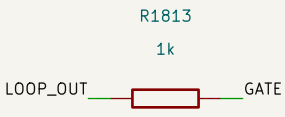


Loop error integrator, gate drive
C1802: Rail bulk bypass
C1805: U1802 V+ pin 5 bypass
FB1801: Rail ferrites
C1808: Command filter, V_SET (C0G)

Loop integrator input, V_SENSE



Loop integrator, U1802 (C0G)



Gate series, LOOP_OUT to GATE

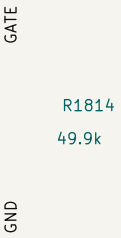
Gate clamp steering diode

PLACE: R1813 (1 k) is required: U1802 drives 1 nF maximum and must see the resistor, not U1805's input capacitance; put R1813 and R1814 at the gate.

ROUTE: LOOP_FB and GATE are the loop's nodes: keep digital return currents and the BRAKE_ISENSE trace away from LOOP_FB.

4. Pass device

U1805 sinks the c
flyback; C1817 an



Linear pass M
R1816: Kelvi
pins 4, 8
D1802: Coil
2, 5, 6, 7
R1814: GATE

J180
TBH-1x02-

Brake coil te
COIL_LO

PLACE: Give U1805
toward it.

PLACE: D1802 dire

PLACE: Kelvin-tap

ROUTE: The coil c
zone; the brake re

ROUTE: Place the

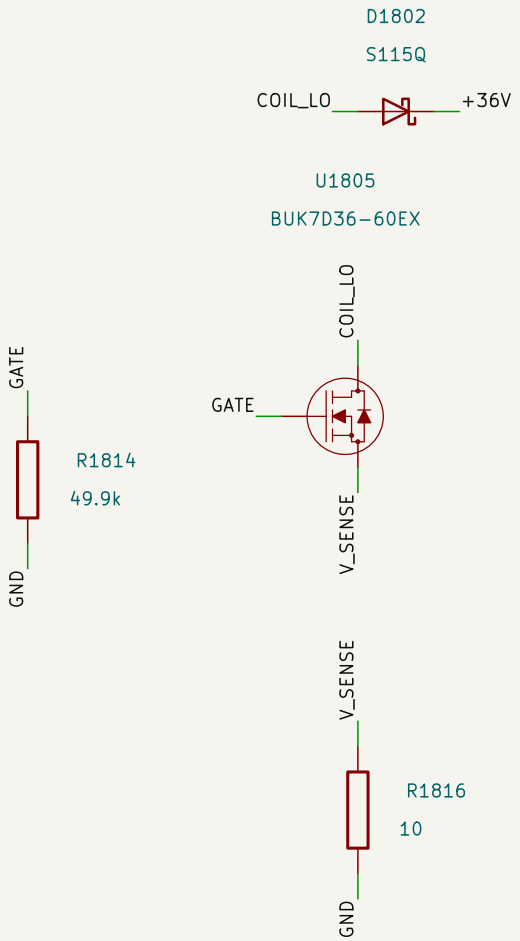
7. Fault buffer

U1803A buffers LI

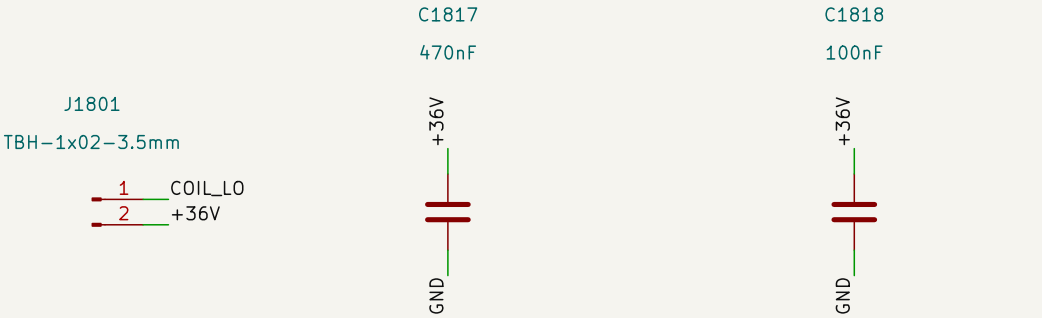
LIMIT_OUT

4. Pass device, Kelvin shunt, coil terminal and flyback

U1805 sinks the coil current from COIL_LO through R1816 to GND; J1801 carries the coil between +36V and COIL_LO with D1802 as its flyback; C1817 and C1818 bypass the coil rail.



Linear pass MOSFET, coil current sink
R1816: Kelvin current shunt, 10 ohm; one per S pins 4, 8
D1802: Coil flyback Schottky; one per D pins 1, 2, 5, 6, 7
R1814: GATE pull-down



Brake coil terminal, +36V and COIL_LO

+36V coil rail bypass

+36V coil rail HF bypass

PLACE: Give U1805's drain pad as close to 6 cm2 of copper as the brake zone allows, on the far side from the torque front end, never spreading toward it.

PLACE: D1802 directly across J1801's pins; C1817 and C1818 at pin 2.

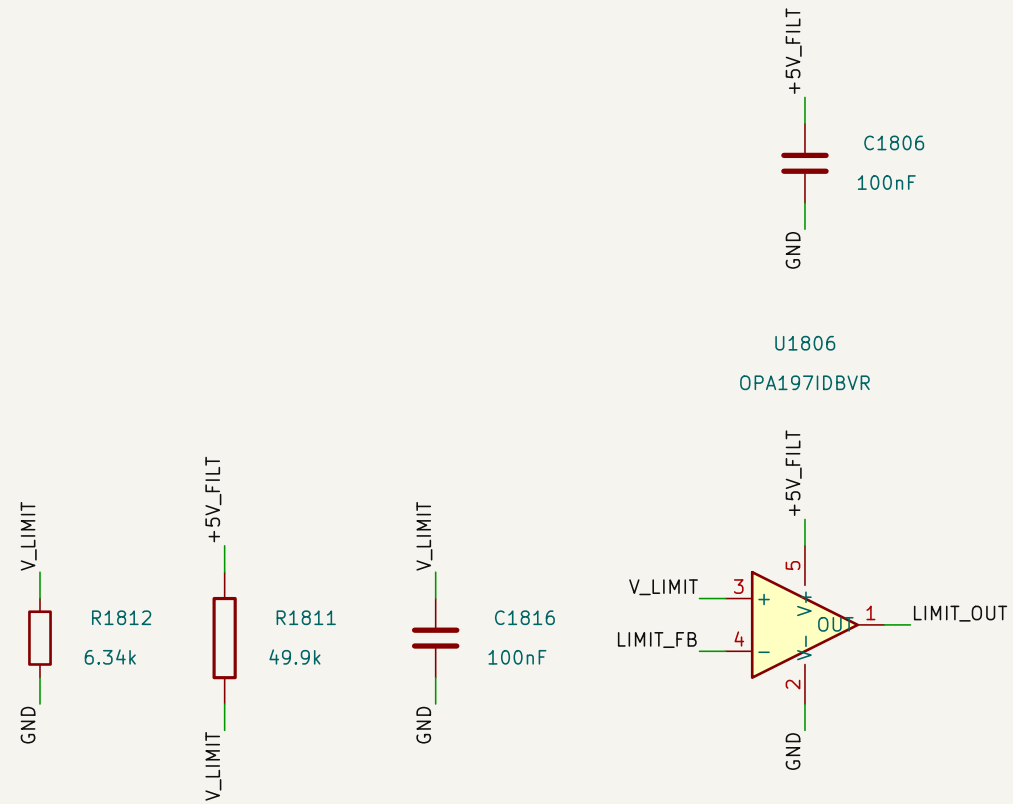
PLACE: Kelvin-tap V_SENSE once at R1816 and fan out to the loop, ceiling and monitor inputs.

ROUTE: The coil current path (J1801 pin 1, U1805 drain to source, R1816, GND) is sized for 50 mA at 36 V and stays out of the torque analog zone; the brake return joins board ground once at the power-stage return point.

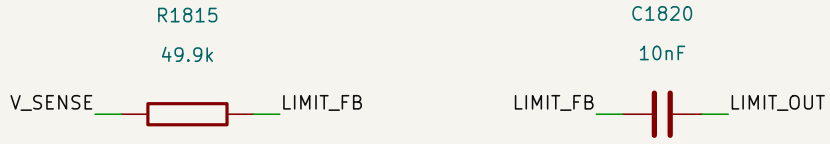
ROUTE: Place the block at the 36 V entry and the brake connector, opposite the bridge, PGA/ADC and reference.

5. Current ceiling

R1811 and R1812 derive V_LIMIT (564 mV) from +5V_FILT, bypassed by C1816; U1806 integrates V_SENSE against it (R1815, C1820) and clamps the gate through D1801 when 56.4 mA is reached.



Current ceiling amplifier, 56.4 mA
C1816: V_LIMIT reference bypass
R1811: V_LIMIT divider top
R1812: V_LIMIT divider bottom
C1806: U1806 V+ pin 5 bypass



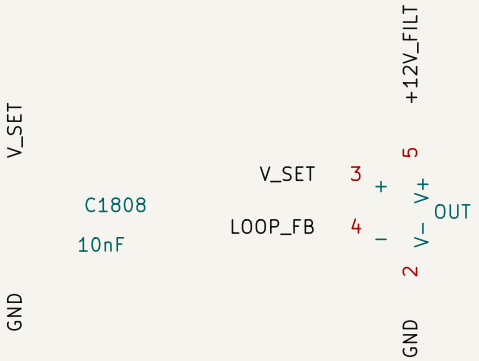
Ceiling integrator input, V_SENSE

Ceiling integrator, U1806 (C0G)

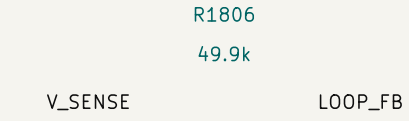
PLACE: R1811, R1812 and C1816 at U1806 pin 3; C1820 tight between pins 4 and 1.

ROUTE: V_LIMIT is a reference node: short and guarded; LIMIT_OUT runs to D1801 and to U1803A pin 1.

OPA197IDBV



Loop error integrator, gate drive
C1802: Rail bulk bypass
C1805: U1802 V+ pin 5 bypass
FB1801: Rail ferrites
C1808: Command filter, V_SET (C0G)



Loop integrator input, V_SENSE

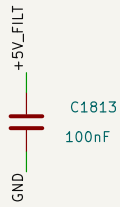
Gate clamp steering diode

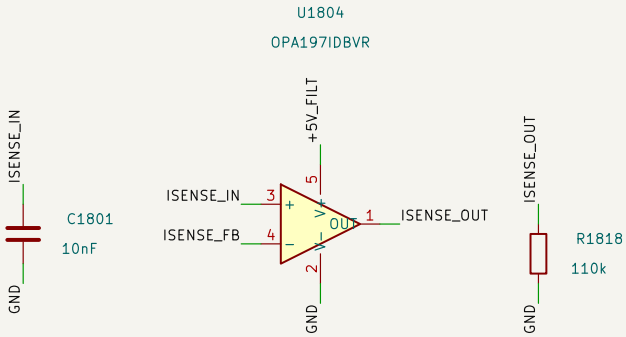
PLACE: R1813 (1 k) is required: U1802 drives 1 nF
R1814 at the gate.

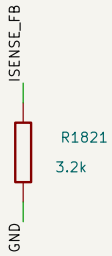
ROUTE: LOOP_FB and GATE are the loop's nodes: ke

6. Current monitor and output divider

U1804 amplifies the filtered V_SENSE (R1802, C1801) by 4.125 (R1817, R1821, C1819) to ISENSE_OUT; R1818 defines it unpowered; R1808 and R1810 halve it to ISENSE_DIV with C1815 shunting pickup; R1819 delivers BRAKE_ISENSE and D1803 clamps it.



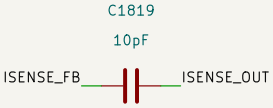




Current monitor amplifier, gain 4.125
C1801: Monitor input filter, ISENSE_IN (C0G)
R1821: Monitor gain–set, ISENSE_FB to GND (0.1 %)
R1818: ISENSE_OUT pull–down, unpowered 0 V
C1813: U1804 V+ pin 5 bypass

Monitor input series, V_SENSE

Monitor gain feedback, U1804



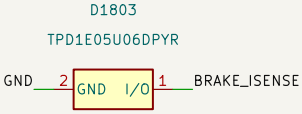
Monitor amplifier compensation

Monitor /2 divider top (0.1 %)

Monitor /2 divider bottom (0.1 %)

ISENSE_DIV midpoint shunt (C0G)

Series output resistor



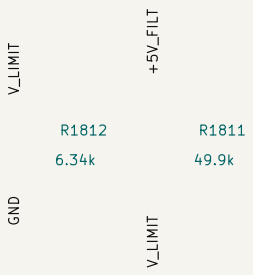
ESD clamp on BRAKE_ISENSE

PLACE: R1817, R1821 and C1819 tight to U1804 pins 1 and 4; pull the ground pour back from under ISENSE_FB (plane capacitance changes the 10 pF compensation).

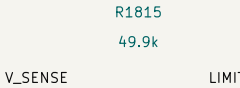
PLACE: C1815 at ISENSE_DIV with a short return; R1808 and R1810 side by side (0.1 %, 25 ppm pair).

PLACE: D1803's ground via on the connector ground that BRAKE_ISENSE leaves through.

ROUTE: BRAKE_ISENSE toward the MCU must not touch LOOP_FB or V_SENSE; the buffer exists to keep digital return currents off them.



Current ceiling amplifier, 56.4 mA
C1816: V_LIMIT reference bypass
R1811: V_LIMIT divider top
R1812: V_LIMIT divider bottom
C1806: U1806 V+ pin 5 bypass



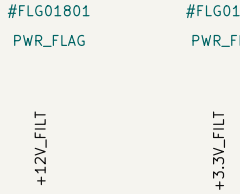
Ceiling integrator input, V_SENSE

PLACE: R1811, R1812 and C1816 at U1

ROUTE: V_LIMIT is a reference node: sh

9. Power drive declarations

These nets have an explicit ERC power

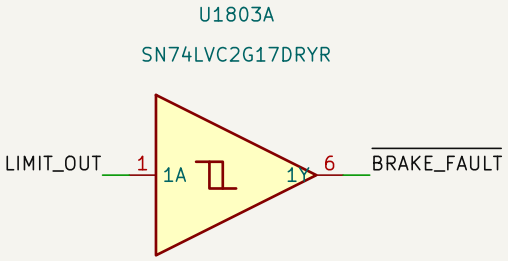


Power driven:
+12V_FILT

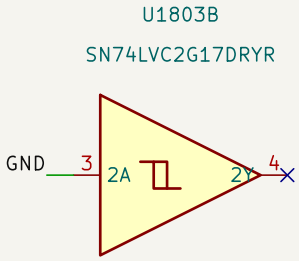
Power driv
+3.3V_FILT

7. Fault buffer

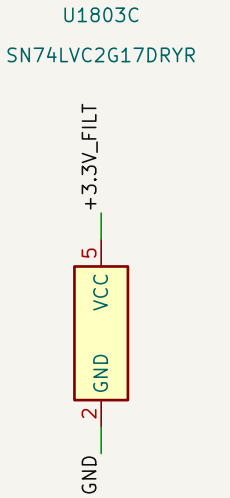
U1803A buffers LIMIT_OUT to the active-low BRAKE_FAULT; R1820 taps it for the instrument port. 2A is grounded and 2Y is open.



Unit 1: Schmitt buffer, LIMIT_OUT to BRAKE_FAULT



Unit 2: Schmitt buffer, LIMIT_OUT to BRAKE_FAULT



Power unit
C1814: U1803C VCC pin 5 bypass

Instrument tap, BRAKE_FAULT

PLACE: U1803A near U1806 with its bypass C1814 at pin 5.

ROUTE: BRAKE_FAULT is a switched-domain output with Ioff: the placing board terminates it with 10 k to GND on the MCU side.

DESIGN NOTES

A0=VDD 0x49

DESIGN CONTRACT

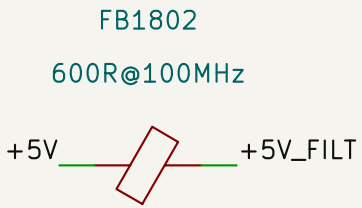
DAC-programmed linear constant-current sink de
3.3 V on I2C feeding a 0.19512 precision divider
device over a 10 ohm Kelvin shunt, a second OP

0-1.006 V ground-referenced current monitor be
and an S115Q flyback across the in-block 2-po
kicad-libs docs/brake-current-sink-design.md;
auto-annotation orders by sheet position), so ev
1. I2C, NOT SPI, AND THE ADDRESS IS ONE RESIS
1k for 0x49, and analog_output_0_3v3_dac80501
reaches only the first two. A0 is re-sampled dur
rather than a clean failure; never lift that resisto
2. THIS BLOCK OWNS NO BUS TERMINATIONS and
BUS SEGMENT: the DAC-side pair on the SWITCHE
VDD+0.3 V digital-input absolute maximum and
because the SN74CB3Q3245 is open by default.
3. THE 110k OUTPUT PULL-DOWN STAYS ON ISEN
3.1095k, ratio 0.49283, −1.43%) and it is a 1%
error budget. General rule: anything whose job is
parallel with a divider leg becomes part of the R
4. BRAKE_ISENSE IS 0-1.006 V FROM A 1.849 ko
the monitor amp stuck at its own +5V_FILT rail,
of the divider, never on ISENSE_OUT. A ceiling ev
or dead, not zero current.

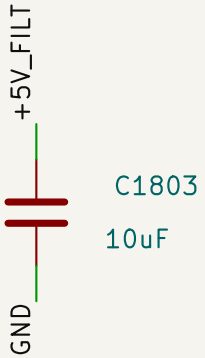
5. BRAKE_FAULT IS A SWITCHED-DOMAIN OUTPUT
TERMINATION, a 10k pull-down to GND, which me
the rail is known up. It is a continuous limiter in
6. FIRMWARE MUST WRITE GAIN (4h) = 0x0101 BE
reference, so the reference alarm holds the outp
READABLE in STATUS, which is why this block is
7. THE FOUR 10 nF FILTER AND COMPENSATION C
dielectric is piezoelectric, this board is mechanic
mechanically generated torque artifact in a torqu
8. V_LIMIT STAYS 5 V-DERIVED AND THE GATE DRI
back to 5 V leaves 90 mV of worst-corner gate-
9. PWR_FLAG on +12V_FILT, +5V_FILT and +3.3V_
10. TWO INSTANCES NEED SEPARATE SHEETS or th
SPI2C and DAC_A0. The ferrites parallel, the PWR

8. Supply ferrites and bypass

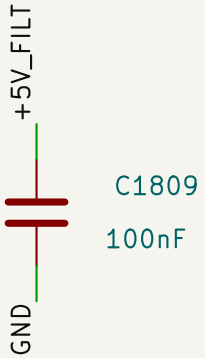
FB1801 filters +12V to +12V_FILT for U1802 (C1802, C1805); FB1802 filters +5V to +5V_FILT for U1804, U1806 and V_LIMIT (C1803, C1806, C1809, C1813); FB1803 filters +3.3V to +3.3V_FILT for U1801 and U1803A (C1804, C1807, C1810, C1814).



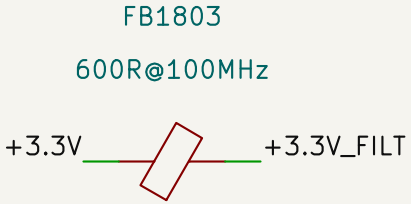
Rail ferrites



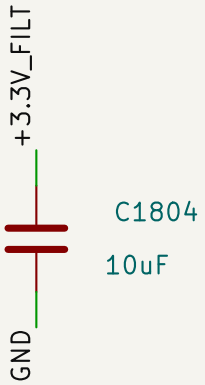
Rail bulk bypass



+5V_FILT bypass at R1811, V_LIMIT top



Rail ferrites

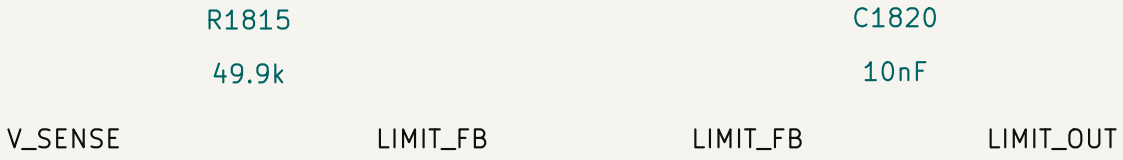


Rail bulk bypass

PLACE: One 100 nF at each supply pin it serves: C1805 at U1802 pin 5, C1813 at U1804 pin 5, C1806 at U1806 pin 5, C1809 at R1811 (the V_LIMIT divider top), C1807 and C1810 at U1801 pin 1, C1814 at U1803C pin 5; the 10 uF parts beside their ferrites.

ROUTE: +12V, +5V and +3.3V arrive at the ferrites' pad 1 (PWR_12V_LOCAL, PWR_5V_LOCAL and PWR_3V3_LOCAL vias, convention 1); the filtered rails stay inside the block.

C1816: V_LIMIT reference bypass
R1811: V_LIMIT divider top
R1812: V_LIMIT divider bottom
C1806: U1806 V+ pin 5 bypass



Ceiling integrator input, V_SENSE

Ceiling integrator, U1806 (C0G)

PLACE: R1811, R1812 and C1816 at U1806 pin 3; C1820 tight between pins 4 and 1.

ROUTE: V_LIMIT is a reference node: short and guarded; LIMIT_OUT runs to D1801 and to U1803A pin 1.

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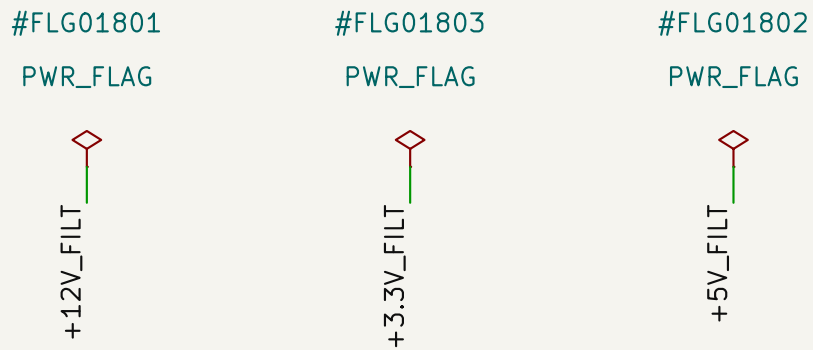
9. Power drive declarations

These nets have an explicit ERC power source declaration.



Power driven:
+12V_FILT

Power driven:
+3.3V_FILT

Power driven:
+5V_FILT

INTERFACES

+36V — +36V

Coil supply, switched domain: J1801 pin 2 and the flyback cathode of D1802, bypassed by C1817 and C1818; the pass device drops what the coil does not.

+12V — +12V

Gate−drive supply of the loop amplifier U1802, through FB1801 to +12V_FILT.

+5V — +5V

Regulated 5.0 V for the ceiling and monitor amplifiers and the V_LIMIT divider, through FB1802 to +5V_FILT (OPA197 minimum 4.5 V).

+3.3V — +3.3V

Switched 3.3 V: DAC and fault−buffer supply through FB1803 to +3.3V_FILT; the reference of both mode straps.

GND — GND

Return of the shunt R1816, the amplifiers, the DAC and the bypass; the brake return joins board ground once, at the power−stage return point.

SCL — SCL

I2C clock to U1801 pin 6 (SCLK/SCL); single−pin net, the board fits the pull−up.

SDA — SDA

I2C data, U1801 pin 8 (SDIN/SDA), address 0x49; single−pin net, the board fits the pull−up.

BRAKE_ISENSE — BRAKE_ISENSE

Current monitor, 0−1.006 V for 0−48.78 mA from a 1.849 kohm source; needs a >= 1 Mohm load; a ceiling event reads 1.163 V; 0 V means unpowered.

$\overline{\text{BRAKE_FAULT}}$ — $\overline{\text{BRAKE_FAULT}}$

Active−low continuous limiter indication from U1803A 1Y; high−Z (Ioff) whenever +3.3V_FILT is down, so the board owes a 10 k pull−down to GND.

$\overline{\text{BRAKE_FAULT_INST}}$ — $\overline{\text{BRAKE_FAULT_INST}}$

Instrument tap of $\overline{\text{BRAKE_FAULT}}$ through R1820 (1 k); INSTRUMENT class.

Instrument tap of BRAKE_FAULT through R1820 (1 k), INSTRUMENT class.

OPERATION

Signal path: U1801 VOUT (pin 2, 0–2.5 V) –> R1801 (10 k), R1803 and R1804 (3.2 k each): ratio 3.2/16.4 = 0.19512, so VSET_RAW is 0–0.4878 V –> R1805 (49.9 k) and C1808 (10 nF), the 303 Hz command filter (tau about 525 us with the divider's 2.58 kohm) –> V_SET –> U1802 + (pin 3). U1802 integrates the error against V_SENSE (R1806 49.9 k, C1812 10 nF) and drives GATE through R1813 (1 k); U1805 sources through R1816 (10 ohm), so V_SENSE follows V_SET and the coil current is 0–48.78 mA at 10 mV per mA, loop crossover about 295 Hz. R1814 (49.9 k) holds the gate off when nothing drives it.

Coil and pass device: the coil hangs from +36V at J1801 pin 2 to COIL_LO (pin 1), the drain of U1805; D1802 (S115Q, 150 V 1 A Schottky) is the flyback across the terminal. At 48.8 mA with a hot 605 ohm coil and the rail 5 % low the pass device keeps 4.2 V; with a cold 467 ohm coil and the rail 5 % high it drops 14.5 V and dissipates about 0.71 W. The 36 V rail is required: a 24 V rail cannot reach rated current.

Independent ceiling: U1806 integrates V_SENSE (R1815 49.9 k, C1820 10 nF) against V_LIMIT = 5 V x 6.34/(49.9 + 6.34) = 564 mV from +5V_FILT (R1811, R1812, C1816): 56.4 mA, 115 % of rated. Above it LIMIT_OUT falls and pulls GATE down through D1801; U1803A (Schmitt, 5.5 V–tolerant input) buffers LIMIT_OUT, near 4.96 V idle and about 0.4 V while limiting, to $\overline{\text{BRAKE_FAULT}}$, a continuous indication, not a latch. V_LIMIT comes from +5V_FILT, not VREFIO, so the ceiling is independent of the DAC and the loop and a sagging rail lowers it.

Monitor: U1804 at gain 1 + 10/3.2 = 4.125 (R1817, R1821, C1819 10 pF) reads V_SENSE through R1802 (49.9 k) and C1801 (10 nF) –> ISENSE_OUT 0–2.012 V; R1808 and R1810 (3.2 k each) halve it to ISENSE_DIV, 0–1.006 V; R1819 (249 ohm) delivers BRAKE_ISENSE and D1803 clamps ESD. The load must be >= 1 Mohm; the divider bounds any single fault, including U1804 stuck at its 5 V rail, to 2.48 V at the pin; a ceiling event reads 1.163 V, above full scale. R1818 (110 k) stays on ISENSE_OUT, not the midpoint, where it would shift the ratio by −1.43 %.

I2C, address 0x49: R1809 (1 k to +3.3V_FILT) selects I2C and R1807 (1 k to +3.3V_FILT) sets A0 to 0x49 (the analog output block takes 0x48). A0 is re–sampled during the first byte of every frame: never lift R1807 without re–wiring it in the same operation. No bus termination inside; SCL and SDA leave as single–pin nets and the board fits one 2.2 k pull–up pair per segment. Firmware writes GAIN (4h) = 0x0101 before any DATA write; until then the reference alarm holds VOUT at 0 V, readable in STATUS.

Supplies and rules: +12V, +5V and +3.3V are filtered by FB1801, FB1802 and FB1803 to +12V_FILT, +5V_FILT and +3.3V_FILT, each carrying a PWR_FLAG; +36V binds to the same switched domain. The five 10 nF capacitors C1801, C1808, C1812, C1815 and C1820 are C0G: 1 mV of piezoelectric charge on V_SET is 0.1 mA of coil current. V_LIMIT stays 5 V–derived and the gate drive stays 12 V. $\overline{\text{BRAKE_FAULT}}$ reads asserted whenever the switched rail is off. Two instances need separate sheets.

DESIGN NOTES

A0=VDD 0x49

DESIGN CONTRACT

DAC–programmed linear constant–current sink delivering 0–48.78 mA into a 24 V magnetic particle brake coil from a 36 V rail: a DAC80501ZDGSR at 3.3 V on I2C feeding a 0.19512 precision divider, an OPA197 integrating error amplifier on a ferrite–filtered 12 V rail driving a BUK7D36–60EX pass device over a 10 ohm Kelvin shunt, a second OPA197 as an independent 56.4 mA current ceiling that clamps the gate through a Schottky, a third as a 0–1.006 V ground–referenced current monitor behind a /2 output divider, an SN74LVC2G17 buffering the ceiling event out as active–low $\overline{\text{BRAKE_FAULT}}$, and an S115Q flyback across the in–block 2–position 3.5 mm vertical coil terminal. The full derivation, connection table, BOM and open items are in kicad–libs docs/brake–current–sink–design.md; this note carries only what breaks silently without it. Designators are not stable (KiCad auto–annotation orders by sheet position), so everything below is named by net.

1. I2C, NOT SPI, AND THE ADDRESS IS ONE RESISTOR. SPI2C is strapped to +3.3V_FILT through 1k for I2C mode; A0 is strapped to +3.3V_FILT through 1k for 0x49, and analog_output_0_3v3_dac80501 takes 0x48. A0 is a FOUR–STATE pin (AGND 0x48, VDD 0x49, SDA 0x4A, SCL 0x4B), so a rail strap reaches only the first two. A0 is re–sampled during the first byte of EVERY frame, so a floating A0 gives an address that changes between frames rather than a clean failure; never lift that resistor without re–wiring it in the same operation.
2. THIS BLOCK OWNS NO BUS TERMINATIONS and must not gain any. SCL and SDA leave as single–pin nets. The board fits ONE 2.2k pull–up pair PER BUS SEGMENT: the DAC–side pair on the SWITCHED 3.3 V rail, because an always–on pull–up reaching a DAC whose VDD is at 0 V exceeds the VDD+0.3 V digital–input absolute maximum and back–feeds +3.3V_FILT through the internal clamps; the MCU–side pair on the ALWAYS–ON rail, because the SN74CB3Q3245 is open by default. Two instances each carrying pull–ups would halve the resistance.
3. THE 110k OUTPUT PULL–DOWN STAYS ON ISENSE_OUT, upstream of the /2 divider. On the midpoint it parallels the bottom leg (110k||3.2k = 3.1095k, ratio 0.49283, −1.43%) and it is a 1% 100ppm/C thick film against the divider's 0.1% 25ppm/C pair, so it would dominate the ratio's whole error budget. General rule: anything whose job is to define a node when the amplifier is dead belongs on the AMP side of a divider; anything in parallel with a divider leg becomes part of the RATIO.
4. BRAKE_ISENSE IS 0–1.006 V FROM A 1.849 kohm SOURCE AND NEEDS A >=1 Mohm LOAD. The /2 divider is what bounds a single fault, including the monitor amp stuck at its own +5V_FILT rail, to 2.48 V on a connector pin; the 249 ohm series resistor's input end is on ISENSE_DIV, downstream of the divider, never on ISENSE_OUT. A ceiling event reads 1.163 V, deliberately ABOVE full scale, so a limit event stays visible. 0 V means unpowered or dead, not zero current.
5. $\overline{\text{BRAKE_FAULT}}$ IS A SWITCHED–DOMAIN OUTPUT WITH Ioff, so it is high–Z whenever +3.3V_FILT is down and THE PLACING BOARD OWES THE MCU–SIDE TERMINATION, a 10k pull–down to GND, which means the line reads ASSERTED whenever the switched rail is off. Firmware must only interpret it while the rail is known up. It is a continuous limiter indication, not a latch. Do not substitute the 2G14; it is the inverter.
6. FIRMWARE MUST WRITE GAIN (4h) = 0x0101 BEFORE ANY DATA WRITE. At 3.3 V the reset default 0x0001 is out of spec against the 2.5 V internal reference, so the reference alarm holds the output at 0 V until that write lands. That is a safety property, not a bug, and over I2C the alarm is READABLE in STATUS, which is why this block is on I2C at all.
7. THE FOUR 10 nF FILTER AND COMPENSATION CAPACITORS MUST BE C0G, not X7R or X5R, and so must the divider midpoint's 10 nF. Class–2 dielectric is piezoelectric, this board is mechanically coupled to a stepper and a hand–driven joystick, and 1 mV on V_SET is 0.1 mA of coil current. A mechanically generated torque artifact in a torque measurement cannot be filtered out. C0G at 10 nF forces an 0805 body; take the area.
8. V_LIMIT STAYS 5 V–DERIVED AND THE GATE DRIVE STAYS 12 V. Moving V_LIMIT to 12 V rescales the 564 mV ceiling threshold; moving the loop amp back to 5 V leaves 90 mV of worst–corner gate–drive margin with a −7.5 mV/degC tempco.
9. PWR_FLAG on +12V_FILT, +5V_FILT and +3.3V_FILT is required: the ferrites break driver propagation. GND is flagged once at board level, not here.
10. TWO INSTANCES NEED SEPARATE SHEETS or their local nets merge: +12V_FILT, +5V_FILT, +3.3V_FILT, V_SET, V_SENSE, V_LIMIT, ISENSE_DIV, GATE, SPI2C and DAC_A0. The ferrites parallel, the PWR_FLAGs conflict, and DAC_A0 merging would silently put both DACs on one address.

36 V protected terminal input, vertical | series diode, TPS1HTC100 high-side switch, instrument taps

Protected and electronically switched 36 V high-voltage input front end on a VERTICAL, top-entry 2-position 5.08 mm pluggable terminal block — Phoenix MSTBVA 2,5/2-G-5,08, OW-CONN-TBH-1X02-5P08-VERT, on the local orb_weaver_tht copy of the MSTBVA footprint — with a SBRT15U50SP5 reverse-polarity series diode and a TPS1HTC100-Q1 smart high-side switch providing adjustable current limit, inrush/soft-start control, analog load-current sense, thermal shutdown, and an integrated inductive discharge clamp.

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Entry and reverse-polarity protection

J501 brings the external 36 V supply onto HV_RAW (pin 2) and GND (pin 1); D501 in series passes it to HV_IN and blocks a reversed supply.

36 V entry, 2-pos 5.08 mm vertical

PLACE: J501's footprint has pin 1 at its origin (the horizontal part's is 10 mm off its pads), its pads are 2.08 x 3.6 mm on a 1.4 mm drill, and its courtyard reaches 5.3 mm inboard of pin 1, so leave that room behind it. Do not rotate it 180 degrees to turn the entry around; pin order would swap GND and the supply in board space.

PLACE: Keep D501 close to J501 so HV_RAW stays short; the whole supply current flows through D501, so give its PowerDI 5 pad copper on both sides for heat.

ROUTE: HV_RAW is the PWR_HV_ENTRY class (0.5 mm clearance) and HV_IN PWR_HV_LOCAL; size the copper for the full supply current and keep the GND return beside the supply path from the terminal onward.

3. Enable, diagnostics and latch inputs

R501 feeds EN from ENABLE and R506 holds it low; R502 and R503 bring DIAG_ENABLE and LATCH to their pins through 10 k each.

ENABLE series, 1 k

DIAG_ENABLE series, 10 k

LATCH series, 10 k

PLACE: Place R506 at pin 2 with a short return to GND; the series resistors can sit between the ports and the pins.

ROUTE: All four nodes are low-current Default-class logic; nothing critical.

4. Fault output

R507 pulls the open-drain $\overline{\text{FAULT}}$ pin up to +3.3V_MCU; R504 brings the flag out as $\overline{\text{FAULT}}$.

$\overline{\text{FAULT}}$ output series, 10 k

PLACE: Place R507 near pin 4; R504 anywhere between the pin node and the port.

ROUTE: +3.3V_MCU here is only the pull-up supply (Default class); the flag is low-current logic.

5. Instrument taps

R510, R511 and R512 tap ENABLE, DIAG_ENABLE and $\overline{\text{FAULT}}$ through 1 k each for the INSTRUMENT ports; the block owns these signals, so the taps live here (convention 14).

Instrument tap, 1 k

Instrument tap, 1 k

Instrument tap, 1 k

PLACE: Place the three taps in a row near the port side of the block; their port copper is a via each (convention 1).

ROUTE: INSTRUMENT class to the ports; a tap that is not probed is left open at the via.

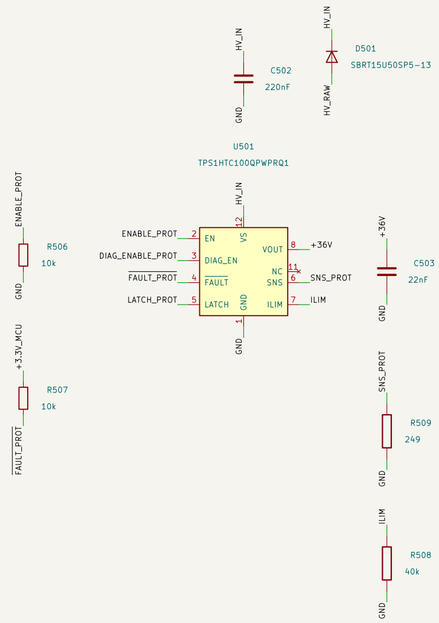
7. Power drive declarations

These nets have an explicit ERC power source declaration.

Power driven: HV_IN

2. High-side switch, input bypass, current limit and output

C502 bypasses HV_IN at the VS pins (12–14); U501 passes HV_IN to +36V when EN is high; R508 on ILIM (pin 7) sets the current limit; C503 holds the switched output.



Smart high-side switch, analog current sense
C502: HV input bypass at VS; D501: Reverse-polarity series diode; one per VS pins 12, 13, 14
C503: Switched-rail output capacitor; one per VOUT pins 8, 9, 10
R508: ILIM programming, 40 k
R507: $\overline{\text{FAULT}}$ pull-up to +3.3V_MCU, 10 k
R506: EN pull-down, 10 k
R509: SNS sense resistor, 249 ohm

PLACE: Place C502 at U501 pins 12–14 with a short return to pin 1 / the thermal pad.

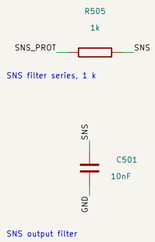
PLACE: Place R508 directly at pin 7 with a short return to GND; place C503 at VOUT (pins 8–10) with a short return to GND. Tie the thermal pad (pin 15) to GND copper with vias; the pad is the heat path at the current limit.

ROUTE: Short, wide copper on both C502 legs; it is the local reservoir for the switch's turn-on.

ROUTE: VS (pins 12–14) and VOUT (pins 8–10) are the PWR_HV_LOCAL current path; keep each group of pins tied together with wide copper. ILIM is a low-current Default-class node that must never be left open.

6. Load-current sense output

R509 at the SNS pin converts the sense current to a voltage; R505 and C501 filter it toward the SNS port.



SNS filter series, 1 k

SNS output filter

PLACE: Place R509 directly at pin 6 with a short return to GND, then R505 and C501 after it; a resistor or capacitor between the pin and R509 changes the sense ratio.

ROUTE: SNS_PROT is a low-level analog node; route it away from the HV_IN and +36V copper and give C501 a return next to R509's.

INTERFACES

+3.3V_MCU — +3.3V_MCU

Pull-up supply for $\overline{\text{FAULT}}$ through R507 (10 k); draws only the pull-up current.

ENABLE — ENABLE

Logic input through R501 (1 k) to EN; R506 holds EN low, so the rail is off until driven.

DIAG_ENABLE — DIAG_ENABLE

Logic input through R502 (10 k) to DIAG_EN; must be driven high for SNS and the diagnostics, open reads low.

LATCH — LATCH

Logic input through R503 (10 k) to LATCH; selects latched shutdown or automatic retry after a fault.

$\overline{\text{FAULT}}$ — $\overline{\text{FAULT}}$

Fault flag through R504 (10 k), pulled up to +3.3V_MCU by R507; low during a fault.

SNS — SNS

Analog load-current output, about 0.31 V per ampere, filtered by R505 and C501 (10 us).

HV_IN — HV_IN

Protected input after D501 and before the switch, bypassed by C502; available to the board unswitched.

+36V — +36V

Switched, current-limited 36 V rail from U501 VOUT (pins 8–10); off until ENABLE is high.

GND — GND

Return: terminal pin 1, switch GND (pin 1) and thermal pad (pin 15), bypass, ILIM and sense returns.

DIAG_ENABLE_INST — DIAG_ENABLE_INST

Instrument tap of DIAG_ENABLE through R511 (1 k), INSTRUMENT class.

ENABLE_INST — ENABLE_INST

Instrument tap of ENABLE through R510 (1 k), INSTRUMENT class.

$\overline{\text{FAULT_INST}}$ — $\overline{\text{FAULT_INST}}$

Instrument tap of $\overline{\text{FAULT}}$ through R512 (1 k), INSTRUMENT class.

OPERATION

Signal path: J501 pin 2 (HV_RAW) -> D501 anode to cathode -> HV_IN -> U501 VS (pins 12–14) -> VOUT (pins 8–10) -> +36V: J501 pin 1 is GND. D501 (SBRT15U50SP5-13, 50 V 15 A super-barrier rectifier) blocks a reversed supply and drops under 0.44 V at these currents. The terminal is polarity-definite: pin 2 is the supply, pin 1 the return. HV_IN is also a port, so a board can take the protected but unswitched supply. Electrically this is the horizontal hv_input_36V_terminal_2pos_5p08_protected block plus three instrument taps.

U501 (TPS1HTC100-Q1, 6 to 60 V, 83 mohm) switches the rail. EN (pin 2) is driven from ENABLE through R501 (1 k) and held low by R506 (10 k): +36V is off until the board drives ENABLE high; supply UVLO releases at about 5.4 V. R508 (40 k) on ILIM programs the current limit at about 1.2 A typical (0.9 to 1.4 A) with a 1.5x transient peak allowance; ILIM must never float (an open ILIM selects the 7.3 A internal default). Thermal shutdown is 165 C typical, retry about 2 ms.

DIAG_ENABLE reaches DIAG_EN (pin 3) through R502 (10 k) and must be driven high for the analog sense and the open-load and short-to-battery diagnostics; open, the internal 200 to 500 k pull-down reads it low. LATCH reaches pin 5 through R503 (10 k) and selects latched shutdown or automatic retry. $\overline{\text{FAULT}}$ (pin 4) is open-drain, pulled up by R507 (10 k) to +3.3V_MCU and brought out through R504 (10 k): low during a fault. ENABLE, DIAG_ENABLE and $\overline{\text{FAULT}}$ each have a 1 k instrument tap (R510, R511, R512) to the INSTRUMENT-class ports; shared bus lines are tapped by the board, these are the block's own signals (convention 14).

SNS (pin 6) sources load current divided by 800 (KSNS): R509 (249 ohm) at the pin converts it to about 0.311 V per ampere (about 0.37 V at the 1.2 A limit; a fault drives about 5.2 mA, about 1.3 V). R505 (1 k) and C501 (10 nF) filter it toward the SNS port (10 us); keeping R509 at the pin and the filter after it preserves the ratio.

No TVS and no power LED in this variant. C502 (220 nF, 100 V X7R) bypasses HV_IN; C503 (22 nF, 100 V) holds the switched output. J501 is the vertical, top-entry Phoenix MSTBVA 2,5/2-G-5,08 (rated 12 A 250 V); the wire leaves perpendicular to the board, so the enclosure needs an aperture above it plus clearance for the plug body, its screw heads and the wire loop.

DESIGN NOTES

R_ILIM I_CL min typ max source 49.9k / 50k 0.73 A 0.92 A 1.11 A datasheet 40k 0.9 A 1.2 A 1.4 A computed 25k 1.5 A 1.96 A 2.3 A datasheet 20k 1.9 A 2.5 A 2.9 A computed 16.7k 2.3 A 3.0 A 3.5 A datasheet 10k 4.0 A 5.3 A 6.3 A datasheet open or GND 6.1 A 7.3 A 8.6 A datasheet — do not use

DESIGN CONTRACT

Protected and electronically switched 36 V high-voltage input front end on a VERTICAL, top-entry 2-position 5.08 mm pluggable terminal block (Phoenix MSTBVA 2,5/2-G-5,08, OW-CONN-TBH-1X02-5P08-VERT, on the local orb_weaver_tht copy of the MSTBVA footprint) with a SBRT15U50SP5 reverse-polarity series diode and a TPS1HTC100-Q1 smart high-side switch providing adjustable current limit, inrush/soft-start control, analog load-current sense, thermal shutdown, and an integrated inductive discharge clamp. ENABLE is pulled low through R506 (10 k) so the rail stays off until driven. No input TVS or power-present LED is populated in this variant, unlike the 24 V barrel-jack and terminal-block variants. Intended for HV/VMOT entry rails feeding stepper drivers, brake supplies, and downstream regulation.
Electrically the horizontal hv_input_36V_terminal_2pos_5p08_protected block, port for port (+3.3V_MCU, +36V, DIAG_ENABLE, ENABLE, GND, HV_IN, LATCH, SNS, -FAULT), plus three 1 k instrument taps (ENABLE_INST, DIAG_ENABLE_INST, -FAULT_INST) on the block's own signals. Signal path is terminal pin 2 to HV_RAW, through D501 to HV_IN and the TPS1HTC100 VS pins, out VOUT as the switched +36V rail; terminal pin 1 is GND. THE TERMINAL IS POLARITY-DEFINITE, not polarity-agnostic.
R508 = 40 kOhm on ILIM sets the current limit, giving I_CL of 0.9 A min / 1.2 A typ / 1.4 A max with a 1.5x transient peak allowance, and R509 = 249 Ohm at the SNS pin sets the SNS scaling (about 0.311 V per ampere): R505 (1 k) and C501 (10 nF) filter it toward the SNS port. DIAG_EN must be driven HIGH or the analog sense and the open-load and short-to-battery diagnostics are all disabled, and ILIM must NEVER float — floating selects the internal default limit and is itself a fault state per datasheet Table 6-2. -FAULT is open-drain, pulled up by R507 (10 k) to +3.3V_MCU, which is only that pull-up supply: it and LATCH are Default-class ports, and no placing board should class +3.3V_MCU as a rail.
The terminal is pad-COMPATIBLE with the horizontal 5.08 mm part, not pad-IDENTICAL: pitch is 5.08 mm in both and pin order ascends in +x in both, but the pad goes from 2.5 x 2.5 mm on a 1.5 mm drill to 2.08 x 3.6 mm on a 1.4 mm drill, the Phoenix-recommended layout for the MSTBVA pin. The narrow-axis annular ring shrinks from 0.50 mm to 0.34 mm, still about 1.9x the 0.18 mm JLCPCB routine PTH minimum; the pad-to-pad gap improves from 2.58 mm to 3.00 mm against the 0.50 mm clearance PWR_HV_ENTRY asks of HV_IN; hole-to-hole is 3.68 mm against a 0.45 mm minimum. Re-run DRC after placing rather than trusting these numbers.
The footprint anchor differs: the horizontal PHOENIX_1757242 is anchored 10 mm off its own pads with pin 1 at (3.54, -10.00); the vertical puts pin 1 at the origin. Migrating an existing placement means changing the part and then moving the footprint by (+3.54, -10.00) so pad 1 returns to its old absolute position; the connector is the only part whose pads move. The mechanical envelope inverts: relative to pad 1 the horizontal courtyard runs x −3.79 to +8.87, y −2.25 to +10.25; the vertical runs x −4.04 to +9.13, y −5.30 to +4.30. Outboard overhang collapses from 10.25 mm to 4.30 mm so the terminal can move inboard, while the inboard keepout grows from 2.25 mm to 5.30 mm, so a swap in place can collide with whatever sits behind the connector even though the pitch did not change.
DO NOT ROTATE 180 DEGREES to make the wire entry face outboard: pin order runs the same direction in both footprints, so rotating swaps GND and the +36 V raw input in board space. The series diode blocks reverse polarity only while the input supply FLOATS; on a board whose GND is shared with USB, the pyControl port, and the InstrumentPort, a reversed terminal puts the supply across those grounds instead and the diode protects nothing. The wire leaves perpendicular to the board, so the enclosure needs an aperture above the terminal plus clearance for the mating MSTB plug body, its screw heads, and the wire loop.

Circuit and PCB layout guidance
Migrated from the saved library sheet; circuit and PCB unchanged
Orb Weaver

Sheet: /hv_input_36V_terminal_2pos_5p08_protected_vertical/
File: hv_input_36V_terminal_2pos_5p08_protected_vertical.kicad_sch

Title: 36 V protected terminal input, switched, vertical

Size: A2	Date: 2026-10-04	**Rev: Source migration 1**
KiCad E.D.A. 10.0.6		Id: 5/20

1 2 3 4

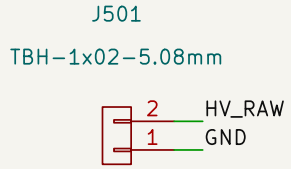
36 V protected terminal input, vertical | series diode, TPS1HTC100 high-side switch, instrument tap

Protected and electronically switched 36 V high-voltage input front end on a VERTICAL, top-entry 2-position 5.08 mm pluggable terminal block – Phoenix MSTBVA 2,5/2 thermal shutdown, and an integrated inductive discharge clamp.

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Entry and reverse-polarity protection

J501 brings the external 36 V supply onto HV_RAW (pin 2) and GND (pin 1); D501 in series passes it to HV_IN and blocks a reversed supply.



36 V entry, 2-pos 5.08 mm vertical

PLACE: J501's footprint has pin 1 at its origin (the horizontal part's is 10 mm off its pads), its pads are 2.08 x 3.6 mm on a 1.4 mm drill, and its courtyard reaches 5.3 mm inboard of pin 1, so leave that room behind it. Do not rotate it 180 degrees to turn the entry around; pin order would swap GND and the supply in board space.

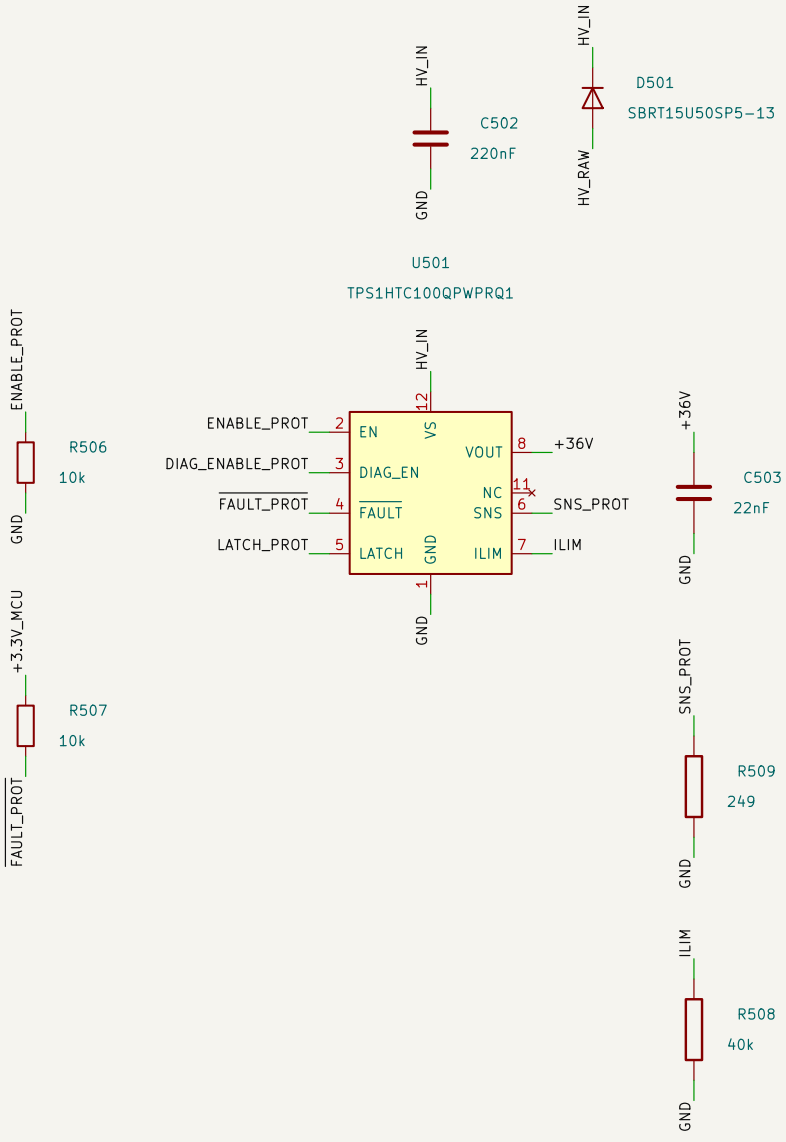
PLACE: Keep D501 close to J501 so HV_RAW stays short; the whole supply current flows through D501, so give its PowerDI 5 pad copper on both sides for heat.

ROUTE: HV_RAW is the PWR_HV_ENTRY class (0.5 mm clearance) and HV_IN PWR_HV_LOCAL; size the copper for the full supply current and keep the GND return beside the supply path from the terminal onward.

-5,08, OW-CONN-TBH-1X02-5P08-VERT, on the local orb_weaver_tht copy of the MSTBVA footprint — with a SBRT15U50SP5 reverse-polarity series diode and a TPS1HTC1

2. High-side switch, input bypass, current limit and output

C502 bypasses HV_IN at the VS pins (12–14); U501 passes HV_IN to +36V when EN is high; R508 on ILIM (pin 7) sets the current limit; C503 holds the switched output.



Smart high-side switch, analog current sense
C502: HV input bypass at VS; D501: Reverse-polarity series diode; one per VS pins 12, 13, 14
C503: Switched-rail output capacitor; one per VOUT pins 8, 9, 10
R508: ILIM programming, 40 k
R507: $\overline{\text{FAULT}}$ pull-up to +3.3V_MCU, 10 k
R506: EN pull-down, 10 k
R509: SNS sense resistor, 249 ohm

PLACE: Place C502 at U501 pins 12–14 with a short return to pin 1 / the thermal pad.

PLACE: Place R508 directly at pin 7 with a short return to GND; place C503 at VOUT (pins 8–10) with a short return to GND. Tie the thermal pad (pin 15) to GND copper with vias; the pad is the heat path at the current limit.

ROUTE: Short, wide copper on both C502 legs; it is the local reservoir for the switch's turn-on.

ROUTE: VS (pins 12–14) and VOUT (pins 8–10) are the PWR_HV_LOCAL current path; keep each group of pins tied together with wide copper. ILIM is a low-current Default-class node that must never be left open.

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Entry and reverse-polarity protection

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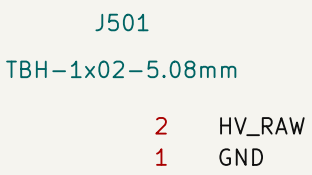

36 V entry, 2-pos 5.08 mm vertical

PLACE: J501's footprint has pin 1 at its origin (the horizontal part's is 10 mm off its pads), its pads are 2.08 x 3.6 mm on a 1.4 mm drill, and its courtyard reaches 5.3 mm inboard pin 1, so leave that room behind it. Do not rotate it 180 degrees to turn the entry around; pin order would swap GND and the supply in board space.

PLACE: Keep D501 close to J501 so HV_RAW stays short; the whole supply current flows through D501, so give its PowerDI 5 pad copper on both sides for heat.

ROUTE: HV_RAW is the PWR_HV_ENTRY class (0.5 mm clearance) and HV_IN PWR_HV_LOCAL; size the copper for the full supply current and keep the GND return beside the supply path terminal onward.

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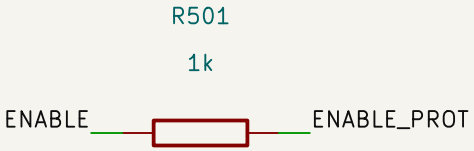
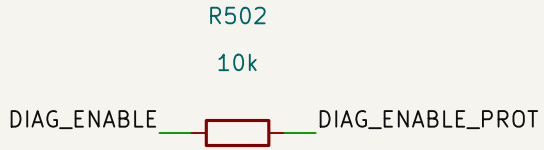
3. Enable, diagnostics and latch inputs

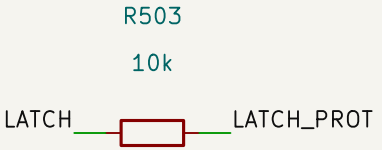
R501 feeds EN from ENABLE and R506 holds it low; R502 and R503 bring DIAG_ENABLE and LATCH to their pins through 10 k each.



ENABLE series, 1 k



DIAG_ENABLE series, 10 k



LATCH series, 10 k

PLACE: Place R506 at pin 2 with a short return to GND; the series resistors can sit between the ports and the pins.

ROUTE: All four nodes are low-current Default-class logic; nothing critical.

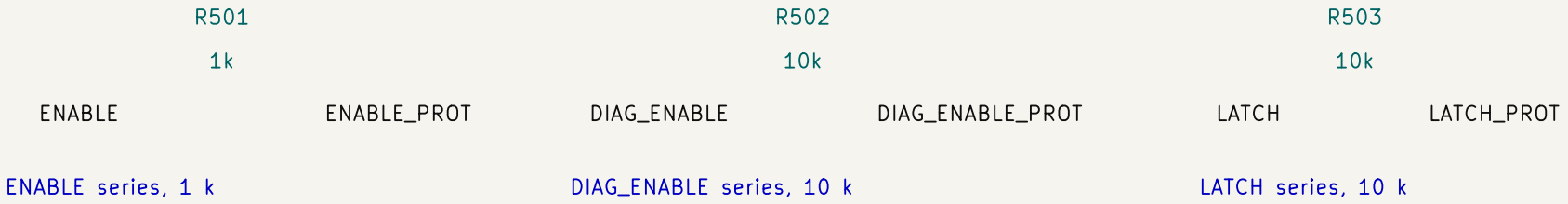
PLACE: J501's footprint has pin 1 at its origin (the horizontal part's is 10 mm off its pads), its pads are 2.08 x 3.6 mm on a 1.4 mm drill, and its courtyard reaches 5.3 mm inboard
pin 1, so leave that room behind it. Do not rotate it 180 degrees to turn the entry around; pin order would swap GND and the supply in board space.

PLACE: Keep D501 close to J501 so HV_RAW stays short; the whole supply current flows through D501, so give its PowerDI 5 pad copper on both sides for heat.

ROUTE: HV_RAW is the PWR_HV_ENTRY class (0.5 mm clearance) and HV_IN PWR_HV_LOCAL; size the copper for the full supply current and keep the GND return beside the supply path
terminal onward.

3. Enable, diagnostics and latch inputs

R501 feeds EN from ENABLE and R506 holds it low; R502 and R503 bring DIAG_ENABLE and LATCH to their pins through 10 k each.



ENABLE series, 1 k

DIAG_ENABLE series, 10 k

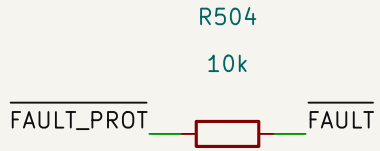
LATCH series, 10 k

PLACE: Place R506 at pin 2 with a short return to GND; the series resistors can sit between the ports and the pins.

ROUTE: All four nodes are low-current Default-class logic; nothing critical.

4. Fault output

R507 pulls the open-drain $\overline{\text{FAULT}}$ pin up to +3.3V_MCU; R504 brings the flag out as $\overline{\text{FAULT}}$.



$\overline{\text{FAULT}}$ output series, 10 k

PLACE: Place R507 near pin 4; R504 anywhere between the pin node and the port.

ROUTE: +3.3V_MCU here is only the pull-up supply (Default class); the flag is low-current logic.

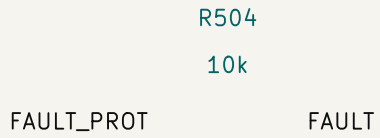
ENABLE series, 1 k DIAG_ENABLE series, 10 k LATCH series, 10 k

PLACE: Place R506 at pin 2 with a short return to GND; the series resistors can sit between the ports and the pins.

ROUTE: All four nodes are low-current Default-class logic; nothing critical.

4. Fault output

R507 pulls the open-drain FAULT pin up to +3.3V_MCU; R504 brings the flag out as FAULT.



FAULT output series, 10 k

PLACE: Place R507 near pin 4; R504 anywhere between the pin node and the port.

ROUTE: +3.3V_MCU here is only the pull-up supply (Default class); the flag is low-current logic.

5. Instrument taps

R510, R511 and R512 tap ENABLE, DIAG_ENABLE and $\overline{\text{FAULT}}$ through 1 k each for the INSTRUMENT ports; the block owns these signals, so the taps live here (convention 14).

Instrument tap, 1 k Instrument tap, 1 k Instrument tap, 1 k

PLACE: Place the three taps in a row near the port side of the block; their port copper is a via each (convention 1).

ROUTE: INSTRUMENT class to the ports; a tap that is not probed is left open at the via.

R508: ILIM programming, 40 k

R507: FAULT pull-up to +3.3V_MCU, 10 k
R506: EN pull-down, 10 k
R509: SNS sense resistor, 249 ohm

PLACE: Place C502 at U501 pins 12–14 with a short return to pin 1 / the thermal pad.

PLACE: Place R508 directly at pin 7 with a short return to GND; place C503 at VOUT (pins 8–10) with a short return to GND. Tie the thermal pad (pin 15) to GND copper with vias; th pad is the heat path at the current limit.

ROUTE: Short, wide copper on both C502 legs; it is the local reservoir for the switch's turn-on.

ROUTE: VS (pins 12–14) and VOUT (pins 8–10) are the PWR_HV_LOCAL current path; keep each group of pins tied together with wide copper. ILIM is a low-current Default-class node must never be left open.

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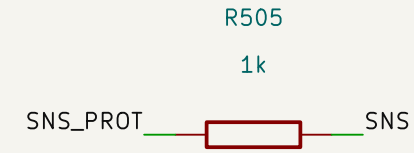
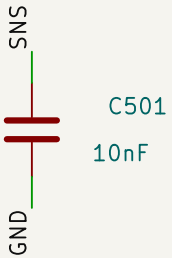
6. Load-current sense output

R509 at the SNS pin converts the sense current to a voltage; R505 and C501 filter it toward the SNS port.



SNS filter series, 1 k



SNS output filter

PLACE: Place R509 directly at pin 6 with a short return to GND, then R505 and C501 after it; a resistor or capacitor between the pin and R509 changes the sense ratio.

ROUTE: SNS_PROT is a low-level analog node; route it away from the HV_IN and +36V copper and give C501 a return next to R509's.

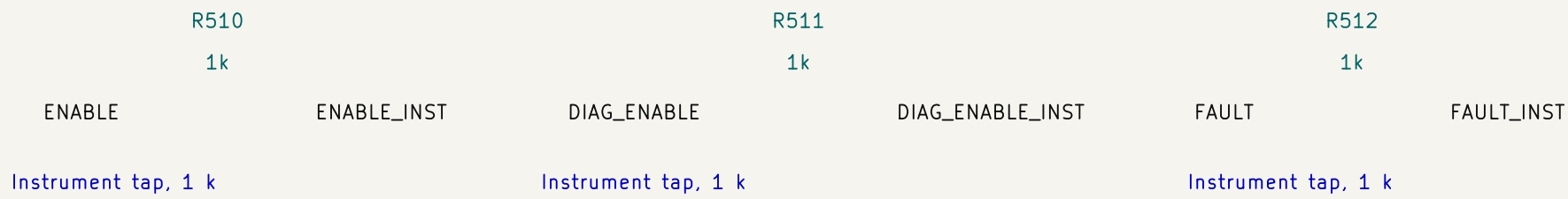
FAULT output series, 10 k

PLACE: Place R507 near pin 4; R504 anywhere between the pin node and the port.

ROUTE: +3.3V_MCU here is only the pull-up supply (Default class); the flag is low-current logic.

5. Instrument taps

R510, R511 and R512 tap ENABLE, DIAG_ENABLE and FAULT through 1 k each for the INSTRUMENT ports; the block owns these signals, so the taps live here (convention 14).



Instrument tap, 1 k

Instrument tap, 1 k

Instrument tap, 1 k

PLACE: Place the three taps in a row near the port side of the block; their port copper is a via each (convention 1).

ROUTE: INSTRUMENT class to the ports; a tap that is not probed is left open at the via.

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7. Power drive declarations

These nets have an explicit ERC power source declaration.

Power driven: HV_IN

Q1 smart high-side switch providing adjustable current limit, inrush/soft-start control, analog load

INTERFACES

+3.3V_MCU — +3.3V_MCU

Pull-up supply for $\overline{\text{FAULT}}$ through R507 (10 k); draws only the pull-up current.

ENABLE — ENABLE

Logic input through R501 (1 k) to EN; R506 holds EN low, so the rail is off until driven.

DIAG_ENABLE — DIAG_ENABLE

Logic input through R502 (10 k) to DIAG_EN; must be driven high for SNS and the diagnostics, open reads low.

LATCH — LATCH

Logic input through R503 (10 k) to LATCH; selects latched shutdown or automatic retry after a fault.

$\overline{\text{FAULT}}$ — $\overline{\text{FAULT}}$

Fault flag through R504 (10 k), pulled up to +3.3V_MCU by R507; low during a fault.

SNS — SNS

Analog load-current output, about 0.31 V per ampere, filtered by R505 and C501 (10 us).

HV_IN — HV_IN

Protected input after D501 and before the switch, bypassed by C502; available to the board unswitched.

+36V — +36V

Switched, current-limited 36 V rail from U501 VOUT (pins 8-10); off until ENABLE is high.

GND — GND

Return: terminal pin 1, switch GND (pin 1) and thermal pad (pin 15), bypass, ILIM and sense returns.

DIAG_ENABLE_INST — DIAG_ENABLE_INST

Instrument tap of DIAG_ENABLE through R511 (1 k), INSTRUMENT class.

ENABLE_INST — ENABLE_INST

Instrument tap of ENABLE through R510 (1 k), INSTRUMENT class.

$\overline{\text{FAULT_INST}}$ — $\overline{\text{FAULT_INST}}$

Instrument tap of $\overline{\text{FAULT}}$ through R512 (1 k), INSTRUMENT class.

DIAG_ENABLE_INST DIAG_ENABLE_INST

Instrument tap of DIAG_ENABLE through R511 (1 k), INSTRUMENT class.

ENABLE_INST ENABLE_INST

Instrument tap of ENABLE through R510 (1 k), INSTRUMENT class.

FAULT_INST FAULT_INST

Instrument tap of FAULT through R512 (1 k), INSTRUMENT class.

OPERATION

Signal path: J501 pin 2 (HV_RAW) −> D501 anode to cathode −> HV_IN −> U501 VS (pins 12−14) −> VOUT (pins 8−10) −> +36V; J501 pin 1 is GND. D501 (SBRT15U50SP5−13, 50 V 15 A super−barrier rectifier) blocks a reversed supply and drops under 0.44 V at these currents. The terminal is polarity−definite: pin 2 is the supply, pin 1 the return. HV_IN is also a port, so a board can take the protected but unswitched supply. Electrically this is the horizontal hv_input_36V_terminal_2pos_5p08_protected block plus three instrument taps.

U501 (TPS1HTC100−Q1, 6 to 60 V, 83 mohm) switches the rail. EN (pin 2) is driven from ENABLE through R501 (1 k) and held low by R506 (10 k): +36V is off until the board drives ENABLE high; supply UVLO releases at about 5.4 V. R508 (40 k) on ILIM programs the current limit at about 1.2 A typical (0.9 to 1.4 A) with a 1.5x transient peak allowance; ILIM must never float (an open ILIM selects the 7.3 A internal default). Thermal shutdown is 165 C typical, retry about 2 ms.

DIAG_ENABLE reaches DIAG_EN (pin 3) through R502 (10 k) and must be driven high for the analog sense and the open−load and short−to−battery diagnostics; open, the internal 200 to 500 k pull−down reads it low. LATCH reaches pin 5 through R503 (10 k) and selects latched shutdown or automatic retry. $\overline{\text{FAULT}}$ (pin 4) is open−drain, pulled up by R507 (10 k) to +3.3V_MCU and brought out through R504 (10 k); low during a fault. ENABLE, DIAG_ENABLE and $\overline{\text{FAULT}}$ each have a 1 k instrument tap (R510, R511, R512) to the INSTRUMENT−class ports; shared bus lines are tapped by the board, these are the block's own signals (convention 14).

SNS (pin 6) sources load current divided by 800 (KSNS): R509 (249 ohm) at the pin converts it to about 0.311 V per ampere (about 0.37 V at the 1.2 A limit; a fault drives about 5.2 mA, about 1.3 V). R505 (1 k) and C501 (10 nF) filter it toward the SNS port (10 us); keeping R509 at the pin and the filter after it preserves the ratio.

No TVS and no power LED in this variant. C502 (220 nF, 100 V X7R) bypasses HV_IN; C503 (22 nF, 100 V) holds the switched output. J501 is the vertical, top−entry Phoenix MSTBVA 2,5/2−G−5,08 (rated 12 A 250 V): the wire leaves perpendicular to the board, so the enclosure needs an aperture above it plus clearance for the plug body, its screw heads and the wire loop.

DESIGN NOTES

R_ILIM I_CL min typ max source 49.9k / 50k 0.73 A 0.92 A 1.11 A datasheet 40k 0.9 A 1.2 A 1.4 A computed 25k 1.5 A 1.96 A 2.3 A datasheet 20k 1.9 A 2.5 A 2.9 A computed 16.7k 2.3 A 3.0 A 3.5 A datasheet 10k 4.0 A 5.3 A 6.3 A datasheet open or GND 6.1 A 7.3 A 8.6 A datasheet − do not use

DESIGN CONTRACT

Protected and electronically switched 36 V high−voltage input front end on a VERTICAL, top−entry 2−position 5.08 mm pluggable terminal block (Phoenix MSTBVA 2,5/2−G−5,08, OW−CONN−TBH−1X02−5P08−VERT, on the local orb_weaver_tht copy of the MSTBVA footprint) with a SBRT15U50SP5 reverse−polarity series diode and a TPS1HTC100−Q1 smart high−side switch providing adjustable current limit, inrush/soft−start control, analog load−current sense, thermal shutdown, and an integrated inductive discharge clamp. ENABLE is pulled low through R506 (10 k) so the rail stays off until driven. No input TVS or power−present LED is populated in this variant, unlike the 24 V barrel−jack and terminal−block variants. Intended for HV/VMOT entry rails feeding stepper drivers, brake supplies, and downstream regulation.
Electrically the horizontal hv_input_36V_terminal_2pos_5p08_protected block, port for port (+3.3V_MCU, +36V, DIAG_ENABLE, ENABLE, GND, HV_IN, LATCH, SNS, ~FAULT), plus three 1 k instrument taps (ENABLE_INST, DIAG_ENABLE_INST, ~FAULT_INST) on the block's own signals. Signal path is terminal pin 2 to HV_RAW, through D501 to HV_IN and the TPS1HTC100 VS pins, out VOUT as the switched +36V rail; terminal pin 1 is GND. THE TERMINAL IS POLARITY−DEFINITE, not polarity−agnostic.
R508 = 40 kOhm on ILIM sets the current limit, giving I_CL of 0.9 A min / 1.2 A typ / 1.4 A max with a 1.5x transient peak allowance, and R509 = 249 Ohm at the SNS pin sets the SNS scaling (about 0.311 V per ampere); R505 (1 k) and C501 (10 nF) filter it toward the SNS port. DIAG_EN must be driven HIGH or the analog sense and the open−load and short−to−battery diagnostics are all disabled, and ILIM must NEVER float − floating selects the internal default limit and is itself a fault state per datasheet Table 4−2. ~FAULT is open−drain, pulled up by R507 (10 k) to +3.3V_MCU, which is only that pull−up supply: it and LATCH are Default−class ports, and no placing board should class +3.3V_MCU as a rail.
The terminal is pad−COMPATIBLE with the horizontal 5.08 mm part, not pad−IDENTICAL: pitch is 5.08 mm in both and pin order ascends in +x in both, but the pad goes from 2.5 x 2.5 mm on a 1.5 mm drill to 2.08 x 3.6 mm on a 1.4 mm drill, the Phoenix−recommended layout for the MSTBVA pin. The narrow−axis annular ring shrinks from 0.50 mm to 0.34 mm, still about 1.9x the 0.18 mm JLCPCB routine PTH minimum; the pad−to−pad gap improves from 2.58 mm to 3.00 mm against the 0.50 mm clearance PWR_HV_ENTRY asks of HV_IN; hole−to−hole is 3.68 mm against a 0.45 mm minimum. Re−run DRC after placing rather than trusting these numbers.
The footprint anchor differs: the horizontal PHOENIX_1757242 is anchored 10 mm off its own pads with pin 1 at (3.54, −10.00); the vertical puts pin 1 at the origin. Migrating an existing placement means changing the part and then moving the footprint by (+3.54, −10.00) so pad 1 returns to its old absolute position; the connector is the only part whose pads move. The mechanical envelope inverts: relative to pad 1 the horizontal courtyard runs x −3.79 to +8.87, y −2.25 to +10.25; the vertical runs x −4.04 to +9.13, y −5.30 to +4.30. Outboard overhang collapses from 10.25 mm to 4.30 mm so the terminal can move inboard, while the inboard keepout grows from 2.25 mm to 5.30 mm, so a swap in place can collide with whatever sits behind the connector even though the pitch did not change.
DO NOT ROTATE 180 DEGREES to make the wire entry face outboard: pin order runs the same direction in both footprints, so rotating swaps GND and the +36 V raw input in board space. The series diode blocks reverse polarity only while the input supply FLOATS; on a board whose GND is shared with USB, the pyControl port, and the InstrumentPort, a reversed terminal puts the supply across those grounds instead and the diode protects nothing. The wire leaves perpendicular to the board, so the enclosure needs an aperture above the terminal plus clearance for the mating MSTB plug body, its screw heads, and the wire loop.