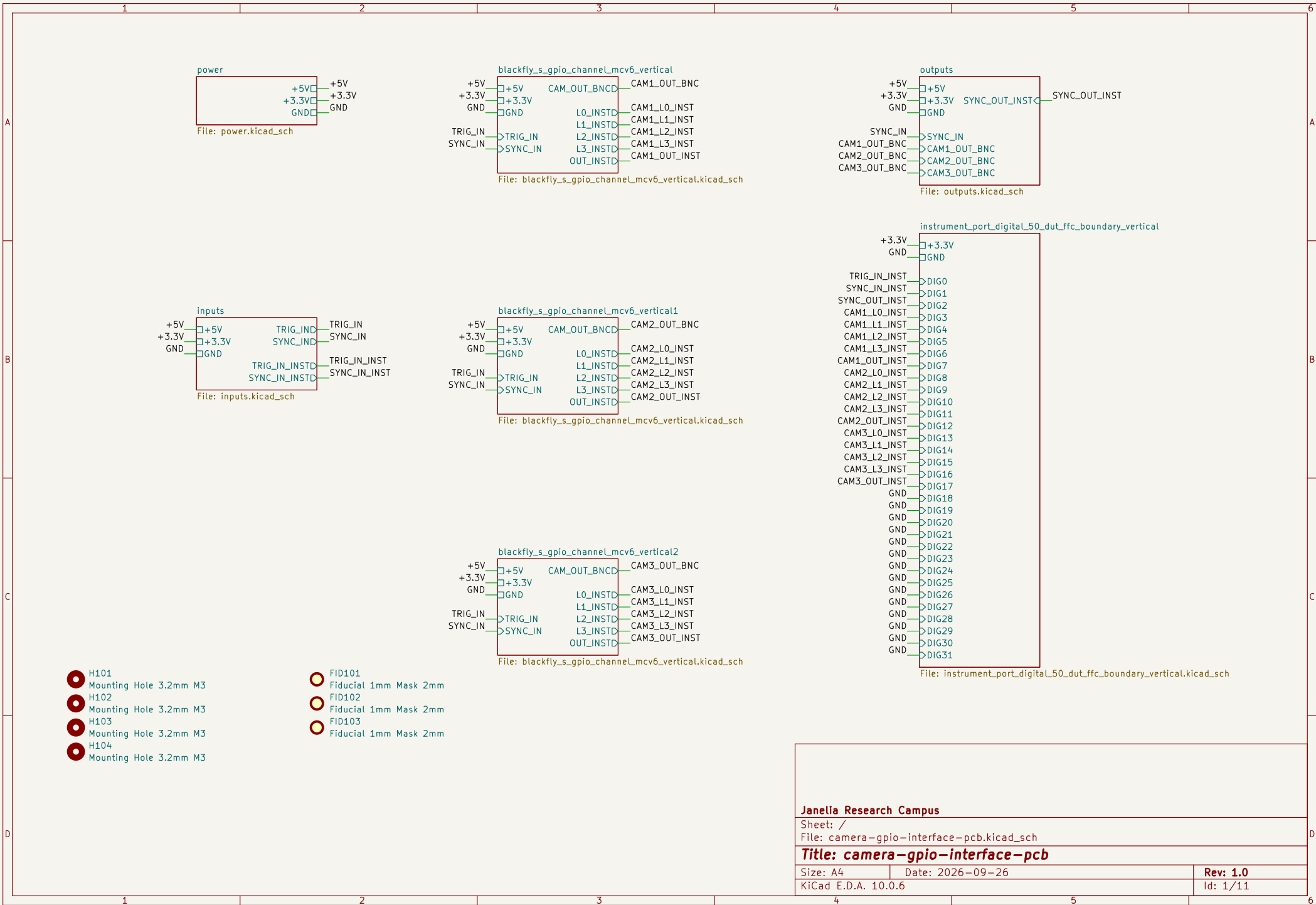
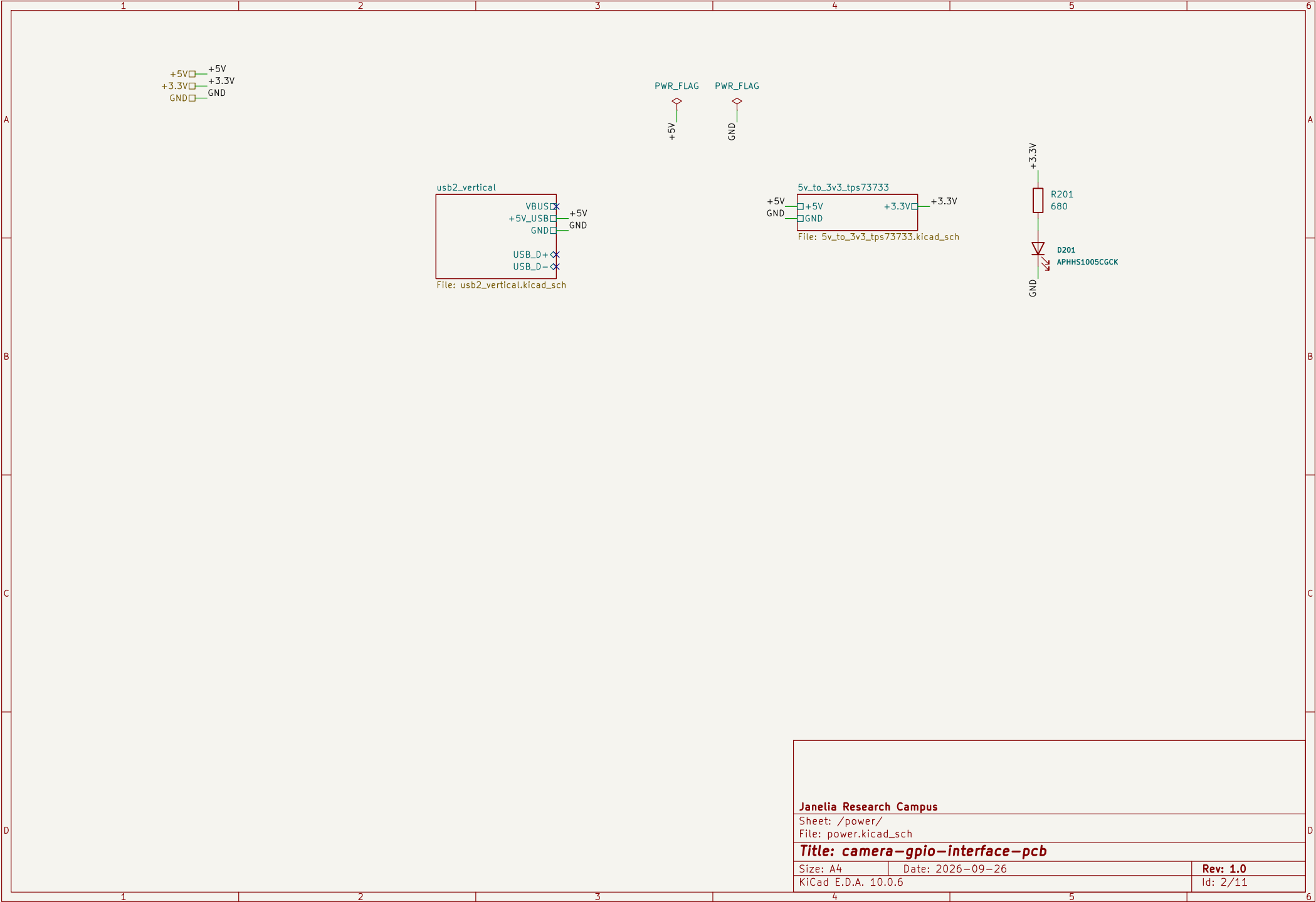






Janelia Research Campus

Sheet: /power/
File: power.kicad_sch

Title: camera-gpio-interface-pcb

Size: A4

Date: 2026-09-26

Rev: 1.0

KiCad E.D.A. 10.0.6

Id: 2/11

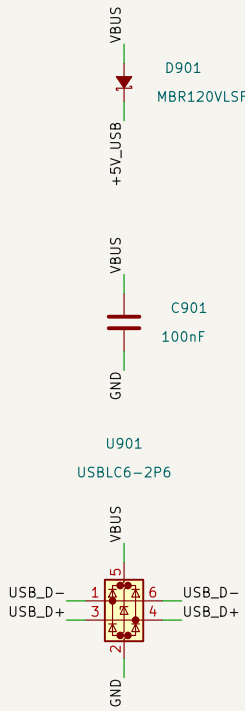
USB–C USB2 device port, vertical receptacle | USB4145, USBLC6 clamp, Rd 5.1 k, 5 V diode–OR

USB–C USB2 device–port front end on a VERTICAL, top–entry receptacle: GCT USB4145–03–0070–C, OW–CONN–USB–C–USB2–SMD–VERT, 16P USB2–only, SMT contacts plus four through–hole shell legs, 7.46 mm tall.

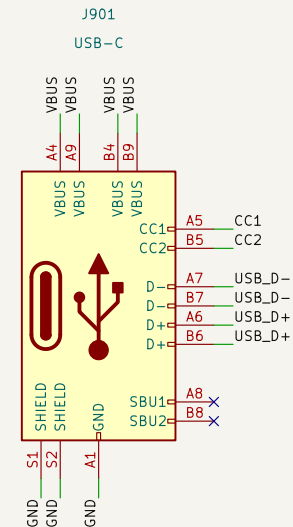
Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Receptacle and ESD clamp

J901 brings VBUS, GND, D+/D–, CC1/CC2 and the shell onto the board; U901 clamps USB_D+, USB_D– and VBUS to GND right at the receptacle. C901 holds the raw VBUS node at the clamp; D901 passes VBUS to +5V_USB and blocks the other 5 V source from feeding back into the host.



ESD clamp on D+, D– and VBUS
C901: VBUS bypass at the clamp
D901: Diode–OR Schottky



usb–connector

PLACE: Place U901 hard against J901 with a ground via at its pin 2; route each data line in one I/O pad and out the other.

PLACE: Place J901's four shell–leg holes and two locator pegs before pouring GND or routing the port; the part does not seat without them.

PLACE: Place C901 between U901 pin 5 and the GND via; D901 sits where +5V_USB leaves the block at its port via.

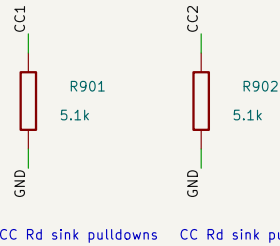
ROUTE: USB_D+ and USB_D– are the USB_HS pair; equal length, coupled at the class gap, brought to the block boundary already coupled.

ROUTE: Jump one leg of each pair once at the body centre for the A/B tie; the 0.3 mm gap at the outer contacts is unroutable.

ROUTE: VBUS and +5V_USB are Default–class rails for the port's 5 V budget; +5V_USB is picked up at the port via by the placing board.

2. CC sink declaration

R901 and R902 (5.1 k) pull CC1 and CC2 to GND; the port presents itself as a sink; nothing reads the source's advertisement.



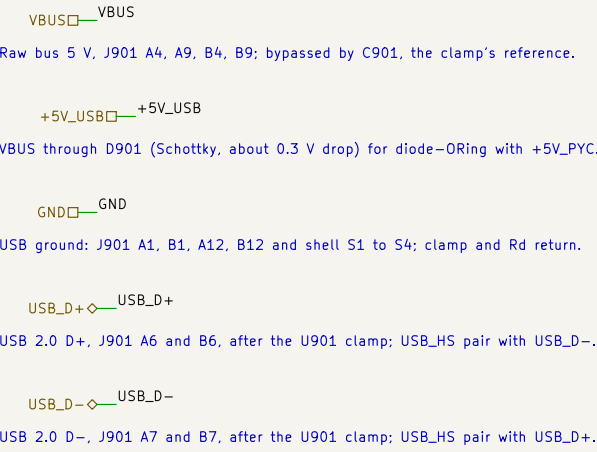
PLACE: Keep R901 at A5 and R902 at B5 with short returns; no other load on CC1 or CC2.
ROUTE: CC1 and CC2 are Default–class local nets that end at the resistors.

3. Power drive declarations

These nets have an explicit ERC power source declaration.



INTERFACES



INTERNAL NETS

CC1: Configuration channel for one plug orientation, J901 A5 to R901 (Rd, 5.1 k to GND); nothing reads it.
CC2: Configuration channel for the other orientation, J901 B5 to R902 (Rd, 5.1 k to GND); nothing reads it.

OPERATION

Signal path: J901 D+ (A6, B6) and D– (A7, B7) pass U901's I/O pads to USB_D+ and USB_D–; both receptacle rows are tied so either plug orientation works. SBU1 and SBU2 (A8, B8) are no–connect; USB2 only, for an RP2040–class device controller.

CC: R901 on CC1 (A5) and R902 on CC2 (B5), 5.1 k to GND, declare a UFP (sink). Nothing reads the CC level, so budget the load against a default–power source unless the host is known to advertise 1.5 A or 3 A.

ESD: U901 (USBLC6–2P6) clamps D+, D– and VBUS; 3.5 pF max per line, 1.7 pF max line to line, 6 V minimum VBUS breakdown, 12 V typical clamp at 1 A 8/20 us, IEC 61000–4–2 level 4 (15 kV air and contact). Clamp performance is set by connection inductance; pin 2 to a ground via, each data line in one I/O pad and out the other.

VBUS: C901 (100 nF) bypasses the raw bus; D901 (MBR120VLSFT1G, 20 V 1 A Schottky, 0.34 V max at 1 A, 0.6 mA leakage at 25 C) makes +5V_USB for diode–ORing with the pyControl block's +5V_PYC. The shell pads S1 to S4 are tied to GND here; isolate them through a pad/cap network instead if the shield must float.

Land pattern (from the block's own record): contacts in two rows on opposite sides of the body at 0.5 mm pitch, every pad 0.3 mm wide; the A/B ties for D+ and D– cross at the body centre with one via jump per pair leg and equal lengths; VBUS and GND each land on four pads to be used in parallel for the 3 A rating. Four plated shell legs and two 0.71 mm locator pegs are mandatory for seating. The cable leaves perpendicular to the board (7.46 mm connector height), so the enclosure needs an aperture above it.

DESIGN CONTRACT

USB–C USB2 device–port front end on a VERTICAL, top–entry receptacle: GCT USB4145–03–0070–C, OW–CONN–USB–C–USB2–SMD–VERT, 16P USB2–only, SMT contacts plus four through–hole shell legs, 7.46 mm tall. Electrically identical to the horizontal usb2 block; USBLC6–2P6 ESD clamp on D+/D– and VBUS, 5.1k Rd pulldowns on CC1 (A5) and CC2 (B5) declaring a sink, 100nF on VBUS, a MBR120VLSFT1G series Schottky from VBUS to +5V_USB for diode–ORing with other 5 V sources (pair it with pycontrol_behavior.port_lj45's +5V_PYC), PWR_FLAG on VBUS, SBU1/SBU2 deliberately unconnected, all four shell pads S1–S4 tied to GND. Ports are VBUS, +5V_USB, GND, USB_D+, USB_D–.

Nothing reads the CC advertisement, so budget the load against a default–power source unless the host is known to advertise 1.5 A or 3 A.

Only the land pattern differs from usb2, and it differs completely, which is why this is a separate block and not a footprint swap: contacts sit in two rows on OPPOSITE sides of the body at y = +/-1.485, 0.5 mm pitch across the six inner contacts and 1.5 mm out to the outer pads, and EVERY pad is 0.3 mm wide, where the horizontal GT–USB–7047C merges A and B into one row and gives VBUS and GND 0.6 mm pads. Three consequences follow for the layout. The A/B ties are the layout's work: D+ (A6/B6) and D– (A7/B7) cross at the body centre and cannot be taken around the ends, because the 0.3 mm gap between the outer contact and the shell–leg pad is unroutable at 0.2/0.2 and the plated leg blocks every layer there, so budget one via jump for one leg of the pair and keep both legs equal length. VBUS lands on four 0.3 mm pads (A4/A9/B4/B9) and GND on four (A1/A12/B1/B12); use all four of each in parallel for the 3 A rating and drop their ties to an inner layer rather than crowding the 1.8 mm corridor between the rows, which the two data joins need. The four shell legs are plated ovals on a 1.1 x 0.6 drill at x = +/-4 and punch every layer, and the two 0.71 mm NPTH locator pegs at (x +/-4, 0) are mandatory for seating; place all six before pouring GND or routing the port. Mechanically the courtyard shrinks to x +/-5.05, y +/-2.31 from the horizontal part's x +/-6.00, y –1.25 to +6.75, so the connector stops needing about 6.75 mm of board past the contacts and can move inboard, but the cable now leaves perpendicular to the board; the enclosure needs an aperture above it plus clearance for the plug body and its wire loop, well beyond the 7.46 mm connector height.

Keep the USBLC6 hard against the receptacle with a ground via at its pin 2 and route each data line in one I/O pad and out the other (clamp performance is dominated by connection inductance), and bring USB_D+/USB_D– to the block boundary already coupled at the USB_HS netclass gap. +5V_USB leaves D901 pad 1 into a port via, where a placing board picks the rail up.

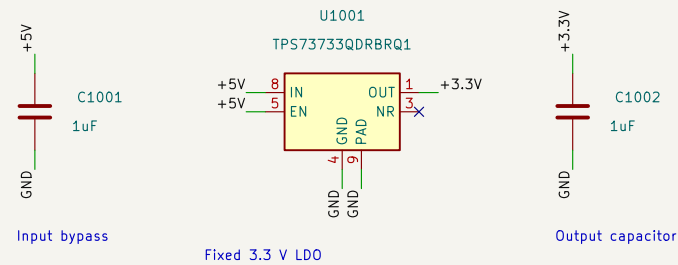
5 V to 3.3 V regulator | TPS73733 fixed 3.3 V LDO

Clean 3.3 V linear regulator from a 5 V input rail using the TI TPS73733 fixed 3.3 V 1 A LDO.

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Regulator and bypass

U1001 regulates +5V to +3.3V with EN tied to IN. C1001 bypasses IN to GND, C1002 holds OUT to GND; NR is open.



PLACE: Place C1001 at pins 8 and 4 and C1002 at pins 1 and 4 with short local ground returns; tie the thermal pad to GND copper.
ROUTE: +5V and +3.3V carry the rail classes (PWR_5V_LOCAL, PWR_3V3_LOCAL); the GND return of the pad is the regulator’s heat path as well.

INTERFACES

+5V — +5V
Input rail; also drives EN, so the regulator is on whenever it is present.

GND — GND
Common return; regulator ground pin and thermal pad.

+3.3V — +3.3V
Regulated output, 3.3 V fixed.

OPERATION

Signal path: +5V → U1001 (IN, pin 8) → +3.3V (OUT, pin 1). EN (pin 5) is tied to IN, so the regulator is on whenever +5V is present; there is no enable control inside this block.
NR (pin 3) is left open: no noise–reduction capacitor is fitted. GND (pin 4) and the thermal pad (pin 9) return to GND.
C1001 (1 uF) bypasses the input, C1002 (1 uF) is the output capacitor; both are the catalog 0402 1 uF part. The rail is rated by the TPS73733 (fixed 3.3 V, 1 A class per the catalog description); derate for the board’s actual load and dropout.

DESIGN CONTRACT

Clean 3.3 V linear regulator from a 5 V input rail using the TI TPS73733 fixed 3.3 V 1 A LDO. Intended for MCU, RP2040, TMC logic, encoder interface, and other low–voltage digital circuitry.

Circuit and PCB layout guidance
Migrated from the saved library sheet; circuit and PCB unchanged
Orb Weaver

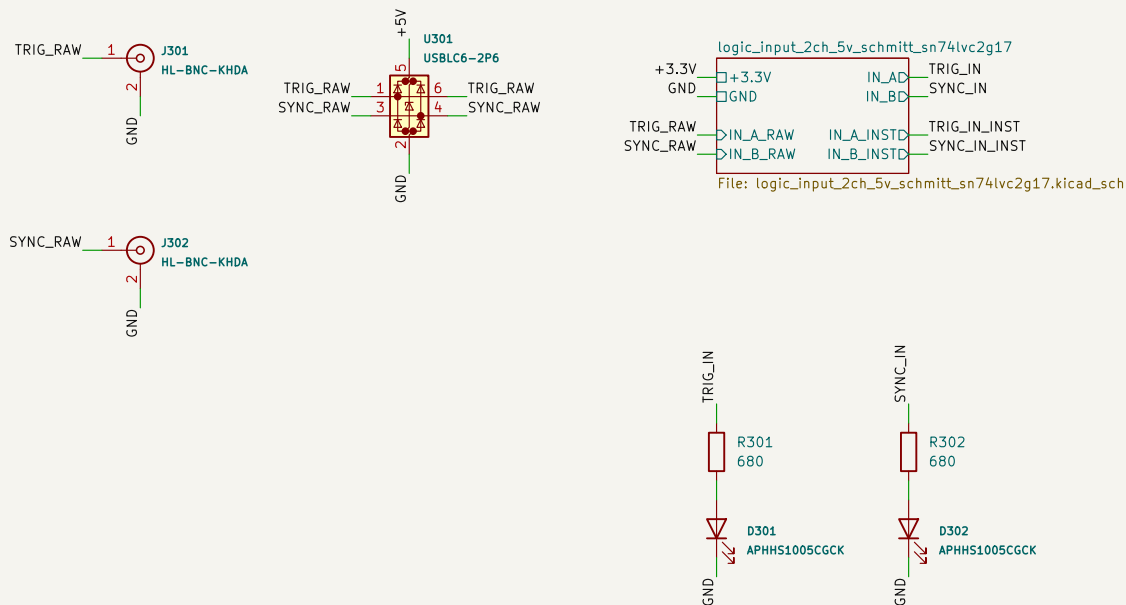
Sheet: /power/5v_to_3v3_tps73733/
File: 5v_to_3v3_tps73733.kicad_sch

Title: 5 V to 3.3 V regulator

Size: A4	Date: 2026–10–04	Rev: Source migration 1
KiCad E.D.A. 10.0.6		Id: 10/11

+5V +5V
+3.3V +3.3V
GND GND

TRIG_IN TRIG_IN
SYNC_IN SYNC_IN
TRIG_IN_INST TRIG_IN_INST
SYNC_IN_INST SYNC_IN_INST



Janelia Research Campus

Sheet: /inputs/
File: inputs.kicad_sch

Title: camera-gpio-interface-pcb

Size: A4 Date: 2026-09-26

KiCad E.D.A. 10.0.6

Rev: 1.0

Id: 3/11

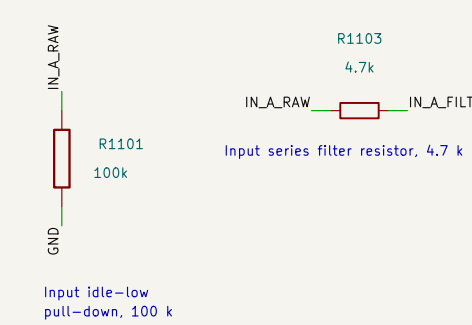
Two-channel Schmitt logic input | 4.7 k / 470 pF filters, SN74LVC2G17, pull-downs and taps

Two-channel single-ended logic input conditioner; per-channel series/RC filtering plus an SN74LVC2G17 dual Schmitt-trigger buffer that turns a 3.3 V or 5 V field-wired logic signal into clean 3.3 V logic, with a 100 ohm InstrumentPort tap on each output.

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Channel A Input filter

R1103 in series with the raw input into C1101 to GND forms the 72 kHz low-pass at 1A; R1101 holds IN_A_RAW low when nothing is plugged in.

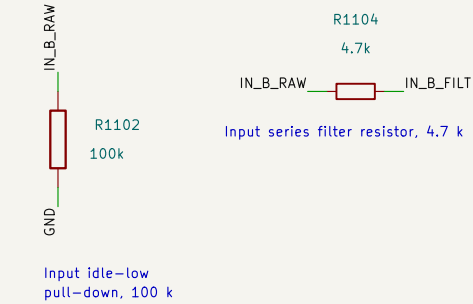


PLACE: Series resistors and filter capacitors on the input edge of the block. C1101 with a short return to GND at the buffer's pin 2 side; keep the raw pair away from motor bridge outputs with a ground reference beside it.

ROUTE: IN_A_RAW and IN_B_RAW enter as tracks (harness side); IN_A_FILT stays inside the block.

2. Channel B Input filter

The same network for channel B into 2A; R1102 holds IN_B_RAW low when unplugged.

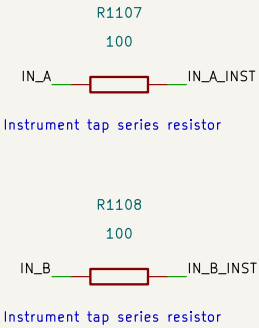


PLACE: Mirror channel A on the input edge so both channels see the same copper and the same delay.

ROUTE: IN_B_FILT stays inside the block.

3. Output pull-downs and Instrument taps

R1105/R1106 (100 k) define IN_A/IN_B while the buffer is unpowered; R1107/R1108 (100 ohm) are the series taps to IN_A_INST and IN_B_INST.

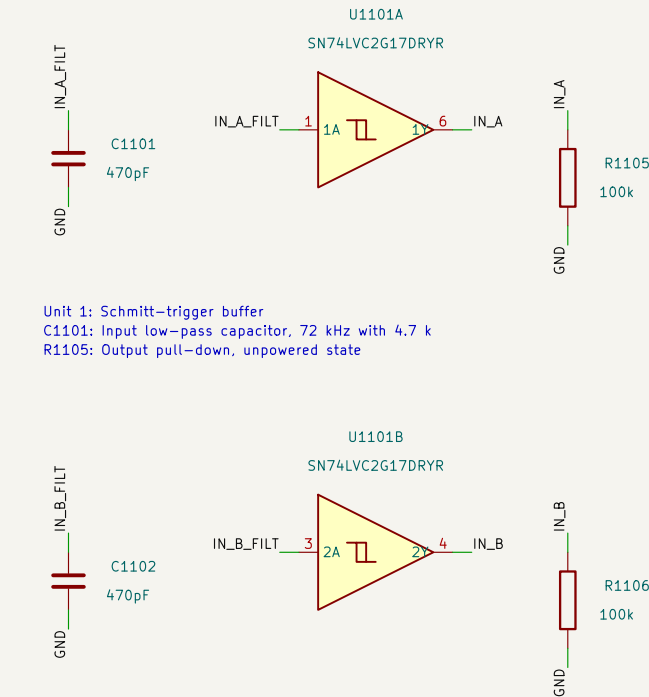


PLACE: Output pull-downs and taps on the output edge, so logic and tap nets leave on the side opposite the harness.

ROUTE: IN_A, IN_B, IN_A_INST and IN_B_INST leave through vias (port copper); the taps carry the INSTRUMENT class, the two tap stubs are 0.15 mm.

4. Schmitt buffer and supply bypass

U1101A gates A (1A to 1Y) and B (2A to 2Y) square the filtered inputs into 3.3 V logic; C1103 (100 nF) bypasses VCC (pin 5) to GND (pin 2).



Unit 1: Schmitt-trigger buffer
C1101: Input low-pass capacitor, 72 kHz with 4.7 k
R1105: Output pull-down, unpowered state



Power unit
C1103: VCC bypass for U1101A

PLACE: U1101A in the middle of the block between the input and output edges. C1103 hard against pin 5 with a short return to pin 2; +3.3V and GND reach the block through vias.

ROUTE: +3.3V carries PWR_3V3_LOCAL; the block's baseline is 0.2 mm tracks and 0.6/0.3 mm vias.

INTERFACES

+3.3V

Buffer supply (VCC, pin 5). 1.65 to 5.5 V; always-on when the taps must be observable before firmware runs, switched when the consumer of IN_A/IN_B powers down with it (loff keeps the unpowered outputs off the bus).

GND

Return for the buffer (pin 2), both filter capacitors and the four pull-downs.

IN_A_RAW

Field-wired channel A input. 0 to 5.5 V legal at any VCC; pulled low by R1101 (100 k) when unplugged.

IN_B_RAW

Field-wired channel B input. 0 to 5.5 V legal at any VCC; pulled low by R1102 (100 k) when unplugged.

IN_A_Q

Conditioned channel A. 3.3 V logic from 1Y (pin 6); pulled down by R1105 when the rail is off.

IN_B_Q

Conditioned channel B. 3.3 V logic from 2Y (pin 4); pulled down by R1106 when the rail is off.

IN_A_INST_Q

Instrument tap of IN_A through R1107 (100 ohm), INSTRUMENT class.

IN_B_INST_Q

Instrument tap of IN_B through R1108 (100 ohm), INSTRUMENT class.

OPERATION

Signal path, per channel: IN_A_RAW -> R1103 (4.7 k) -> IN_A_FILT (C1101 470 pF to GND) -> U1101A 1A (pin 1) -> 1Y (pin 6) -> IN_A, tapped through R1107 (100 ohm) to IN_A_INST; channel B is R1104, C1102, 2A (pin 3), 2Y (pin 4), IN_B and R1108 to IN_B_INST. R1101/R1102 (100 k) pull the raw inputs low when unplugged, on the harness side of the series resistor so no divider eats VIH margin; R1105/R1106 (100 k) define the outputs when +3.3V is off.

Filter: 4.7 k and 470 pF give a time constant of about 2.2 us and a corner near 72 kHz; a 3.3 V edge reaches the worst-case VT+ of 2.0 V about 2 us later, the same on both channels, so relative timing is kept. For faster edges swap C1101/C1102 (27 pF gives about 1.25 MHz).

The Schmitt input is the point: at VCC = 3 V, VT+ is 1.3 to 2.0 V and VT- 0.8 to 1.3 V with at least 0.4 V of hysteresis, so slow or noisy field edges cannot double-trigger; a 3.3 V source clears VT+ by at least 1.3 V, a 5 V TTL VDH of 2.4 V by 0.4 V. Inputs are rated 0 to 5.5 V at any VCC (6.5 V absolute), so a 5 V source is legal; a source below ground draws about 0.2 mA per volt through the 4.7 k (about 1 mA from -5 V), and a short to a 36 V is bounded to about 7 mA into the buffer.

Supply: VCC 1.65 to 5.5 V, 10 uA max, +/-24 mA drive at 3 V; loff (10 uA max) keeps the outputs off a live downstream input when the rail is down, which is why the sequencing between source and buffer does not matter. C1103 (100 nF) bypasses pin 5.

DESIGN CONTRACT

Two-channel single-ended logic input conditioner; per-channel series/RC filtering plus an SN74LVC2G17 dual Schmitt-trigger buffer that turns a 3.3 V or 5 V field-wired logic signal into clean 3.3 V logic, with a 100 ohm InstrumentPort tap on each output. Generic sibling of quadrature_encoder_input_5v_sn74lvc2g17; same circuit and values, generic names, no encoder-supply passthrough. Use this one for BNC trigger and sync inputs, sensor and switch logic lines and any other pair of inputs a board conditions; use the encoder block when the harness also carries the encoder supply; place this block twice for four inputs. Connector-agnostic: the jack or terminal lives on the board sheet. Bring the raw lines in on IN_A_RAW and IN_B_RAW, take conditioned 3.3 V logic out on IN_A and IN_B and the taps out on IN_A_INST and IN_B_INST; rails +3.3V and GND. Per channel: R1103/R1104 4.7 kohm series (OW-RES-4K7-0402, C25900) into C1101/C1102 470 pF COG to ground (OW-CAP-470P-0402-COG-100V, C1518202) and U1101A SN74LVC2G17DRYR gate A/B (OW-MISC-SN74LVC2G17DRYR, C2675856); R1101/R1102 100 kohm pull-down (OW-PASS-RC0402JR-07100KL, C106234) on the harness side of the series resistor, so an unplugged input reads low without forming a divider that eats VIH margin; R1105/R1106 100 kohm pull-down on each output for loff high-Z, so an always-on downstream buffer never sees a floating input when this rail is down; R1107/R1108 100 ohm T-taps (OW-PASS-0402WGF1000TCE, C25076) to the _INST ports, INSTRUMENT netclass from the instrument-taps profile; C1103 100 nF (OW-CAP-100N-0402-X5R-16V, C162178) hard against U1101C pin 5.

The Schmitt input is the point of the block: an ordinary LVC buffer specifies a maximum input transition rate of about 8 ns/V, which a slow or noisy field edge violates and double-triggers; the 2G17 has no such limit and 0.4 V minimum hysteresis at 3 V. Thresholds VT+ <= 2.0 V and VT- >= 0.8 V, so a 3.3 V microcontroller pin clears the high threshold by 0.9 V or more and a 5 V TTL-level VDH of 2.4 V by 0.4 V.

Tolerance: inputs are rated 0 to 5.5 V at any valid VCC, 6.5 V absolute maximum, with no clamp diode to VCC, so a 5 V source plugged in by mistake is legal; a source held below ground draws about 0.2 mA per volt through the 4.7 kohm (a -5 V DAC output about 1 mA), and a short to a 36 V rail is bounded to about 7 mA and destroys a 0.19 USD buffer instead of the consumer.

Filter: 4.7 kohm and 470 pF give a 72 kHz corner and about 2 us from a 3.3 V edge to the Schmitt threshold, the same on both channels so their relative timing is preserved: 470 pF suits sub-10 kHz timing edges on long unshielded leads, swap C1101/C1102 for a faster corner when the signal needs it (27 pF gives 1.25 MHz).

Rails are generic labels: bind +3.3V to the always-on rail when the taps must be observable before firmware runs, or to the switched domain when the consumer of IN_A/IN_B can be powered down and must rise and fall with it; sequencing between source and buffer is a non-issue because loff disables the outputs when the part is unpowered.

First consumer: camera-gpio-interface-pcb, TRIG_IN and SYNC_IN BNCs from a pyControl breakout on IN_A_RAW/IN_B_RAW, TRIG_IN/SYNC_IN out, taps on DIG0/DIG1 of the digital-50 InstrumentPort.

Series resistors and filter capacitors on the input edge, the 2G17 and its decoupling in the middle, output pull-downs and taps on the output edge, so harness-side nets stay on one edge and logic and tap nets leave on the other. Keep the input pair away from motor bridge outputs and give it a ground reference.

Project-local pending bench verification; promotable once a second board uses it.

Circuit and PCB layout guidance
Migrated from the saved library sheet; circuit and PCB unchanged

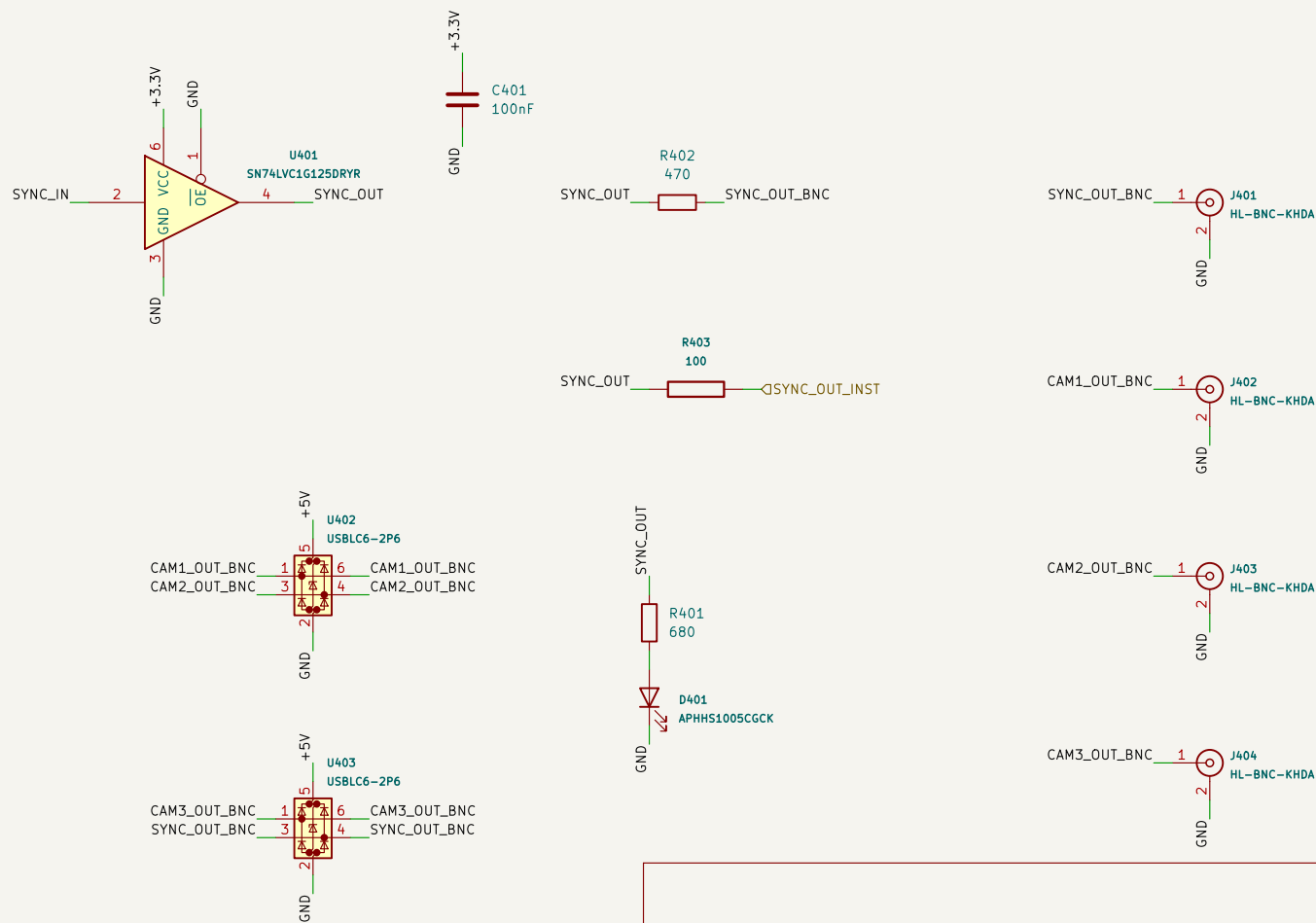
Orb Weaver

Sheet: /inputs/logic_input_2ch_5v_schmitt_sn74lvc2g17/
File: logic_input_2ch_5v_schmitt_sn74lvc2g17.kicad_sch

Title: Two-channel Schmitt logic input

Size: A2 Date: 2026-10-04 Rev: Source migration 1
KiCad E.D.A. 10.0.6 Id: 11/11

+5V □ +5V
+3.3V □ +3.3V
GND □ GND
SYNC_IN □ SYNC_IN
CAM1_OUT_BNC □ CAM1_OUT_BNC
CAM2_OUT_BNC □ CAM2_OUT_BNC
CAM3_OUT_BNC □ CAM3_OUT_BNC



Janelia Research Campus

Sheet: /outputs/

File: outputs.kicad_sch

Title: camera-gpio-interface-pcb

Size: A4

Date: 2026-09-26

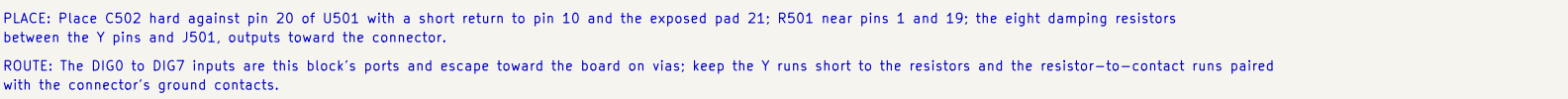
Rev: 1.0

KiCad E.D.A. 10.0.6

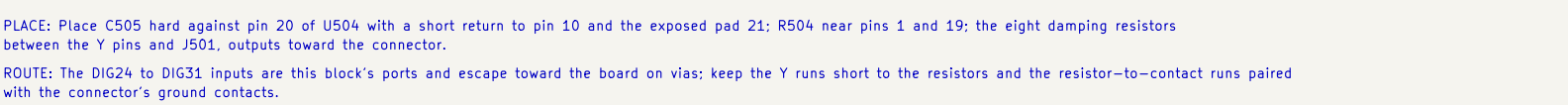
Id: 4/11

OUT-side InstrumentPort-Digital=50 with integrated read-only buffering, on a VERTICAL, top-entry 50-Contact ZIF connector: Hirose FH12-50S=0.55VA(54), OW-CONN-FH12-50S=0-55VA-54, LCSC C597991, 0.5mm pitch, symbol Conn_01x50, footprint orb_weaver_connectors:Hirose_FH12-50S=0.55VA_1x50=4MP_P0.5mm_Vertical; the four mechanical lands are unnumbered pads and carry no net. Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

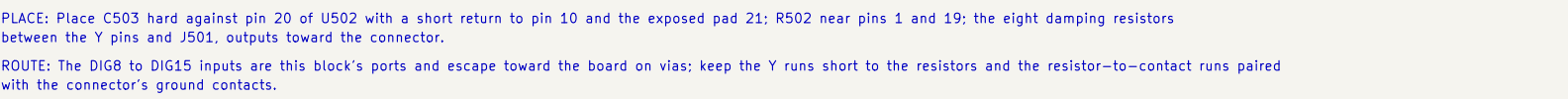
U501 buffers DIG0 to DIG7 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18); R505 to R512 (100 ohm) damp each output into its connector contact
C502 bypasses VCC (pin 20); R501 holds both enables (pins 1 and 19) low.



U504 buffers DIG24 to DIG31 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18); R529 to R536 (100 ohm) damp each output into its connector contact C505 bypasses VCC (pin 20); R504 holds both enables (pins 1 and 19) low.

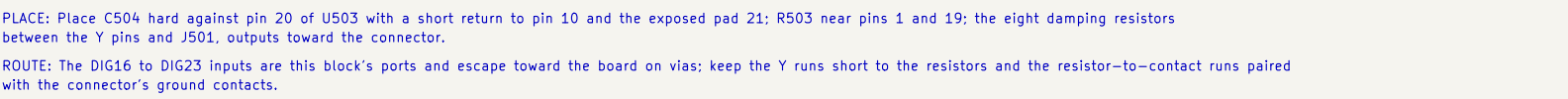
[illegible][illegible]

U502 buffers DIG8 to DIG15 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18); R513 to R520 (100 ohm) damp each output into its connector contact; C503 bypasses VCC (pin 20); R502 holds both enables (pins 1 and 19) low.

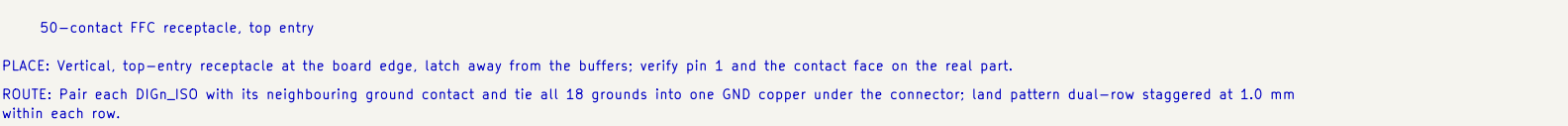


C501 (4.7 uF) holds the +3.3V rail where it enters the block; the per-package 100 nF bypasses are in the octet groups

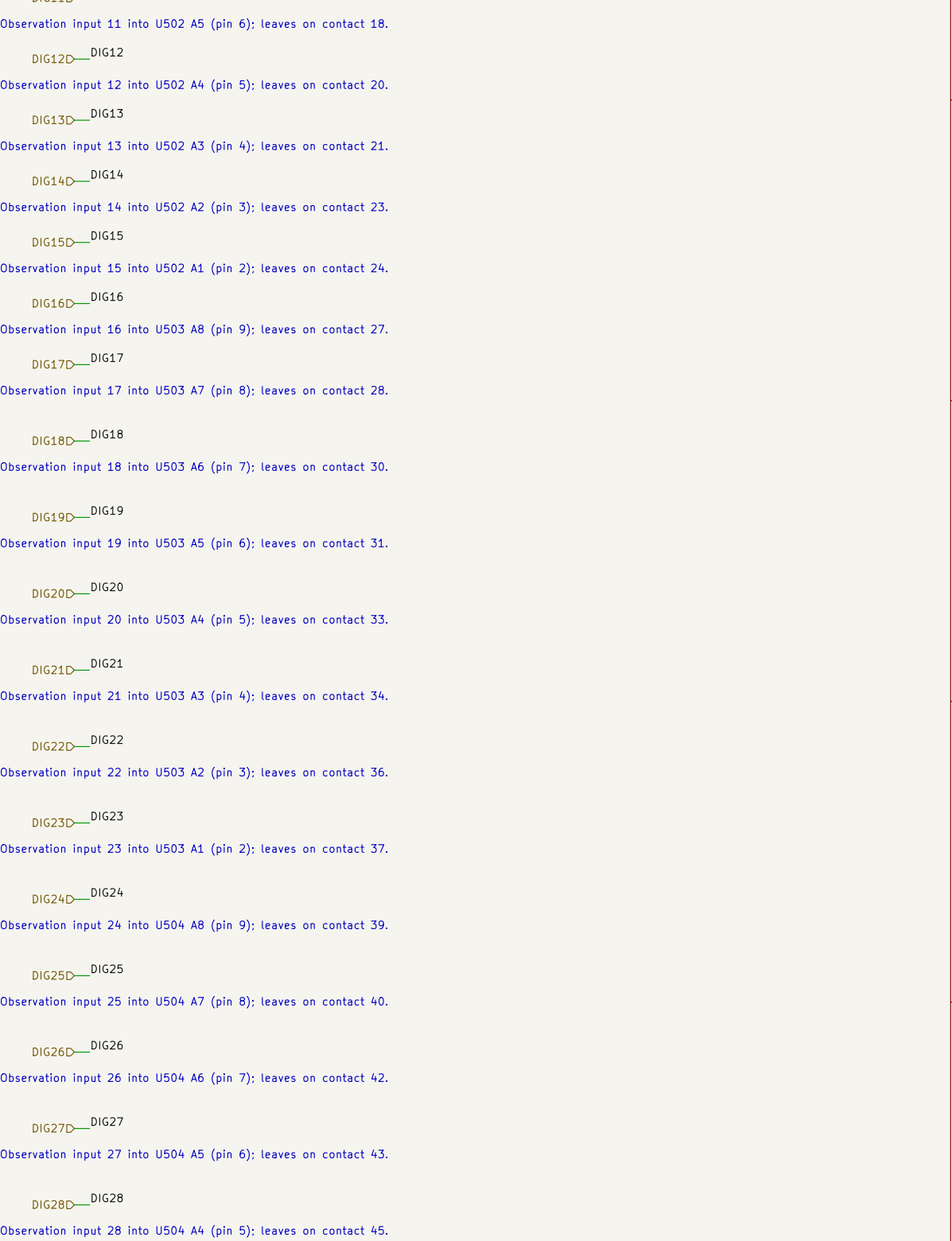
U503 buffers DIG16 to DIG23 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18); R521 to R528 (100 ohm) damp each output into its connector contact; C504 bypasses VCC (pin 20); R503 holds both enables (pins 1 and 19) low.



J501 carries the 32 damped outputs (DIGN_50) on the contract's DUT contacts and the 18 grounds on one GND; the four mechanical lands carry no net



Always-on 3.3 V buffer supply (VCC pins 20): never reaches the cable.



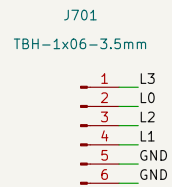
Blackfly S GPIO channel | trigger in, sync in, exposure out, five taps; vertical or horizontal header

One FLIR Blackfly S camera GPIO channel (trigger, sync, exposure output, instrument taps) on a 6-position 3.5 mm Phoenix header; the connector family pilot: the vertical MCV and the horizontal MC header are pad-identical, so one source publishes both orientations

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Camera header

J701, the 6-position 3.5 mm Phoenix header; pins 1 to 4 are Lines 3, 0, 2 and 1, pins 5 and 6 are the camera's two grounds.



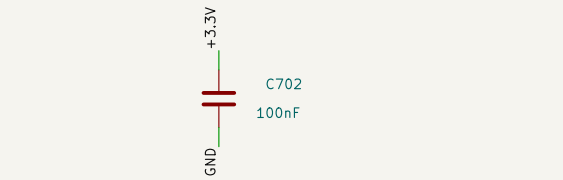
Camera GPIO header, 6-pos
3.5 mm

PLACE: Place J701 at the board edge the plug needs: the vertical body takes the plug from above, the horizontal from its +Y side; the anchor is the pad-array centre for both.

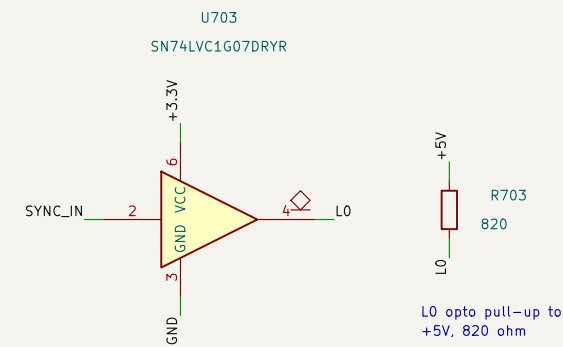
ROUTE: L3, L0, L2 and L1 run straight from the pads to their clamps and parts; GND from pins 5 and 6 into the block's return.

3. Line 0 sync drive

U703's open-drain Y pulls L0 low; R703 (820 ohm) returns it to +5V, the opto input's drive level; C702 bypasses U703's VCC.



VCC pin 6 bypass, U703



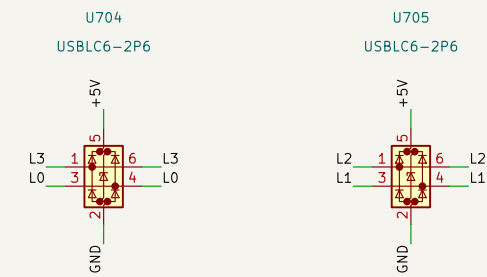
Line 0 sync driver, open drain

PLACE: Place U703 near J701 pin 2 with C702 at its pin 6; R703 from L0 to the +5V entry.

ROUTE: L0 carries about 6 mA pulses into the camera's opto input; keep its return with the trigger line.

5. ESD clamps

U704 clamps L3 and L0, U705 clamps L2 and L1, both referenced to +5V and GND; each pair's two I/O pins are tied to the node.



ESD array for L3/L0

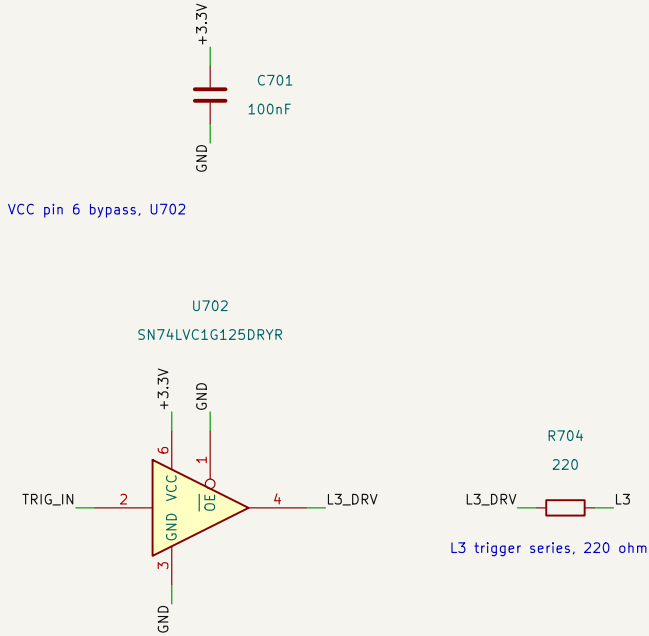
ESD array for L2/L1

PLACE: Place both arrays right at J701's pads, before any series part, with the shortest GND return.

ROUTE: Wire the paired I/O pads together on the node itself; no separate track between them.

2. Line 3 trigger drive

U702 (always enabled) drives L3_DRV; R704 (220 ohm) in series feeds camera Line 3 on L3; C701 bypasses U702's VCC.



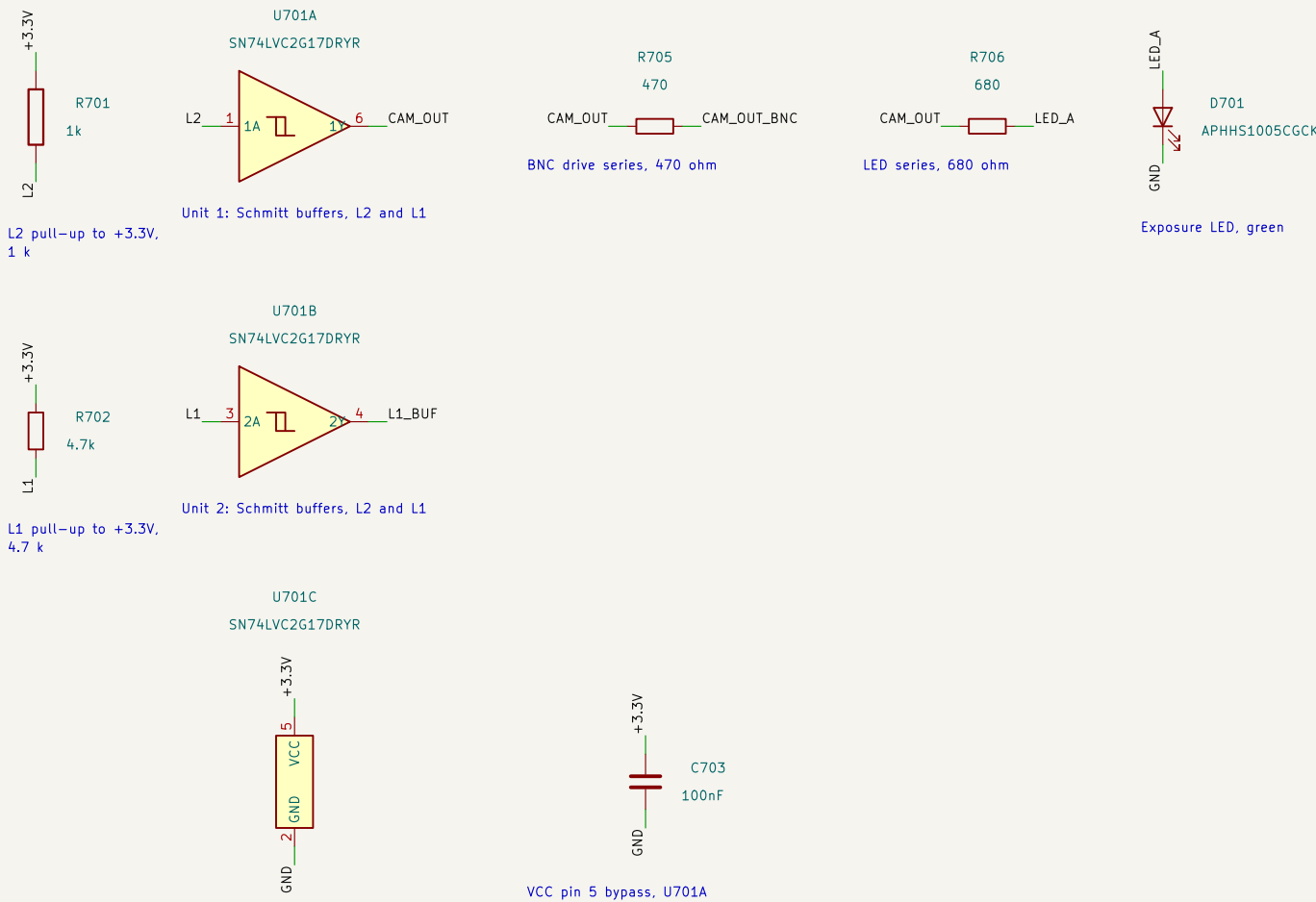
Line 3 trigger driver, always enabled

PLACE: Place U702 near J701 pin 1 with C701 at its pin 6 and a short return to pin 3; R704 between the driver and the connector.

ROUTE: L3 is a 3.3 V edge-triggered line; short, over ground, away from the switching parts of the board.

4. Exposure output, BNC drive and LED

R701 pulls Line 2 up, U701A gate 1 squares it into CAM_OUT; R705 drives the BNC, R706 lights D701; R702 pulls Line 1 up and gate 2 buffers it into L1_BUF; C703 bypasses U701A.



Power unit

PLACE: Place U701A between the connector and the BNC side with C703 at its pin 5; R701 and R702 at the connector pads; D701 where it is visible.

ROUTE: CAM_OUT is the board's exposure reference; route R705's far end to the BNC with a ground return beside it.

INTERFACES

+5V — +5V
Must be a 5 V rail; the Line 0 opto drive level (R703) and both ESD clamps' VBUS reference.

+3.3V — +3.3V
Logic rail for U701A, U702, U703 and the L2/L1 pull-ups; always-on if the taps must read before firmware.

GND — GND
Camera pins 5 (opto ground) and 6 (ground) both land here, with the logic and ESD returns.

TRIG_IN — TRIG_IN
Conditioned 3.3 V frame trigger from the board's input Schmitt into U702 (pin 2).

SYNC_IN — SYNC_IN
Conditioned 3.3 V Rsync from the board's input Schmitt into U703 (pin 2).

CAM_OUT_BNC — CAM_OUT_BNC
Exposure-active output; CAM_OUT through R705 (470 ohm); the BNC itself is the board's.

L0_INST — L0_INST
100 ohm tap (R707) on L0, camera Line 0 OPTOIN; the sync drive.

L1_INST — L1_INST
100 ohm tap (R708) on L1_BUF, camera Line 1 OPTOOUT after the Schmitt buffer.

L2_INST — L2_INST
100 ohm tap (R709) on L2, camera Line 2, the open-drain exposure output.

L3_INST — L3_INST
100 ohm tap (R710) on L3, camera Line 3, the frame trigger.

OUT_INST — OUT_INST
100 ohm tap (R711) on CAM_OUT, the buffered exposure signal.

INTERNAL NETS

CAM_OUT: Buffered Line 2 (exposure active) from U701A 1Y; drives the BNC resistor, the LED resistor and the OUT tap.

L0: Camera pin 2, Line 0 OPTOIN; open-drain U703 Y, pulled to +5V by R703 (820 ohm), clamped by U704.

L1: Camera pin 4, Line 1 OPTOOUT, pulled up to +3.3V by R702 (4.7 k), into Schmitt 2A, clamped by U705.

L1_BUF: Schmitt 2Y; buffered Line 1 for the L1_INST tap.

L2: Camera pin 3, Line 2 as open-drain exposure output, pulled up by R701 (1 k), into Schmitt 1A, clamped by U705.

L3: Camera pin 1, Line 3 GPI trigger, driven by U702 through R704 (220 ohm), clamped by U704.

L3_DRV: U702 Y, the trigger drive before the 220 ohm series resistor.

LED_A: LED anode; R706 (680 ohm) from CAM_OUT, so D701 lights while exposure is active.

OPERATION

Camera side: J701's terminal numbers are the camera's Hirose HR10A-7R-6PB pin numbers, wired with the FLIR 1 m flying-lead GPIO cable into a Phoenix MC 1.5/6-ST-3.5 plug; pin 1 green Line 3 (GPI, trigger), pin 2 black Line 0 (OPTOIN, sync), pin 3 red Line 2 (GPIO, exposure output), pin 4 white Line 1 (OPTOOUT), pin 5 blue opto ground and pin 6 brown ground, both on GND (common-ground wiring).

Trigger path: TRIG_IN -> U702 (SN74LVC1G125, OE pin 1 grounded, so always enabled) -> L3_DRV -> R704 (220 ohm) -> L3 -> camera Line 3; camera settings TriggerSelector FrameStart, TriggerSource Line3 RisingEdge. Sync path: SYNC_IN -> U703 (SN74LVC1G07 open drain) -> L0, pulled to +5V by R703 (820 ohm); 5 V across 820 ohm is about 6 mA, less by the opto input's forward drop. Both drivers run from +3.3V with 5.5 V-tolerant I/O.

Exposure output: camera Line 2 (LineMode Output, LineSource ExposureActive, V3.3Enable false, so open drain) is pulled up by R701 (1 k) to +3.3V and squared by Schmitt U701A 1A -> 1Y = CAM_OUT, which drives the BNC through R705 (470 ohm), the green LED D701 through R706 (680 ohm; about (3.3 - 2.1) / 680 = 1.8 mA, LED on while exposure is active) and the OUT_INST tap. Line 1 (OPTOOUT, LineSource Off) is pulled up by R702 (4.7 k) and buffered 2A -> 2Y into L1_BUF for its tap.

ESD: two USBLC6-2P6 arrays with VBUS on +5V clamp L3 and L0 (U704) and L2 and L1 (U705), 15 kV IEC 61000-4-2 level 4, at most 3.5 pF per line; both I/O pins of each pair are wired to the node, so the footprint's paired pads need no track between them. +5V must therefore be a 5 V rail: it is the clamp reference and the opto drive level, and feeds nothing else.

Variants (family.json): mcv6_vertical fits J701 = OW-CONN-TBH-1X06-3P5-VERT (Phoenix MCV 1.5/6-G-3.5, top entry); mcv6_horizontal fits OW-CONN-1844252 (Phoenix MC 1.5/6-G-3.5, side entry toward the footprint's +Y). The two footprints are pad-identical (six 1.8 x 3.6 mm ovals on 3.5 mm, origin at the pad-array centre), so the variant swaps only the connector's body, courtyard and 3D model; every pad, track and via stays, and the anchor connector_center is the same point for both.

The placing board provides +3.3V (bind it to the always-on rail when the taps must be observable before firmware runs), a 5 V rail on +5V, the BNC on CAM_OUT_BNC, the conditioned 3.3 V TRIG_IN and SYNC_IN, and the instrument port behind the five 100 ohm taps; the three pull-ups are inside because the block owns L0, L1 and L2 (layout convention 10). Place one block per camera; the horizontal variant's plug needs the board edge its wire exit faces.

DESIGN CONTRACT

One FLIR Blackfly S camera GPIO channel (trigger, sync, exposure output, instrument taps) on a 6-position 3.5 mm Phoenix header; the connector family pilot: the vertical MCV and the horizontal MC header are pad-identical, so one source publishes both orientations

Circuit and PCB layout guidance
Migrated from the saved family core; circuit, variants and PCB unchanged

Orb Weaver

Sheet: /blackfly_s_gpio_channel_mcv6_vertical/
File: blackfly_s_gpio_channel_mcv6_vertical.kicad_sch

Title: **Blackfly S GPIO channel family**

Size: A2

Date: 2026-10-04

Rev: Source migration 1

KiCad E.D.A. 10.0.6

Id: 7/11

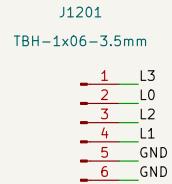
Blackfly S GPIO channel | trigger in, sync in, exposure out, five taps; vertical or horizontal header

One FLIR Blackfly S camera GPIO channel (trigger, sync, exposure output, instrument taps) on a 6-position 3.5 mm Phoenix header; the connector family pilot: the vertical MCV and the horizontal MC header are pad-identical, so one source publishes both orientations

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Camera header

J701, the 6-position 3.5 mm Phoenix header; pins 1 to 4 are Lines 3, 0, 2 and 1, pins 5 and 6 are the camera's two grounds.

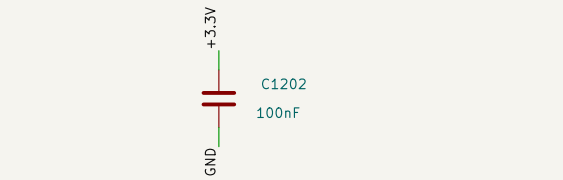


Camera GPIO header, 6-pos
3.5 mm

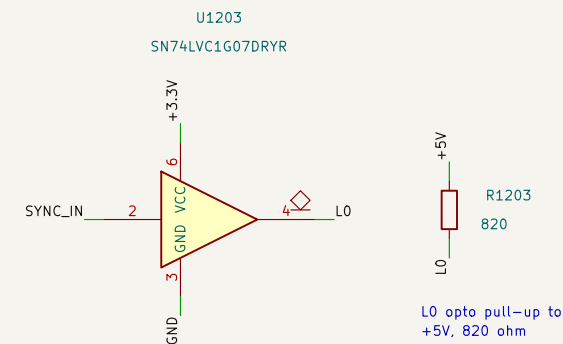
PLACE: Place J701 at the board edge the plug needs: the vertical body takes the plug from above, the horizontal from its +Y side; the anchor is the pad-array centre for both.
ROUTE: L3, L0, L2 and L1 run straight from the pads to their clamps and parts; GND from pins 5 and 6 into the block's return.

3. Line 0 sync drive

U703's open-drain Y pulls L0 low; R703 (820 ohm) returns it to +5V, the opto input's drive level; C702 bypasses U703's VCC.



VCC pin 6 bypass, U703

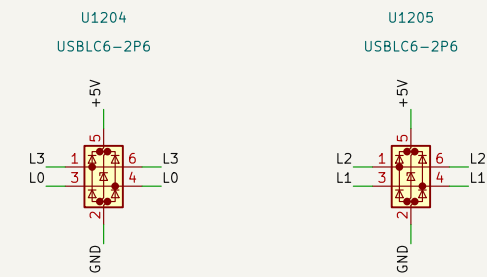


Line 0 sync driver, open drain

PLACE: Place U703 near J701 pin 2 with C702 at its pin 6; R703 from L0 to the +5V entry.
ROUTE: L0 carries about 6 mA pulses into the camera's opto input; keep its return with the trigger line.

5. ESD clamps

U704 clamps L3 and L0, U705 clamps L2 and L1, both referenced to +5V and GND; each pair's two I/O pins are tied to the node.



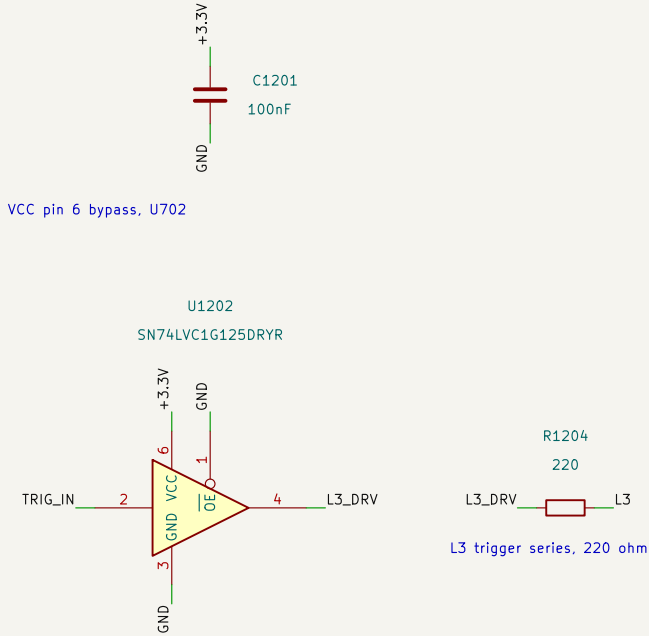
ESD array for L3/L0

ESD array for L2/L1

PLACE: Place both arrays right at J701's pads, before any series part, with the shortest GND return.
ROUTE: Wire the paired I/O pads together on the node itself; no separate track between them.

2. Line 3 trigger drive

U702 (always enabled) drives L3_DRV; R704 (220 ohm) in series feeds camera Line 3 on L3; C701 bypasses U702's VCC.

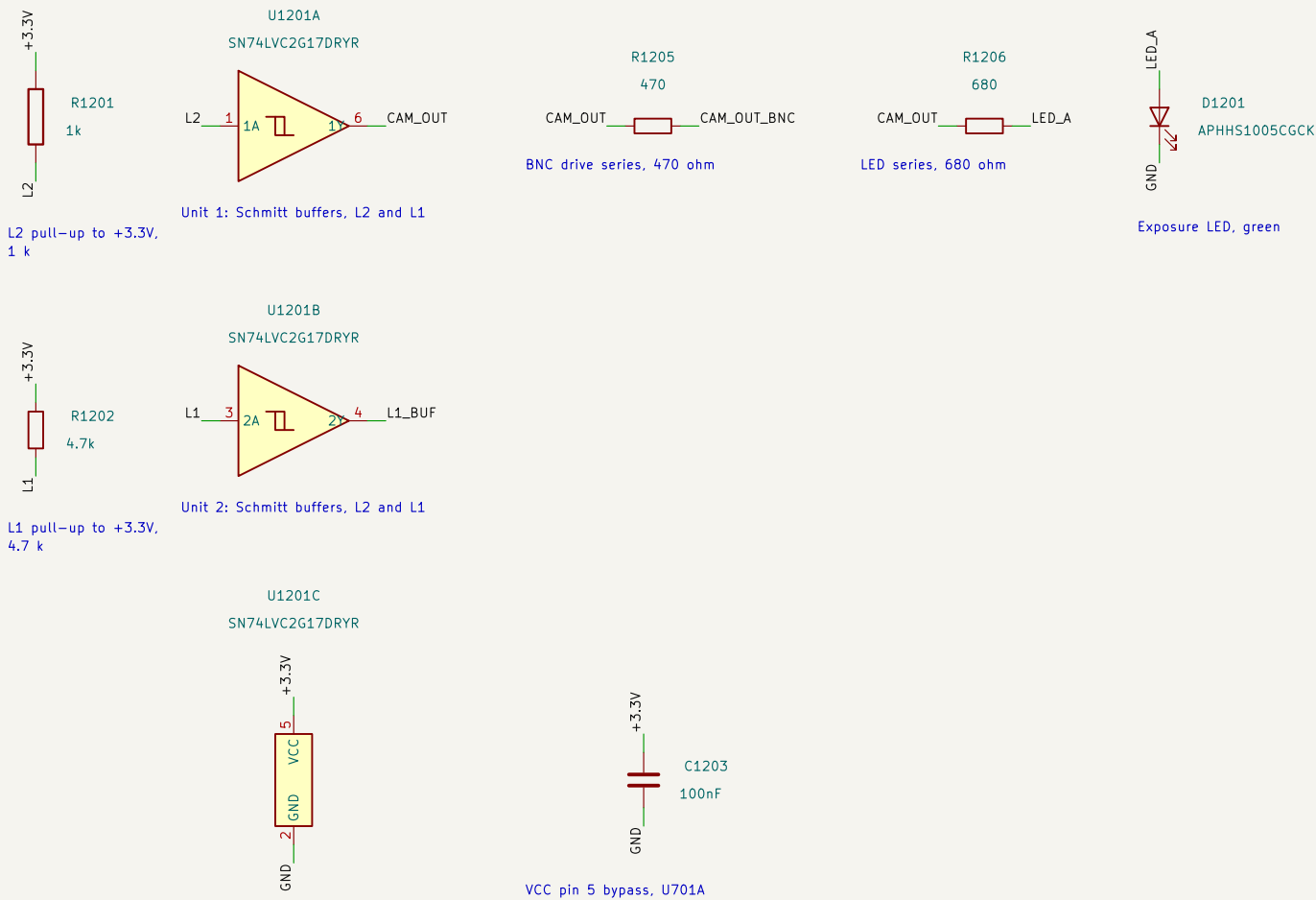


Line 3 trigger driver, always enabled

PLACE: Place U702 near J701 pin 1 with C701 at its pin 6 and a short return to pin 3; R704 between the driver and the connector.
ROUTE: L3 is a 3.3 V edge-triggered line; short, over ground, away from the switching parts of the board.

4. Exposure output, BNC drive and LED

R701 pulls Line 2 up, U701A gate 1 squares it into CAM_OUT; R705 drives the BNC, R706 lights D701; R702 pulls Line 1 up and gate 2 buffers it into L1_BUF; C703 bypasses U701A.



PLACE: Place U701A between the connector and the BNC side with C703 at its pin 5; R701 and R702 at the connector pads; D701 where it is visible.
ROUTE: CAM_OUT is the board's exposure reference; route R705's far end to the BNC with a ground return beside it.

INTERFACES

+5V — +5V
Must be a 5 V rail; the Line 0 opto drive level (R703) and both ESD clamps' VBUS reference.

+3.3V — +3.3V
Logic rail for U701A, U702, U703 and the L2/L1 pull-ups; always-on if the taps must read before firmware.

GND — GND
Camera pins 5 (opto ground) and 6 (ground) both land here, with the logic and ESD returns.

TRIG_IN — TRIG_IN
Conditioned 3.3 V frame trigger from the board's input Schmitt into U702 (pin 2).

SYNC_IN — SYNC_IN
Conditioned 3.3 V Rsync from the board's input Schmitt into U703 (pin 2).

CAM_OUT_BNC — CAM_OUT_BNC
Exposure-active output; CAM_OUT through R705 (470 ohm); the BNC itself is the board's.

L0_INST — L0_INST
100 ohm tap (R707) on L0, camera Line 0 OPTOIN; the sync drive.

L1_INST — L1_INST
100 ohm tap (R708) on L1_BUF, camera Line 1 OPTOOUT after the Schmitt buffer.

L2_INST — L2_INST
100 ohm tap (R709) on L2, camera Line 2, the open-drain exposure output.

L3_INST — L3_INST
100 ohm tap (R710) on L3, camera Line 3, the frame trigger.

OUT_INST — OUT_INST
100 ohm tap (R711) on CAM_OUT, the buffered exposure signal.

INTERNAL NETS

CAM_OUT: Buffered Line 2 (exposure active) from U701A 1Y; drives the BNC resistor, the LED resistor and the OUT tap.

L0: Camera pin 2, Line 0 OPTOIN; open-drain U703 Y, pulled to +5V by R703 (820 ohm), clamped by U704.

L1: Camera pin 4, Line 1 OPTOOUT, pulled up to +3.3V by R702 (4.7 k), into Schmitt 2A, clamped by U705.

L1_BUF: Schmitt 2Y; buffered Line 1 for the L1_INST tap.

L2: Camera pin 3, Line 2 as open-drain exposure output, pulled up by R701 (1 k), into Schmitt 1A, clamped by U705.

L3: Camera pin 1, Line 3 GPI trigger, driven by U702 through R704 (220 ohm), clamped by U704.

L3_DRV: U702 Y, the trigger drive before the 220 ohm series resistor.

LED_A: LED anode; R706 (680 ohm) from CAM_OUT, so D701 lights while exposure is active.

OPERATION

Camera side: J701's terminal numbers are the camera's Hirose HR10A-7R-6PB pin numbers, wired with the FLIR 1 m flying-lead GPIO cable into a Phoenix MC 1.5/6-ST-3.5 plug; pin 1 green Line 3 (GPI, trigger), pin 2 black Line 0 (OPTOIN, sync), pin 3 red Line 2 (GPIO, exposure output), pin 4 white Line 1 (OPTOOUT), pin 5 blue opto ground and pin 6 brown ground, both on GND (common-ground wiring).

Trigger path: TRIG_IN -> U702 (SN74LVC1G125, OE pin 1 grounded, so always enabled) -> L3_DRV -> R704 (220 ohm) -> L3 -> camera Line 3; camera settings TriggerSelector FrameStart, TriggerSource Line3 RisingEdge. Sync path: SYNC_IN -> U703 (SN74LVC1G07 open drain) -> L0, pulled to +5V by R703 (820 ohm); 5 V across 820 ohm is about 6 mA, less by the opto input's forward drop. Both drivers run from +3.3V with 5.5 V-tolerant I/O.

Exposure output: camera Line 2 (LineMode Output, LineSource ExposureActive, V3.3Enable false, so open drain) is pulled up by R701 (1 k) to +3.3V and squared by Schmitt U701A 1A -> 1Y = CAM_OUT, which drives the BNC through R705 (470 ohm), the green LED D701 through R706 (680 ohm; about (3.3 - 2.1) / 680 = 1.8 mA, LED on while exposure is active) and the OUT_INST tap. Line 1 (OPTOOUT, LineSource Off) is pulled up by R702 (4.7 k) and buffered 2A -> 2Y into L1_BUF for its tap.

ESD: two USBLC6-2P6 arrays with VBUS on +5V clamp L3 and L0 (U704) and L2 and L1 (U705), 15 kV IEC 61000-4-2 level 4, at most 3.5 pF per line; both I/O pins of each pair are wired to the node, so the footprint's paired pads need no track between them. +5V must therefore be a 5 V rail: it is the clamp reference and the opto drive level, and feeds nothing else.

Variants (family.json): mcv6_vertical fits J701 = OW-CONN-TBH-1X06-3P5-VERT (Phoenix MCV 1.5/6-G-3.5, top entry); mc6_horizontal fits OW-CONN-1844252 (Phoenix MC 1.5/6-G-3.5, side entry toward the footprint's +Y). The two footprints are pad-identical (six 1.8 x 3.6 mm ovals on 3.5 mm, origin at the pad-array centre), so the variant swaps only the connector's body, courtyard and 3D model; every pad, track and via stays, and the anchor connector_center is the same point for both.

The placing board provides +3.3V (bind it to the always-on rail when the taps must be observable before firmware runs), a 5 V rail on +5V, the BNC on CAM_OUT_BNC, the conditioned 3.3 V TRIG_IN and SYNC_IN, and the instrument port behind the five 100 ohm taps; the three pull-ups are inside because the block owns L0, L1 and L2 (layout convention 10). Place one block per camera; the horizontal variant's plug needs the board edge its wire exit faces.

DESIGN CONTRACT

One FLIR Blackfly S camera GPIO channel (trigger, sync, exposure output, instrument taps) on a 6-position 3.5 mm Phoenix header; the connector family pilot: the vertical MCV and the horizontal MC header are pad-identical, so one source publishes both orientations

Circuit and PCB layout guidance
Migrated from the saved family core; circuit, variants and PCB unchanged

Orb Weaver

Sheet: /blackfly_s_gpio_channel_mcv6_vertical1/
File: blackfly_s_gpio_channel_mcv6_vertical.kicad_sch

Title: **Blackfly S GPIO channel family**

Size: A2 Date: 2026-10-04 Rev: Source migration 1

KiCad E.D.A. 10.0.6 Id: 12/11

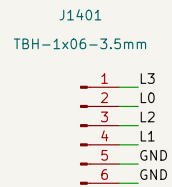
Blackfly S GPIO channel | trigger in, sync in, exposure out, five taps; vertical or horizontal header

One FLIR Blackfly S camera GPIO channel (trigger, sync, exposure output, instrument taps) on a 6-position 3.5 mm Phoenix header; the connector family pilot: the vertical MCV and the horizontal MC header are pad-identical, so one source publishes both orientations

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Camera header

J701, the 6-position 3.5 mm Phoenix header; pins 1 to 4 are Lines 3, 0, 2 and 1, pins 5 and 6 are the camera's two grounds.



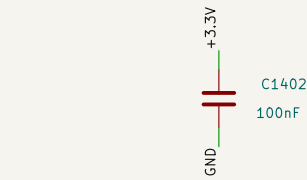
Camera GPIO header, 6-pos
3.5 mm

PLACE: Place J701 at the board edge the plug needs; the vertical body takes the plug from above, the horizontal from its +Y side; the anchor is the pad-array centre for both.

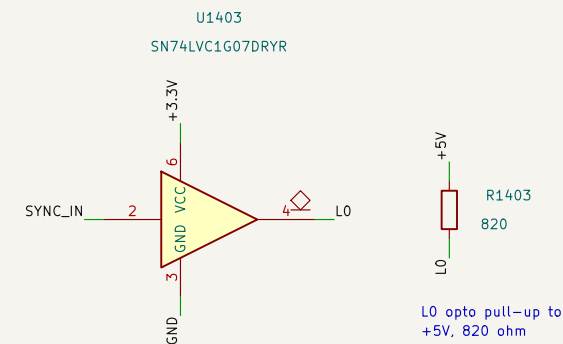
ROUTE: L3, L0, L2 and L1 run straight from the pads to their clamps and parts; GND from pins 5 and 6 into the block's return.

3. Line 0 sync drive

U703's open-drain Y pulls L0 low; R703 (820 ohm) returns it to +5V, the opto input's drive level; C702 bypasses U703's VCC.



VCC pin 6 bypass, U703



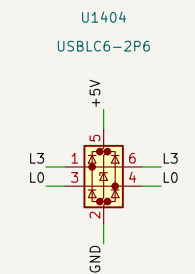
Line 0 sync driver, open drain

PLACE: Place U703 near J701 pin 2 with C702 at its pin 6; R703 from L0 to the +5V entry.

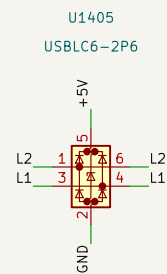
ROUTE: L0 carries about 6 mA pulses into the camera's opto input; keep its return with the trigger line.

5. ESD clamps

U704 clamps L3 and L0, U705 clamps L2 and L1, both referenced to +5V and GND; each pair's two I/O pins are tied to the node.



ESD array for L3/L0



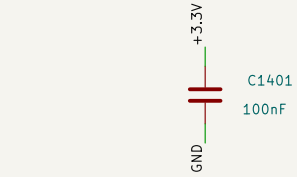
ESD array for L2/L1

PLACE: Place both arrays right at J701's pads, before any series part, with the shortest GND return.

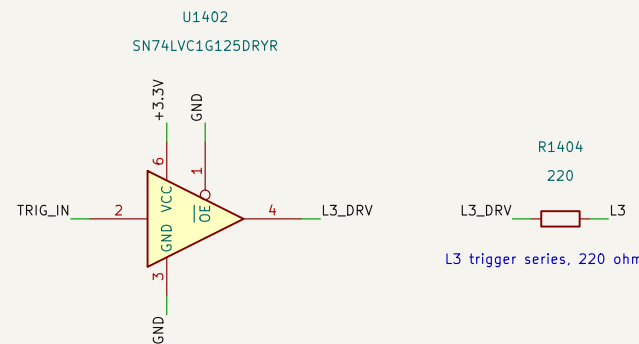
ROUTE: Wire the paired I/O pads together on the node itself; no separate track between them.

2. Line 3 trigger drive

U702 (always enabled) drives L3_DRV; R704 (220 ohm) in series feeds camera Line 3 on L3; C701 bypasses U702's VCC.



VCC pin 6 bypass, U702



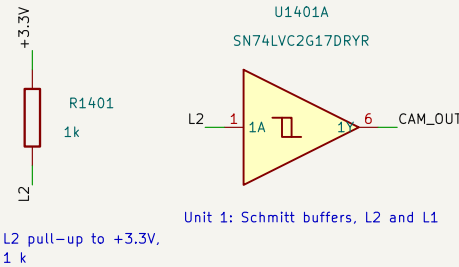
Line 3 trigger driver, always enabled

PLACE: Place U702 near J701 pin 1 with C701 at its pin 6 and a short return to pin 3; R704 between the driver and the connector.

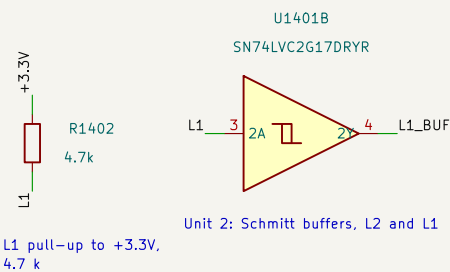
ROUTE: L3 is a 3.3 V edge-triggered line; short, over ground, away from the switching parts of the board.

4. Exposure output, BNC drive and LED

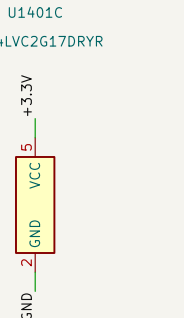
R701 pulls Line 2 up, U701A gate 1 squares it into CAM_OUT; R705 drives the BNC, R706 lights D701; R702 pulls Line 1 up and gate 2 buffers it into L1_BUF; C703 bypasses U701A.



Unit 1: Schmitt buffers, L2 and L1



Unit 2: Schmitt buffers, L2 and L1



Power unit

PLACE: Place U701A between the connector and the BNC side with C703 at its pin 5; R701 and R702 at the connector pads; D701 where it is visible.

ROUTE: CAM_OUT is the board's exposure reference; route R705's far end to the BNC with a ground return beside it.

INTERFACES

+5V

Must be a 5 V rail; the Line 0 opto drive level (R703) and both ESD clamps' VBUS reference.

+3.3V

Logic rail for U701A, U702, U703 and the L2/L1 pull-ups; always-on if the taps must read before firmware.

GND

Camera pins 5 (opto ground) and 6 (ground) both land here, with the logic and ESD returns.

TRIG_IN

Conditioned 3.3 V frame trigger from the board's input Schmitt into U702 (pin 2).

SYNC_IN

Conditioned 3.3 V Rsync from the board's input Schmitt into U703 (pin 2).

CAM_OUT_BNC

Exposure-active output; CAM_OUT through R705 (470 ohm); the BNC itself is the board's.

L0_INST

100 ohm tap (R707) on L0, camera Line 0 OPTOIN; the sync drive.

L1_INST

100 ohm tap (R708) on L1_BUF, camera Line 1 OPTOOUT after the Schmitt buffer.

L2_INST

100 ohm tap (R709) on L2, camera Line 2, the open-drain exposure output.

L3_INST

100 ohm tap (R710) on L3, camera Line 3, the frame trigger.

OUT_INST

100 ohm tap (R711) on CAM_OUT, the buffered exposure signal.

INTERNAL NETS

CAM_OUT: Buffered Line 2 (exposure active) from U701A 1Y; drives the BNC resistor, the LED resistor and the OUT tap.

L0: Camera pin 2, Line 0 OPTOIN; open-drain U703 Y, pulled to +5V by R703 (820 ohm), clamped by U704.

L1: Camera pin 4, Line 1 OPTOOUT, pulled up to +3.3V by R702 (4.7 k), into Schmitt 2A, clamped by U705.

L1_BUF: Schmitt 2Y; buffered Line 1 for the L1_INST tap.

L2: Camera pin 3, Line 2 as open-drain exposure output, pulled up by R701 (1 k), into Schmitt 1A, clamped by U705.

L3: Camera pin 1, Line 3 GPI trigger, driven by U702 through R704 (220 ohm), clamped by U704.

L3_DRV: U702 Y, the trigger drive before the 220 ohm series resistor.

LED_A: LED anode; R706 (680 ohm) from CAM_OUT, so D701 lights while exposure is active.

OPERATION

Camera side: J701's terminal numbers are the camera's Hirose HR10A-7R-6PB pin numbers, wired with the FLIR 1 m flying-lead GPIO cable into a Phoenix MC 1.5/6-ST-3.5 plug; pin 1 green Line 3 (GPI, trigger), pin 2 black Line 0 (OPTOIN, sync), pin 3 red Line 2 (GPIO, exposure output), pin 4 white Line 1 (OPTOOUT), pin 5 blue opto ground and pin 6 brown ground, both on GND (common-ground wiring).

Trigger path: TRIG_IN -> U702 (SN74LVC1G125, OE pin 1 grounded, so always enabled) -> L3_DRV -> R704 (220 ohm) -> L3 -> camera Line 3; camera settings TriggerSelector FrameStart, TriggerSource Line3 RisingEdge. Sync path: SYNC_IN -> U703 (SN74LVC1G07 open drain) -> L0, pulled to +5V by R703 (820 ohm); 5 V across 820 ohm is about 6 mA, less by the opto input's forward drop. Both drivers run from +3.3V with 5.5 V-tolerant I/O.

Exposure output: camera Line 2 (LineMode Output, LineSource ExposureActive, V3.3Enable false, so open drain) is pulled up by R701 (1 k) to +3.3V and squared by Schmitt U701A 1A -> 1Y = CAM_OUT, which drives the BNC through R705 (470 ohm), the green LED D701 through R706 (680 ohm; about (3.3 - 2.1) / 680 = 1.8 mA, LED on while exposure is active) and the OUT_INST tap. Line 1 (OPTOOUT, LineSource Off) is pulled up by R702 (4.7 k) and buffered 2A -> 2Y into L1_BUF for its tap.

ESD: two USBLC6-2P6 arrays with VBUS on +5V clamp L3 and L0 (U704) and L2 and L1 (U705), 15 kV IEC 61000-4-2 level 4, at most 3.5 pF per line; both I/O pins of each pair are wired to the node, so the footprint's paired pads need no track between them. +5V must therefore be a 5 V rail: it is the clamp reference and the opto drive level, and feeds nothing else.

Variants (family.json): mcv6_vertical fits J701 = OW-CONN-TBH-1X06-3P5-VERT (Phoenix MCV 1.5/6-G-3.5, top entry); mc6_horizontal fits OW-CONN-1844252 (Phoenix MC 1.5/6-G-3.5, side entry toward the footprint's +Y). The two footprints are pad-identical (six 1.8 x 3.6 mm ovals on 3.5 mm, origin at the pad-array centre), so the variant swaps only the connector's body, courtyard and 3D model; every pad, track and via stays, and the anchor connector_center is the same point for both.

The placing board provides +3.3V (bind it to the always-on rail when the taps must be observable before firmware runs), a 5 V rail on +5V, the BNC on CAM_OUT_BNC, the conditioned 3.3 V TRIG_IN and SYNC_IN, and the instrument port behind the five 100 ohm taps; the three pull-ups are inside because the block owns L0, L1 and L2 (layout convention 10). Place one block per camera; the horizontal variant's plug needs the board edge its wire exit faces.

DESIGN CONTRACT

One FLIR Blackfly S camera GPIO channel (trigger, sync, exposure output, instrument taps) on a 6-position 3.5 mm Phoenix header; the connector family pilot: the vertical MCV and the horizontal MC header are pad-identical, so one source publishes both orientations

Circuit and PCB layout guidance
Migrated from the saved family core; circuit, variants and PCB unchanged

Orb Weaver

Sheet: /blackfly_s_gpio_channel_mcv6_vertical2/
File: blackfly_s_gpio_channel_mcv6_vertical.kicad_sch

Title: Blackfly S GPIO channel family

Size: A2

Date: 2026-10-04

Rev: Source migration 1

KiCad E.D.A. 10.0.6

Id: 14/11