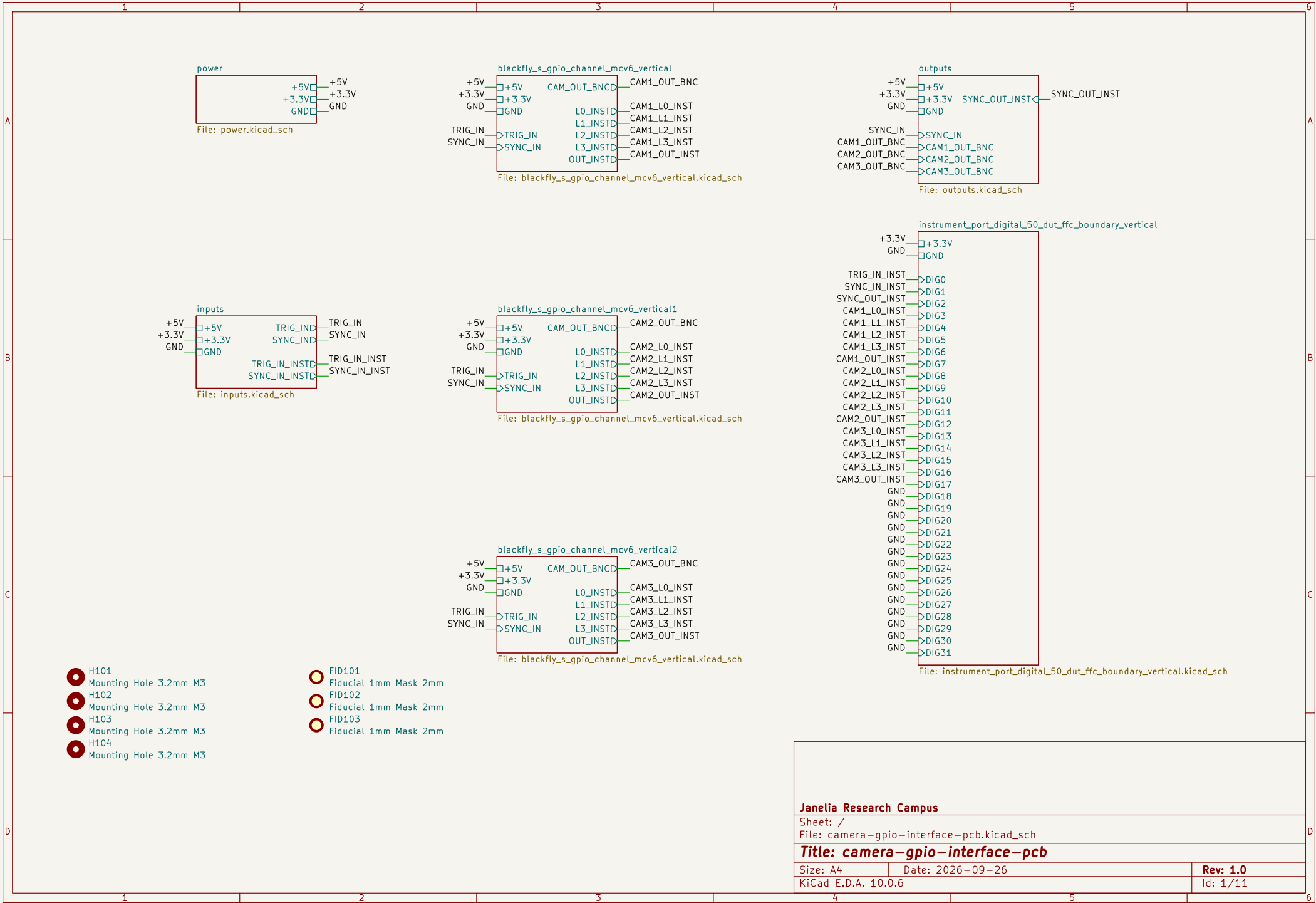




1

2

3

4

Blackfly S GPIO channel | trigger in, sync in, exposure out, five taps; vertical or horizontal header

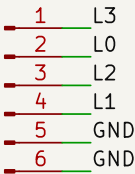
One FLIR Blackfly S camera GPIO channel (trigger, sync, exposure output, instrument taps) on a 6-position 3.5 mm Phoenix header; the connector family pilot: the vertical body; the horizontal body; the anchor; the clamps; the pads; the return. Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Camera header

J701, the 6-position 3.5 mm Phoenix header; pins 1 to 4 are Lines 3, 0, 2 and 1, pins 5 and 6 are the camera's two grounds.

J701

TBH-1x06-3.5mm



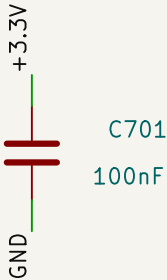
Camera GPIO header, 6-pos
3.5 mm

PLACE: Place J701 at the board edge the plug needs: the vertical body takes the plug from above, the horizontal from its +Y side; the anchor is the pad-array centre for both.

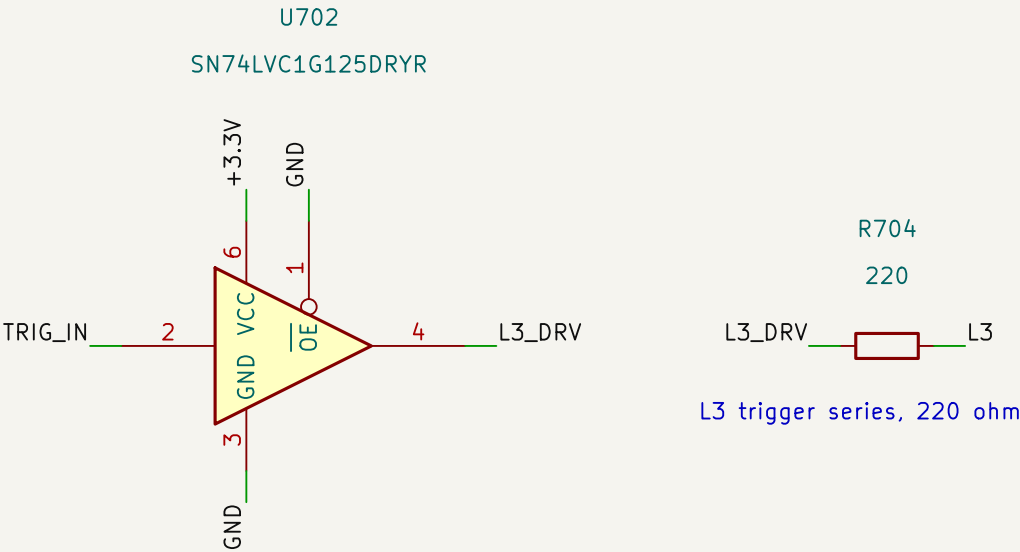
ROUTE: L3, L0, L2 and L1 run straight from the pads to their clamps and parts; GND from pins 5 and 6 into the block's return.

2. Line 3 trigger drive

U702 (always enabled) drives L3_DRV; R704 (220 ohm) in series feeds camera Line 3 on L3; C701 bypasses U702's VCC.



VCC pin 6 bypass, U702



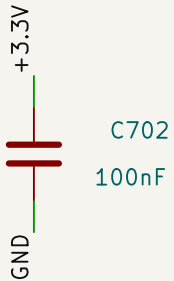
Line 3 trigger driver, always enabled

PLACE: Place U702 near J701 pin 1 with C701 at its pin 6 and a short return to pin 3; R704 between the driver and the connector.

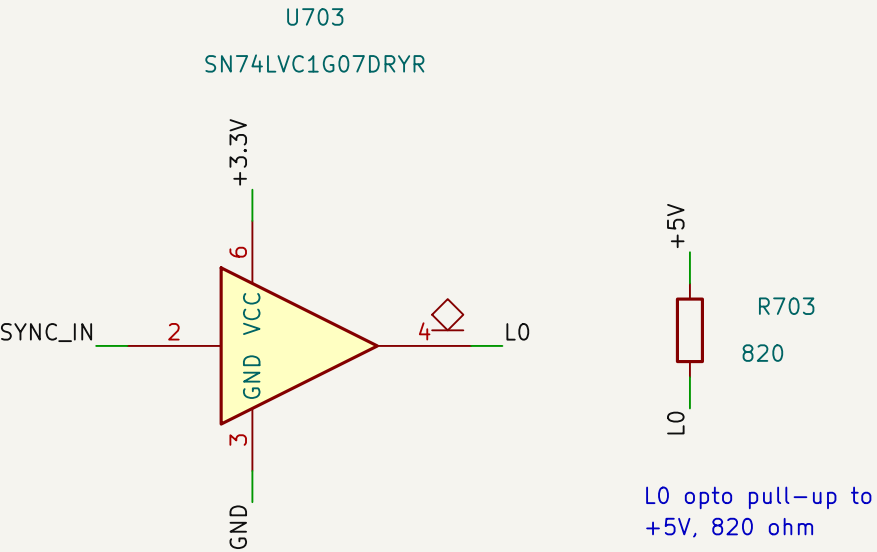
ROUTE: L3 is a 3.3 V edge-triggered line: short, over ground, away from the switching parts of the board.

3. Line 0 sync drive

U703's open-drain Y pulls L0 low; R703 (820 ohm) returns it to +5V, the opto input's drive level; C702 bypasses U703's VCC.



VCC pin 6 bypass, U703



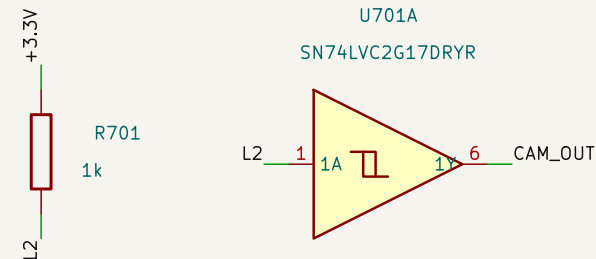
Line 0 sync driver, open drain

PLACE: Place U703 near J701 pin 2 with C702 at its pin 6; R703 from L0 to the +5V entry.

ROUTE: L0 carries about 6 mA pulses into the camera's opto input; keep its return with the trigger line.

4. Exposure output, BNC drive and LED

R701 pulls Line 2 up, U701A gate 1 squares it into CAM_OUT; R705 drives the BNC, R706 lights D701; R702 pulls Line 1 up and gate 2 buffers it into L1_BUF; C703 bypasses U701A.

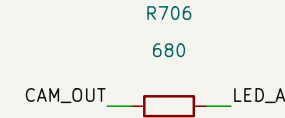


Unit 1: Schmitt buffers, L2 and L1

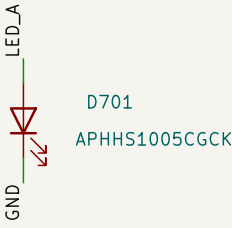
L2 pull-up to +3.3V, 1 k



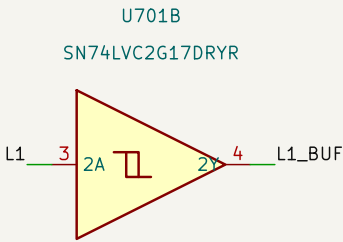
BNC drive series, 470 ohm



LED series, 680 ohm

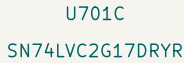


Exposure LED, green

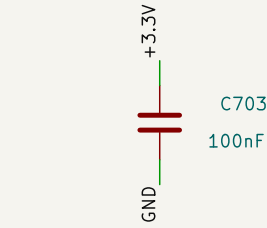


Unit 2: Schmitt buffers, L2 and L1

L1 pull-up to +3.3V, 4.7 k



Power unit



VCC pin 5 bypass, U701A

INTERNAL NETS

CAM_OUT: Buffered Line 2

L0: Camera pin 2, Line 0

L1: Camera pin 4, Line 1

L1_BUF: Schmitt 2Y: buffered

L2: Camera pin 3, Line 2

L3: Camera pin 1, Line 3

L3_DRV: U702 Y, the trigger

LED_A: LED anode: R706

OPERATION

Camera side: J701's terminals are connected to a Phoenix MC 1,5/6-ST-4 white Line 1 (OPTOOUT).

Trigger path: TRIG_IN -> Line 3; camera settings TRIG_IN, L0, pulled to +5V by R701, 5.5 V-tolerant I/O.

Exposure output: camera +3.3V and squared by Schmitt buffer U701A. R706 (680 ohm: about (3.3V/680) = 4.8mA, pulled up by R702 (4.7 k).

ESD: two USBLC6-2P6 are used for ESD protection, 100 pF per line; both I/O pins are connected to the +3.3V rail: it is the clamp reference.

Variants (family.json): model is Phoenix MC 1,5/6-ST-4 white Line 1 (OPTOOUT) (Phoenix 1844252) (Phoenix 3.5 mm, origin at the package center, the anchor connector_center).

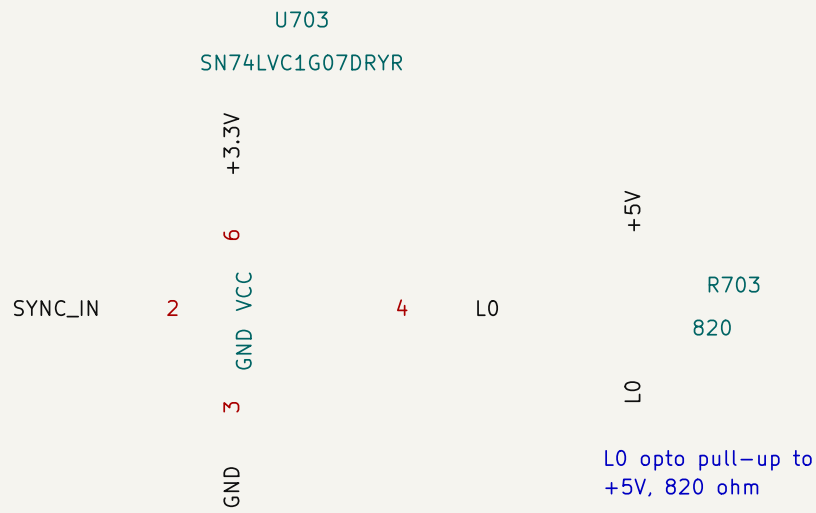
The placing board provides the connection on CAM_OUT_BNC, the connector is on the exit faces because the block owns the exit faces.

DESIGN CONTRACT

One FLIR Blackfly S camera family pilot: the vertical

PLACE: Place U701A between the connector and the BNC side with C703 at its pin 5; R701 and R702 at the connector pads; D701 where it is visible.

ROUTE: CAM_OUT is the board's exposure reference: route R705's far end to the BNC with a ground return beside it.



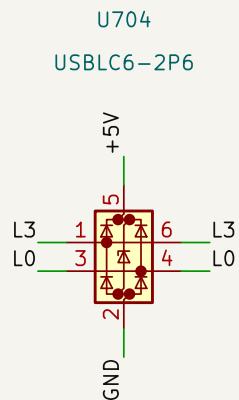
Line 0 sync driver, open drain

PLACE: Place U703 near J701 pin 2 with C702 at its pin 6; R703 from L0 to the +5V entry.

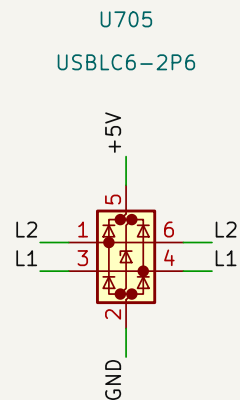
ROUTE: L0 carries about 6 mA pulses into the camera's opto input; keep its return with the trigger line.

5. ESD clamps

U704 clamps L3 and L0, U705 clamps L2 and L1, both referenced to +5V and GND; each pair's two I/O pins are tied to the node.



ESD array for L3/L0



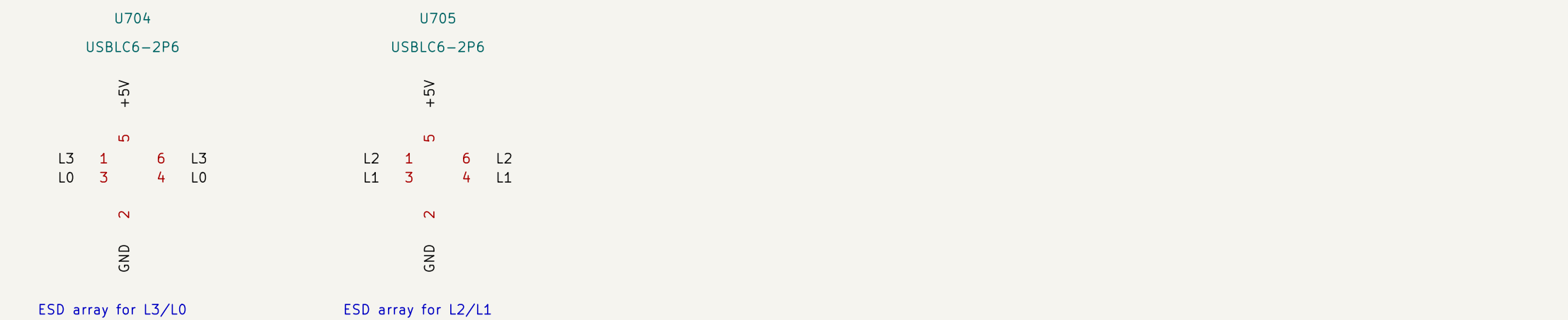
ESD array for L2/L1

PLACE: Place both arrays right at J701's pads, before any series part, with the shortest GND return.

ROUTE: Wire the paired I/O pads together on the node itself; no separate track between them.

5. ESD clamps

U704 clamps L3 and L0, U705 clamps L2 and L1, both referenced to +5V and GND; each pair’s two I/O pins are tied to the node.

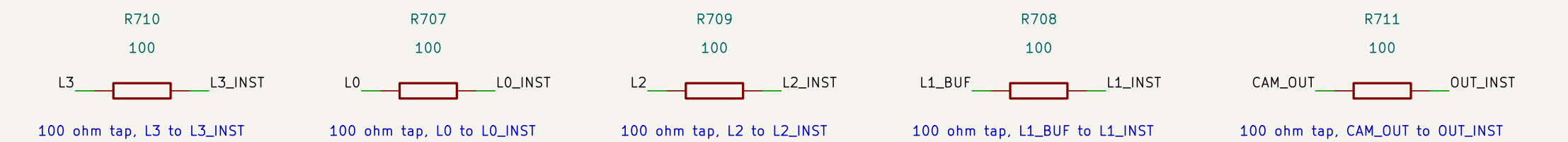


PLACE: Place both arrays right at J701’s pads, before any series part, with the shortest GND return.

ROUTE: Wire the paired I/O pads together on the node itself; no separate track between them.

6. Instrument taps

100 ohm series taps: R710 on L3, R707 on L0, R709 on L2, R708 on L1_BUF, R711 on CAM_OUT, each to its _INST port.



PLACE: Place the five taps as a row toward the instrument–port side of the block.

ROUTE: INSTRUMENT class to the instrument port; every tapped node has a DC definition (driven or pulled up).

INTERFACES

+5V  +5V

Must be a 5 V rail: the Line 0 opto drive level (R703) and both ESD clamps' VBUS reference.

+3.3V  +3.3V

Logic rail for U701A, U702, U703 and the L2/L1 pull-ups; always-on if the taps must read before firmware.

GND  GND

Camera pins 5 (opto ground) and 6 (ground) both land here, with the logic and ESD returns.

TRIG_IN  TRIG_IN

Conditioned 3.3 V frame trigger from the board's input Schmitt into U702 (pin 2).

SYNC_IN  SYNC_IN

Conditioned 3.3 V Rsync from the board's input Schmitt into U703 (pin 2).

CAM_OUT_BNC  CAM_OUT_BNC

Exposure-active output: CAM_OUT through R705 (470 ohm); the BNC itself is the board's.

L0_INST  L0_INST

100 ohm tap (R707) on L0, camera Line 0 OPTOIN: the sync drive.

L1_INST  L1_INST

100 ohm tap (R708) on L1_BUF, camera Line 1 OPTOOUT after the Schmitt buffer.

L2_INST  L2_INST

100 ohm tap (R709) on L2, camera Line 2, the open-drain exposure output.

L3_INST  L3_INST

100 ohm tap (R710) on L3, camera Line 3, the frame trigger.

OUT_INST  OUT_INST

100 ohm tap (R711) on CAM_OUT, the buffered exposure signal.

INTERNAL NETS

CAM_OUT: Buffered Line 2 (exposure active) from U701A 1Y; drives the BNC resistor, the LED resistor and the OUT tap.

L0: Camera pin 2, Line 0 OPTOIN: open–drain U703 Y, pulled to +5V by R703 (820 ohm), clamped by U704.

L1: Camera pin 4, Line 1 OPTOOUT, pulled up to +3.3V by R702 (4.7 k), into Schmitt 2A, clamped by U705.

L1_BUF: Schmitt 2Y: buffered Line 1 for the L1_INST tap.

L2: Camera pin 3, Line 2 as open–drain exposure output, pulled up by R701 (1 k), into Schmitt 1A, clamped by U705.

L3: Camera pin 1, Line 3 GPI trigger, driven by U702 through R704 (220 ohm), clamped by U704.

L3_DRV: U702 Y, the trigger drive before the 220 ohm series resistor.

LED_A: LED anode: R706 (680 ohm) from CAM_OUT, so D701 lights while exposure is active.

OPERATION

Camera side: J701’s terminal numbers are the camera’s Hirose HR10A–7R–6PB pin numbers, wired with the FLIR 1 m flying–lead GPIO cable into a Phoenix MC 1,5/6–ST–3,5 plug: pin 1 green Line 3 (GPI, trigger), pin 2 black Line 0 (OPTOIN, sync), pin 3 red Line 2 (GPIO, exposure output), pin 4 white Line 1 (OPTOOUT), pin 5 blue opto ground and pin 6 brown ground, both on GND (common–ground wiring).

Trigger path: TRIG_IN → U702 (SN74LVC1G125, $\overline{OE}$ pin 1 grounded, so always enabled) → L3_DRV → R704 (220 ohm) → L3 → camera Line 3; camera settings TriggerSelector FrameStart, TriggerSource Line3 RisingEdge. Sync path: SYNC_IN → U703 (SN74LVC1G07 open drain) → L0, pulled to +5V by R703 (820 ohm): 5 V across 820 ohm is about 6 mA, less by the opto input’s forward drop. Both drivers run from +3.3V with 5.5 V–tolerant I/O.

Exposure output: camera Line 2 (LineMode Output, LineSource ExposureActive, V3_3Enable false, so open drain) is pulled up by R701 (1 k) to +3.3V and squared by Schmitt U701A 1A → 1Y = CAM_OUT, which drives the BNC through R705 (470 ohm), the green LED D701 through R706 (680 ohm: about $(3.3 - 2.1) / 680 = 1.8$ mA, LED on while exposure is active) and the OUT_INST tap. Line 1 (OPTOOUT, LineSource Off) is pulled up by R702 (4.7 k) and buffered 2A → 2Y into L1_BUF for its tap.

ESD: two USBLC6–2P6 arrays with VBUS on +5V clamp L3 and L0 (U704) and L2 and L1 (U705), 15 kV IEC 61000–4–2 level 4, at most 3.5 pF per line; both I/O pins of each pair are wired to the node, so the footprint’s paired pads need no track between them. +5V must therefore be a 5 V rail: it is the clamp reference and the opto drive level, and feeds nothing else.

Variants (family.json): mcv6_vertical fits J701 = OW–CONN–TBH–1X06–3P5–VERT (Phoenix MCV 1,5/6–G–3,5, top entry); mc6_horizontal fits OW–CONN–1844252 (Phoenix MC 1,5/6–G–3,5, side entry toward the footprint’s +Y). The two footprints are pad–identical (six 1.8 x 3.6 mm ovals on 3.5 mm, origin at the pad–array centre), so the variant swaps only the connector’s body, courtyard and 3D model; every pad, track and via stays, and the anchor connector_center is the same point for both.

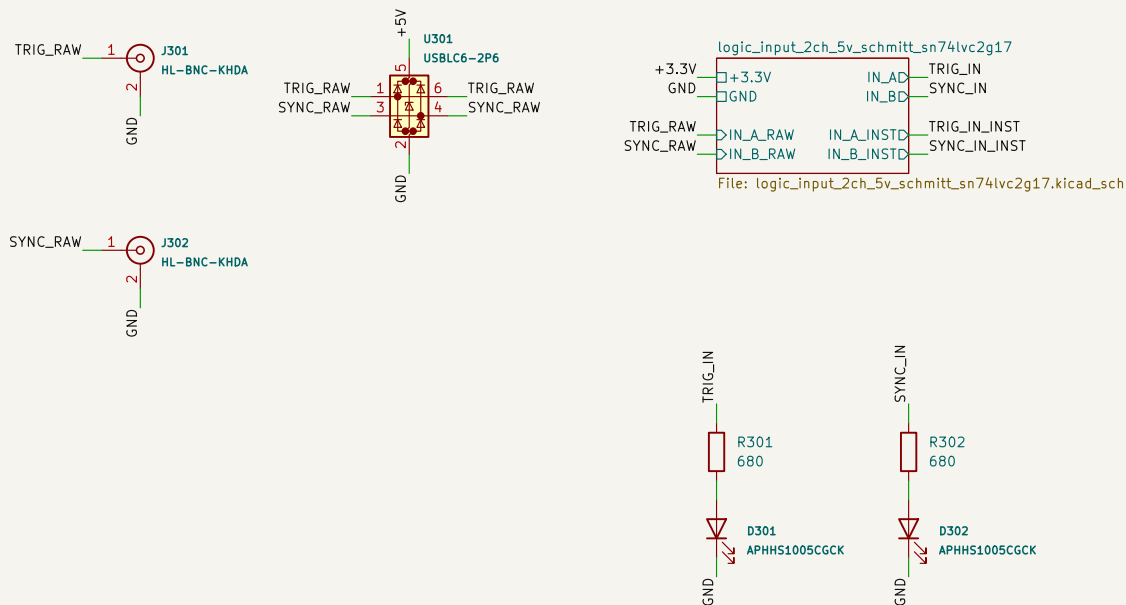
The placing board provides +3.3V (bind it to the always–on rail when the taps must be observable before firmware runs), a 5 V rail on +5V, the BNC on CAM_OUT_BNC, the conditioned 3.3 V TRIG_IN and SYNC_IN, and the instrument port behind the five 100 ohm taps; the three pull–ups are inside because the block owns L0, L1 and L2 (layout convention 10). Place one block per camera; the horizontal variant’s plug needs the board edge its wire exit faces.

DESIGN CONTRACT

One FLIR Blackfly S camera GPIO channel (trigger, sync, exposure output, instrument taps) on a 6–position 3.5 mm Phoenix header; the connector family pilot: the vertical MCV and the horizontal MC header are pad–identical, so one source publishes both orientations

+5V □ +5V
+3.3V □ +3.3V
GND □ GND

TRIG_IN □ TRIG_IN
SYNC_IN □ SYNC_IN
TRIG_IN_INST □ TRIG_IN_INST
SYNC_IN_INST □ SYNC_IN_INST



Janelia Research Campus

Sheet: /inputs/
File: inputs.kicad_sch

Title: camera-gpio-interface-pcb

Size: A4 Date: 2026-09-26

KiCad E.D.A. 10.0.6

Rev: 1.0

Id: 3/11

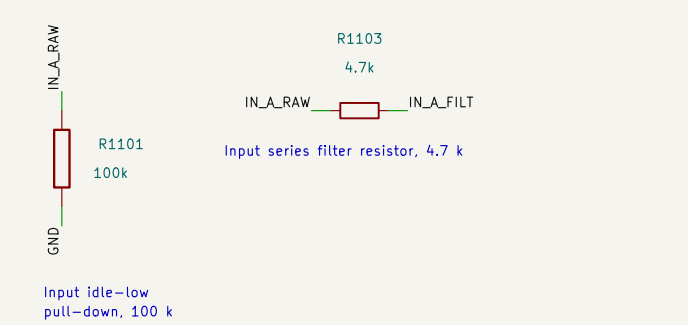
Two-channel Schmitt logic input | 4.7 k / 470 pF filters, SN74LVC2G17, pull-downs and taps

Two-channel single-ended logic input conditioner; per-channel series/RC filtering plus an SN74LVC2G17 dual Schmitt-trigger buffer that turns a 3.3 V or 5 V field-wired logic signal into clean 3.3 V logic, with a 100 ohm InstrumentPort tap on each output.

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Channel A Input filter

R1103 in series with the raw input into C1101 to GND forms the 72 kHz low-pass at 1A; R1101 holds IN_A_RAW low when nothing is plugged in.

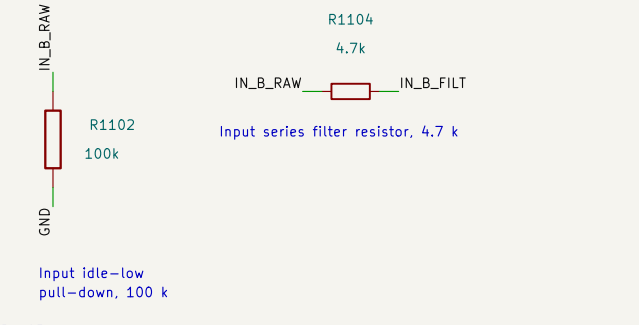


PLACE: Series resistors and filter capacitors on the input edge of the block. C1101 with a short return to GND at the buffer's pin 2 side; keep the raw pair away from motor bridge outputs with a ground reference beside it.

ROUTE: IN_A_RAW and IN_B_RAW enter as tracks (harness side); IN_A_FILT stays inside the block.

2. Channel B Input filter

The same network for channel B into 2A; R1102 holds IN_B_RAW low when unplugged.

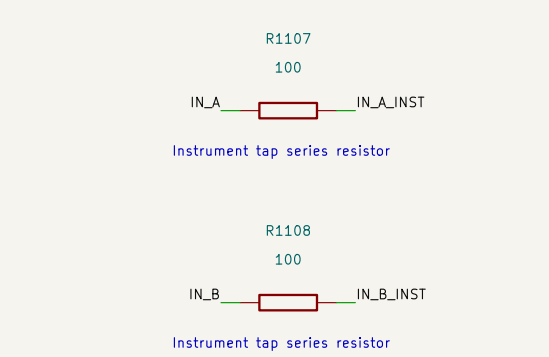


PLACE: Mirror channel A on the input edge so both channels see the same copper and the same delay.

ROUTE: IN_B_FILT stays inside the block.

3. Output pull-downs and Instrument taps

R1105/R1106 (100 k) define IN_A/IN_B while the buffer is unpowered; R1107/R1108 (100 ohm) are the series taps to IN_A_INST and IN_B_INST.

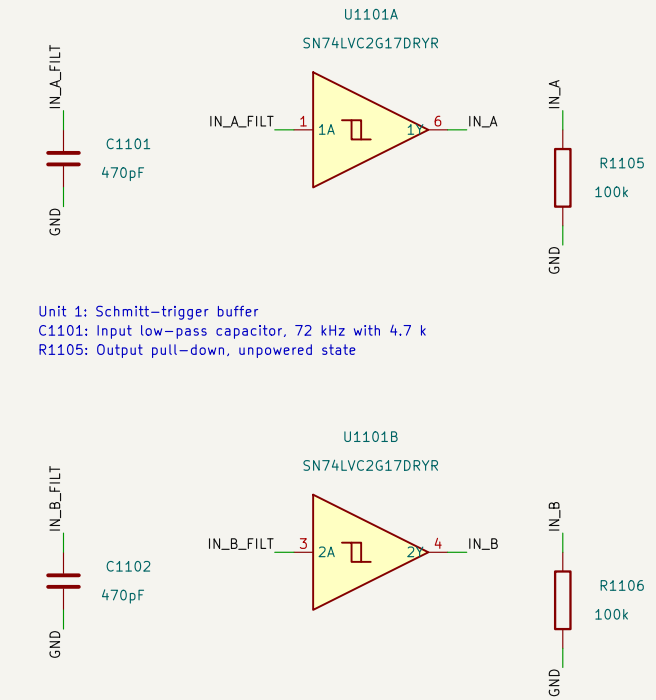
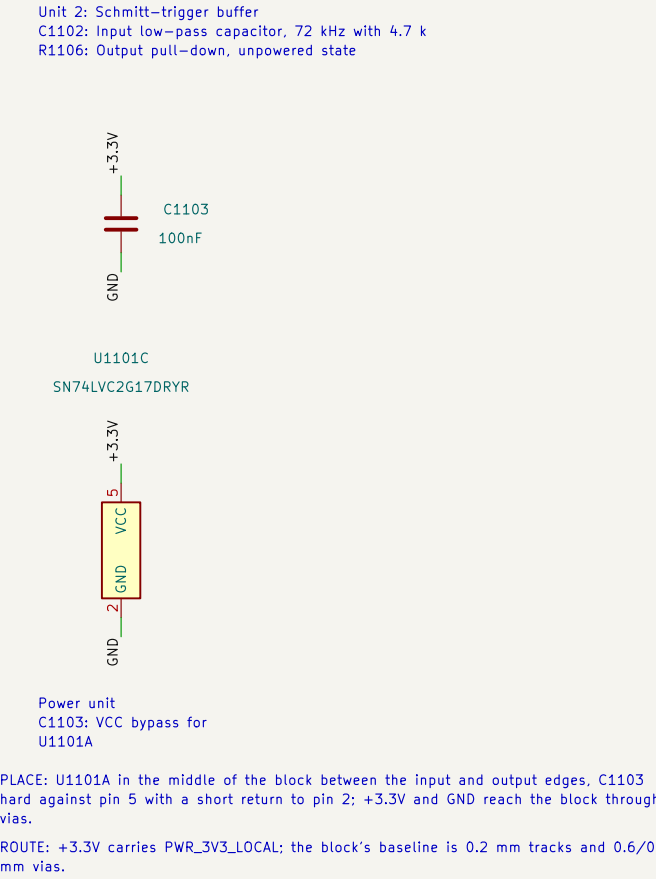


PLACE: Output pull-downs and taps on the output edge, so logic and tap nets leave on the side opposite the harness.

ROUTE: IN_A, IN_B, IN_A_INST and IN_B_INST leave through vias (port copper); the taps carry the INSTRUMENT class, the two tap stubs are 0.15 mm.

4. Schmitt buffer and supply bypass

U1101A gates A (1A to 1Y) and B (2A to 2Y) square the filtered inputs into 3.3 V logic; C1103 (100 nF) bypasses VCC (pin 5) to GND (pin 2).



PLACE: U1101A in the middle of the block between the input and output edges. C1103 hard against pin 5 with a short return to pin 2; +3.3V and GND reach the block through vias.

ROUTE: +3.3V carries PWR_3V3_LOCAL; the block's baseline is 0.2 mm tracks and 0.6/0.3 mm vias.

INTERFACES

+3.3V

Buffer supply (VCC, pin 5). 1.65 to 5.5 V; always-on when the taps must be observable before firmware runs, switched when the consumer of IN_A/IN_B powers down with it (loff keeps the unpowered outputs off the bus).

GND

Return for the buffer (pin 2). both filter capacitors and the four pull-downs.

IN_A_RAW

Field-wired channel A input. 0 to 5.5 V legal at any VCC; pulled low by R1101 (100 k) when unplugged.

IN_B_RAW

Field-wired channel B input. 0 to 5.5 V legal at any VCC; pulled low by R1102 (100 k) when unplugged.

IN_A_Q

Conditioned channel A. 3.3 V logic from 1Y (pin 6); pulled down by R1105 when the rail is off.

IN_B_Q

Conditioned channel B. 3.3 V logic from 2Y (pin 4); pulled down by R1106 when the rail is off.

IN_A_INST_Q

Instrument tap of IN_A through R1107 (100 ohm), INSTRUMENT class.

IN_B_INST_Q

Instrument tap of IN_B through R1108 (100 ohm), INSTRUMENT class.

OPERATION

Signal path, per channel: IN_A_RAW -> R1103 (4.7 k) -> IN_A_FILT (C1101 470 pF to GND) -> U1101A 1A (pin 1) -> 1Y (pin 6) -> IN_A, tapped through R1107 (100 ohm) to IN_A_INST; channel B is R1104, C1102, 2A (pin 3), 2Y (pin 4), IN_B and R1108 to IN_B_INST. R1101/R1102 (100 k) pull the raw inputs low when unplugged, on the harness side of the series resistor so no divider eats VIH margin; R1105/R1106 (100 k) define the outputs when +3.3V is off.

Filter: 4.7 k and 470 pF give a time constant of about 2.2 us and a corner near 72 kHz; a 3.3 V edge reaches the worst-case VT+ of 2.0 V about 2 us later, the same on both channels, so relative timing is kept. For faster edges swap C1101/C1102 (27 pF gives about 1.25 MHz).

The Schmitt input is the point: at VCC = 3 V, VT+ is 1.3 to 2.0 V and VT- 0.8 to 1.3 V with at least 0.4 V of hysteresis, so slow or noisy field edges cannot double-trigger; a 3.3 V source clears VT+ by at least 1.3 V, a 5 V TTL VDH of 2.4 V by 0.4 V. Inputs are rated 0 to 5.5 V at any VCC (6.5 V absolute), so a 5 V source is legal; a source below ground draws about 0.2 mA per volt through the 4.7 k (about 1 mA from -5 V), and a short to 36 V is bounded to about 7 mA into the buffer.

Supply: VCC 1.65 to 5.5 V, 10 uA max, +/-24 mA drive at 3 V; loff (10 uA max) keeps the outputs off a live downstream input when the rail is down, which is why the sequencing between source and buffer does not matter. C1103 (100 nF) bypasses pin 5.

DESIGN CONTRACT

Two-channel single-ended logic input conditioner; per-channel series/RC filtering plus an SN74LVC2G17 dual Schmitt-trigger buffer that turns a 3.3 V or 5 V field-wired logic signal into clean 3.3 V logic, with a 100 ohm InstrumentPort tap on each output. Generic sibling of quadrature_encoder_input_5v_sn74lvc2g17; same circuit and values, generic names, no encoder-supply passthrough. Use this one for BNC trigger and sync inputs, sensor and switch logic lines and any other pair of inputs a board conditions; use the encoder block when the harness also carries the encoder supply; place this block twice for four inputs. Connector-agnostic: the jack or terminal lives on the board sheet. Bring the raw lines in on IN_A_RAW and IN_B_RAW, take conditioned 3.3 V logic out on IN_A and IN_B and the taps out on IN_A_INST and IN_B_INST; rails +3.3V and GND. Per channel: R1103/R1104 4.7 kohm series (OW-RES-4K7-0402, C25900) into C1101/C1102 470 pF COG to ground (OW-CAP-470P-0402-COG-100V, C1518002) and U1101A SN74LVC2G17DRYR gate A/B (OW-MISC-SN74LVC2G17DRYR, C2675856); R1101/R1102 100 kohm pull-down (OW-PASS-RC0402JR-07100KL, C106234) on the harness side of the series resistor, so an unplugged input reads low without forming a divider that eats VIH margin; R1105/R1106 100 kohm pull-down on each output for loff high-Z, so an always-on downstream buffer never sees a floating input when this rail is down; R1107/R1108 100 ohm T-taps (OW-PASS-0402WGF1000TCE, C25076) to the _INST ports, INSTRUMENT netclass from the instrument-taps profile; C1103 100 nF (OW-CAP-100N-0402-X5R-16V, C162178) hard against U1101C pin 5.

The Schmitt input is the point of the block: an ordinary LVC buffer specifies a maximum input transition rate of about 8 ns/V, which a slow or noisy field edge violates and double-triggers; the 2G17 has no such limit and 0.4 V minimum hysteresis at 3 V. Thresholds VT+ <= 2.0 V and VT- >= 0.8 V, so a 3.3 V microcontroller pin clears the high threshold by 0.9 V or more and a 5 V TTL-level VDH of 2.4 V by 0.4 V.

Tolerance: inputs are rated 0 to 5.5 V at any valid VCC, 6.5 V absolute maximum, with no clamp diode to VCC, so a 5 V source plugged in by mistake is legal; a source held below ground draws about 0.2 mA per volt through the 4.7 kohm (a -5 V DAC output about 1 mA), and a short to a 36 V rail is bounded to about 7 mA and destroys a 0.19 USD buffer instead of the consumer.

Filter: 4.7 kohm and 470 pF give a 72 kHz corner and about 2 us from a 3.3 V edge to the Schmitt threshold, the same on both channels so their relative timing is preserved: 470 pF suits sub-10 kHz timing edges on long unshielded leads, swap C1101/C1102 for a faster corner when the signal needs it (27 pF gives 1.25 MHz).

Rails are generic labels: bind +3.3V to the always-on rail when the taps must be observable before firmware runs, or to the switched domain when the consumer of IN_A/IN_B can be powered down and must rise and fall with it; sequencing between source and buffer is a non-issue because loff disables the outputs when the part is unpowered.

First consumer: camera-gpio-interface-pcb, TRIG_IN and SYNC_IN BNCs from a pyControl breakout on IN_A_RAW/IN_B_RAW, TRIG_IN/SYNC_IN out, taps on DIG0/DIG1 of the digital-50 InstrumentPort.

Series resistors and filter capacitors on the input edge, the 2G17 and its decoupling in the middle, output pull-downs and taps on the output edge, so harness-side nets stay on one edge and logic and tap nets leave on the other. Keep the input pair away from motor bridge outputs and give it a ground reference.

Project-local pending bench verification; promotable once a second board uses it.

Circuit and PCB layout guidance
Migrated from the saved library sheet; circuit and PCB unchanged

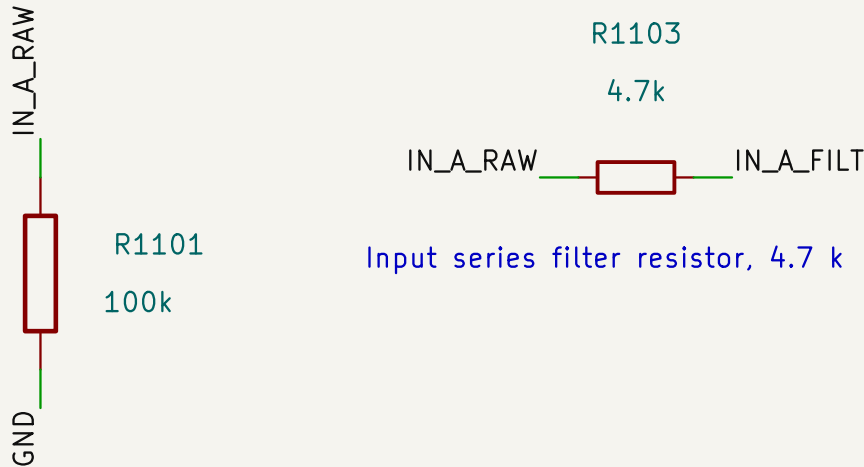
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File: logic_input_2ch_5v_schmitt_sn74lvc2g17.kicad_sch

Title: Two-channel Schmitt logic input

Size: A2 Date: 2026-10-04 Rev: Source migration 1
KiCad E.D.A. 10.0.6 Id: 11/11

1. Channel A input filter

R1103 in series with the raw input into C1101 to GND forms the 72 kHz low-pass at 1A; R1101 holds IN_A_RAW low when nothing is plugged in.



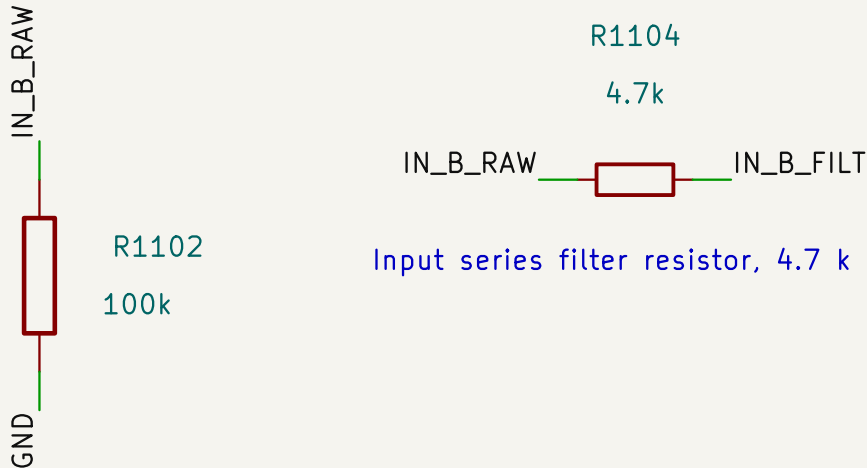
Input idle-low
pull-down, 100 k

PLACE: Series resistors and filter capacitors on the input edge of the block, C1101 with a short return to GND at the buffer's pin 2 side; keep the raw pair away from motor bridge outputs with a ground reference beside it.

ROUTE: IN_A_RAW and IN_B_RAW enter as tracks (harness side); IN_A_FILT stays inside the block.

2. Channel B input filter

The same network for channel B into 2A; R1102 holds IN_B_RAW low when unplugged.



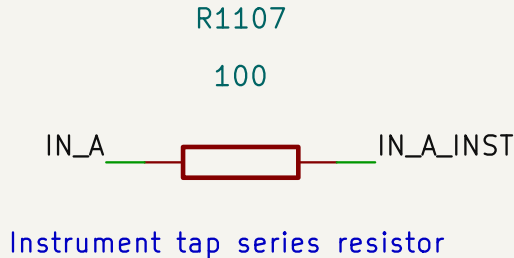
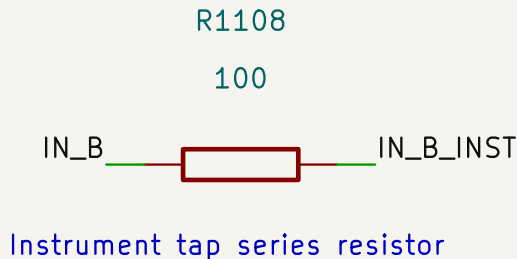
Input idle-low
pull-down, 100 k

PLACE: Mirror channel A on the input edge so both channels see the same copper and the same delay.

ROUTE: IN_B_FILT stays inside the block.

3. Output pull-downs and instrument taps

R1105/R1106 (100 k) define IN_A/IN_B while the buffer is unpowered;
R1107/R1108 (100 ohm) are the series taps to IN_A_INST and IN_B_INST.

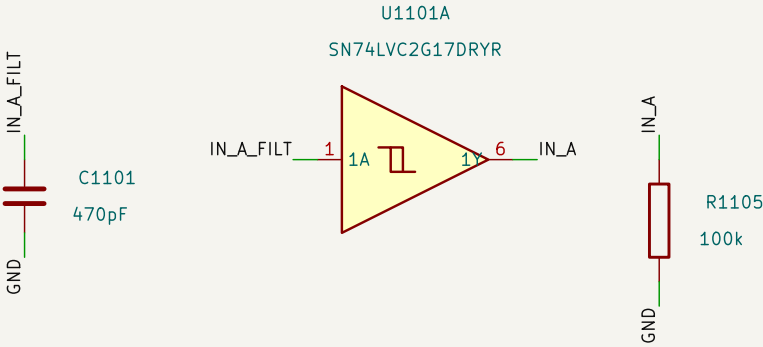


PLACE: Output pull-downs and taps on the output edge, so logic and tap nets leave on the side opposite the harness.

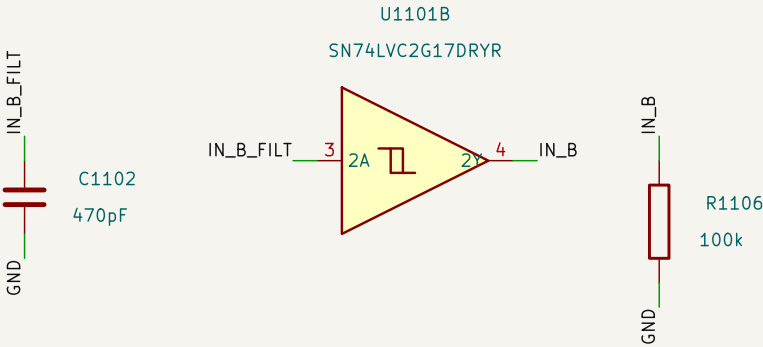
ROUTE: IN_A, IN_B, IN_A_INST and IN_B_INST leave through vias (port copper); the taps carry the INSTRUMENTclass, the two tap stubs are 0.15 mm.

4. Schmitt buffer and supply bypass

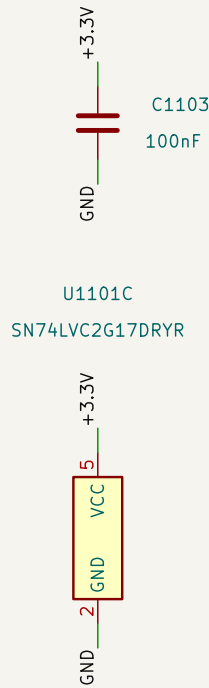
U1101A gates A (1A to 1Y) and B (2A to 2Y) square the filtered inputs into 3.3 V logic; C1103 (100 nF) bypasses VCC (pin 5) to GND (pin 2).



Unit 1: Schmitt-trigger buffer
C1101: Input low-pass capacitor, 72 kHz with 4.7 k
R1105: Output pull-down, unpowered state



Unit 2: Schmitt-trigger buffer
C1102: Input low-pass capacitor, 72 kHz with 4.7 k
R1106: Output pull-down, unpowered state



Power unit
C1103: VCC bypass for U1101A

PLACE: U1101A in the middle of the block between the input and output edges, C1103 hard against pin 5 with a short return to pin 2; +3.3V and GND reach the block through vias.

ROUTE: +3.3V carries PWR_3V3_LOCAL; the block's baseline is 0.2 mm tracks and 0.6/0.3 mm vias.

INTERFACES

+3.3V +3.3V
Buffer supply (VCC, pin 5), 1.65 to 5.5 V; always-on when the IN_A/IN_B powers down with it (loff keeps the unpowered outputs high).

GND GND
Return for the buffer (pin 2), both filter capacitors and the field-wired inputs.

IN_A_RAW IN_A_RAW
Field-wired channel A input, 0 to 5.5 V legal at any VCC; pulled down to GND by R1103 (4.7 k).

IN_B_RAW IN_B_RAW
Field-wired channel B input, 0 to 5.5 V legal at any VCC; pulled down to GND by R1104 (4.7 k).

IN_A IN_A
Conditioned channel A, 3.3 V logic from 1Y (pin 6); pulled down to GND by R1105 (100 k).

IN_B IN_B
Conditioned channel B, 3.3 V logic from 2Y (pin 4); pulled down to GND by R1106 (100 k).

IN_A_INST IN_A_INST
Instrument tap of IN_A through R1107 (100 ohm), INSTRUMENT netclass from the instrument-tap class.

IN_B_INST IN_B_INST
Instrument tap of IN_B through R1108 (100 ohm), INSTRUMENT netclass from the instrument-tap class.

OPERATION

Signal path, per channel: IN_A_RAW -> R1103 (4.7 k) -> IN_A_INST; channel B is R1104/R1102 (100 k) pull the raw inputs low when unplugged; R1105/R1106 (100 k) define the outputs when +3.3V is off.

Filter: 4.7 k and 470 pF give a time constant of about 2.2 us; if the input is high for 2.2 us later, the same on both channels, so relative timing is kept.

The Schmitt input is the point: at VCC = 3 V, VT+ is 1.3 to 2.0 V (not absolute), so a 5 V source is legal; a source below ground draws about 7 mA into the buffer.

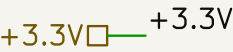
Supply: VCC 1.65 to 5.5 V, 10 uA max, +/-24 mA drive at 3 V; which is why the sequencing between source and buffer does not matter.

DESIGN CONTRACT

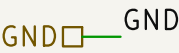
Two-channel single-ended logic input conditioner: per-channel 3.3 V or 5 V field-wired logic signal into clean 3.3 V logic, with a quadrature_encoder_input_5v_sn74lvc2g17: same circuit and value. sync inputs, sensor and switch logic lines and any other pair of encoder supply; place this block twice for four inputs. Connect IN_A_RAW and IN_B_RAW, take conditioned 3.3 V logic out on IN_A and IN_B. Per channel: R1103/R1104 4.7 kohm series (OW-RES-4K7-0402) (OW-CAP-470P-0402-C0G-100V, C1518202) and U1101A SN74LVC2G17 (OW-PASS-RC0402JR-073) reads low without forming a divider that eats VIH margin; R1105/R1106 downstream buffer never sees a floating input when this rail is low; the _INST ports, INSTRUMENT netclass from the instrument-tap class; U1101C pin 5.

The Schmitt input is the point of the block: an ordinary LVC buffer with field edge violates and double-triggers; the 2G17 has no such problem. V, so a 3.3 V microcontroller pin clears the high threshold by 0.7 V. Tolerance: inputs are rated 0 to 5.5 V at any valid VCC, 6.5 V max; is legal; a source held below ground draws about 0.2 mA per input; is bounded to about 7 mA and destroys a 0.19 USD buffer instead. Filter: 4.7 kohm and 470 pF give a 72 kHz corner and about 2.2 us; relative timing is preserved; 470 pF suits sub-10 kHz timing edge; signal needs it (27 pF gives 1.25 MHz). Rails are generic labels: bind +3.3V to the always-on rail where the consumer of IN_A/IN_B can be powered down and must risk disabling the outputs when the part is unpowered.

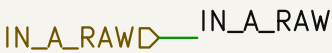
INTERFACES



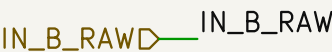
Buffer supply (VCC, pin 5), 1.65 to 5.5 V; always–on when the taps must be observable before firmware runs, switched when the consumer of IN_A/IN_B powers down with it (loff keeps the unpowered outputs off the bus).



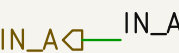
Return for the buffer (pin 2), both filter capacitors and the four pull–downs.



Field–wired channel A input, 0 to 5.5 V legal at any VCC; pulled low by R1101 (100 k) when unplugged.



Field–wired channel B input, 0 to 5.5 V legal at any VCC; pulled low by R1102 (100 k) when unplugged.



Conditioned channel A, 3.3 V logic from 1Y (pin 6); pulled down by R1105 when the rail is off.



Conditioned channel B, 3.3 V logic from 2Y (pin 4); pulled down by R1106 when the rail is off.



Instrument tap of IN_A through R1107 (100 ohm), INSTRUMENT class.



Instrument tap of IN_B through R1108 (100 ohm), INSTRUMENT class.

OPERATION

Signal path, per channel: IN_A_RAW -> R1103 (4.7 k) -> IN_A_FILT (C1101 470 pF to GND) -> U1101A 1A (pin 1) -> 1Y (pin 6) -> IN_A, tapped through R1107 (100 ohm) to IN_A_INST; channel B is R1104, C1102, 2A (pin 3), 2Y (pin 4), IN_B and R1108 to IN_B_INST. R1101/R1102 (100 k) pull the raw inputs low when unplugged, on the harness side of the series resistor so no divider eats VIH margin; R1105/R1106 (100 k) define the outputs when +3.3V is off.

Filter: 4.7 k and 470 pF give a time constant of about 2.2 us and a corner near 72 kHz; a 3.3 V edge reaches the worst-case VT+ of 2.0 V about 2 us later, the same on both channels, so relative timing is kept. For faster edges swap C1101/C1102 (27 pF gives about 1.25 MHz).

The Schmitt input is the point: at VCC = 3 V, VT+ is 1.3 to 2.0 V and VT- 0.8 to 1.3 V with at least 0.4 V of hysteresis, so slow or noisy field edges cannot double-trigger; a 3.3 V source clears VT+ by at least 1.3 V, a 5 V TTL VOH of 2.4 V by 0.4 V. Inputs are rated 0 to 5.5 V at any VCC (6.5 V absolute), so a 5 V source is legal; a source below ground draws about 0.2 mA per volt through the 4.7 k (about 1 mA from -5 V), and a short to 36 V is bounded to about 7 mA into the buffer.

Supply: VCC 1.65 to 5.5 V, 10 uA max, +/-24 mA drive at 3 V; loff (10 uA max) keeps the outputs off a live downstream input when the rail is down, which is why the sequencing between source and buffer does not matter. C1103 (100 nF) bypasses pin 5.

DESIGN CONTRACT

Two-channel single-ended logic input conditioner: per-channel series/RC filtering plus an SN74LVC2G17 dual Schmitt-trigger buffer that turns a 3.3 V or 5 V field-wired logic signal into clean 3.3 V logic, with a 100 ohm InstrumentPort tap on each output. Generic sibling of quadrature_encoder_input_5v_sn74lvc2g17: same circuit and values, generic names, no encoder-supply passthrough. Use this one for BNC trigger and sync inputs, sensor and switch logic lines and any other pair of inputs a board conditions; use the encoder block when the harness also carries the encoder supply; place this block twice for four inputs. Connector-agnostic: the jack or terminal lives on the board sheet. Bring the raw lines in on IN_A_RAW and IN_B_RAW, take conditioned 3.3 V logic out on IN_A and IN_B and the taps out on IN_A_INST and IN_B_INST; rails +3.3V and GND. Per channel: R1103/R1104 4.7 kohm series (OW-RES-4K7-0402, C25900) into C1101/C1102 470 pF COG to ground (OW-CAP-470P-0402-COG-100V, C1518202) and U1101A SN74LVC2G17DRYR gate A/B (OW-MISC-SN74LVC2G17DRYR, C2675856); R1101/R1102 100 kohm pull-down (OW-PASS-RC0402JR-07100KL, C106234) on the harness side of the series resistor, so an unplugged input reads low without forming a divider that eats VIH margin; R1105/R1106 100 kohm pull-down on each output for loff high-Z, so an always-on downstream buffer never sees a floating input when this rail is down; R1107/R1108 100 ohm T-taps (OW-PASS-0402WGF1000TCE, C25076) to the _INST ports, INSTRUMENT netclass from the instrument-taps profile; C1103 100 nF (OW-CAP-100N-0402-X5R-16V, C162178) hard against U1101C pin 5.

The Schmitt input is the point of the block: an ordinary LVC buffer specifies a maximum input transition rate of about 8 ns/V, which a slow or noisy field edge violates and double-triggers; the 2G17 has no such limit and 0.4 V minimum hysteresis at 3 V. Thresholds VT+ <= 2.0 V and VT- >= 0.8 V, so a 3.3 V microcontroller pin clears the high threshold by 0.9 V or more and a 5 V TTL-level VOH of 2.4 V by 0.4 V.

Tolerance: inputs are rated 0 to 5.5 V at any valid VCC, 6.5 V absolute maximum, with no clamp diode to VCC, so a 5 V source plugged in by mistake is legal; a source held below ground draws about 0.2 mA per volt through the 4.7 kohm (a -5 V DAC output about 1 mA), and a short to a 36 V rail is bounded to about 7 mA and destroys a 0.19 USD buffer instead of the consumer.

Filter: 4.7 kohm and 470 pF give a 72 kHz corner and about 2 us from a 3.3 V edge to the Schmitt threshold, the same on both channels so their relative timing is preserved; 470 pF suits sub-10 kHz timing edges on long unshielded leads, swap C1101/C1102 for a faster corner when the signal needs it (27 pF gives 1.25 MHz).

Rails are generic labels: bind +3.3V to the always-on rail when the taps must be observable before firmware runs, or to the switched domain when the consumer of IN_A/IN_B can be powered down and must rise and fall with it; sequencing between source and buffer is a non-issue because loff disables the outputs when the part is unpowered.

First consumer: camera-gpio-interface-pcb, TRIG IN and SYNC IN BNCs from a pyControl breakout on IN_A_RAW/IN_B_RAW, TRIG_IN/SYNC_IN out, taps on DIG0/DIG1 of the digital-50 InstrumentPort.

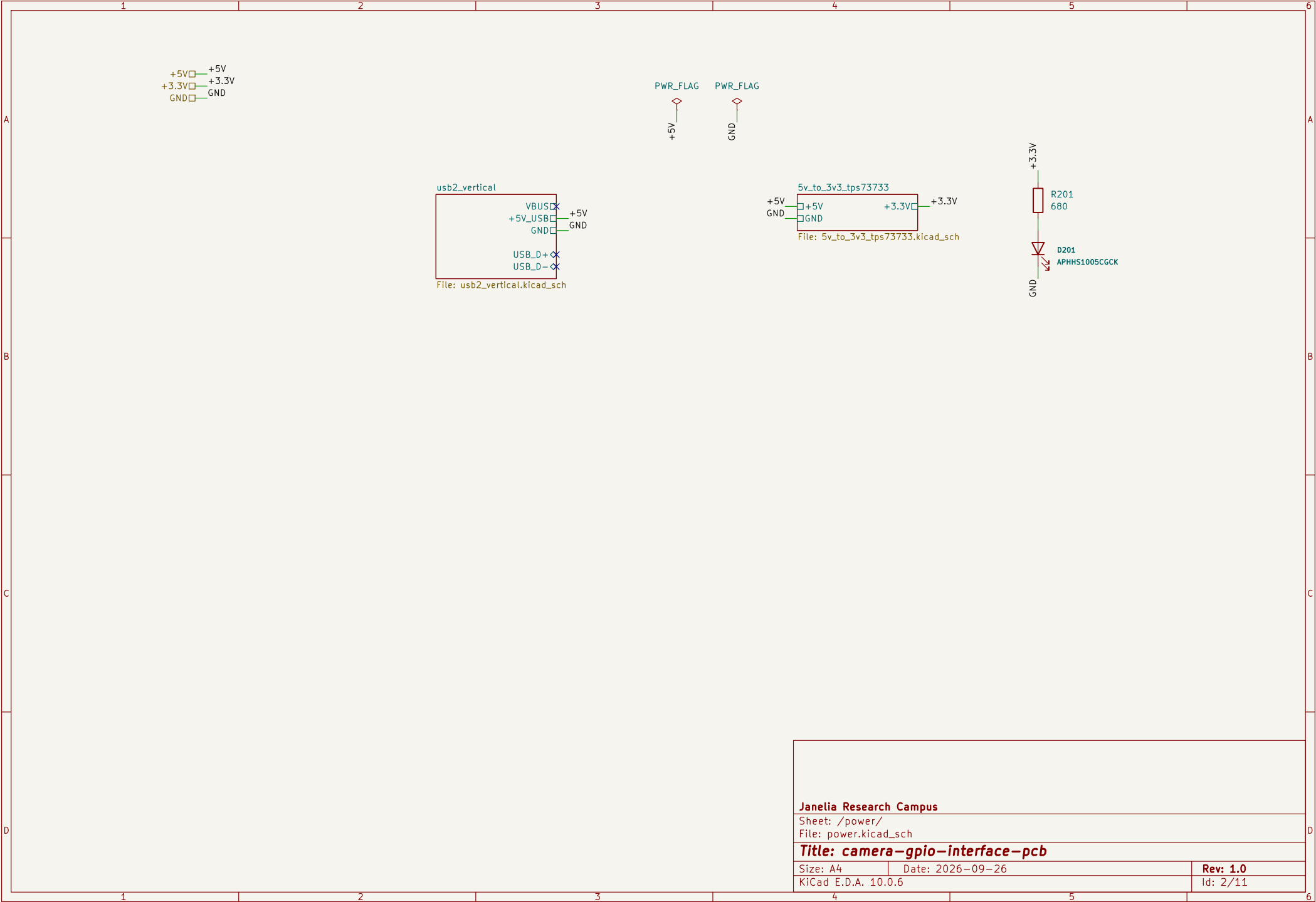
Series resistors and filter capacitors on the input edge, the 2G17 and its decoupling in the middle, output pull-downs and taps on the output edge, so harness-side nets stay on one edge and logic and tap nets leave on the other. Keep the input pair away from motor bridge outputs and give it a ground reference.

Project-local pending bench verification; promotable once a second board uses it.

D

E

F



Janelia Research Campus

Sheet: /power/
File: power.kicad_sch

Title: camera-gpio-interface-pcb

Size: A4

Date: 2026-09-26

Rev: 1.0

KiCad E.D.A. 10.0.6

Id: 2/11

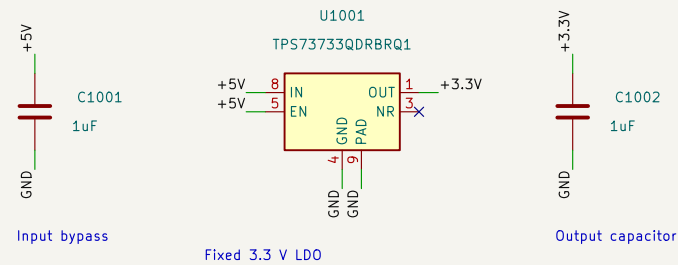
5 V to 3.3 V regulator | TPS73733 fixed 3.3 V LDO

Clean 3.3 V linear regulator from a 5 V input rail using the TI TPS73733 fixed 3.3 V 1 A LDO.

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Regulator and bypass

U1001 regulates +5V to +3.3V with EN tied to IN. C1001 bypasses IN to GND, C1002 holds OUT to GND; NR is open.



PLACE: Place C1001 at pins 8 and 4 and C1002 at pins 1 and 4 with short local ground returns; tie the thermal pad to GND copper.
ROUTE: +5V and +3.3V carry the rail classes (PWR_5V_LOCAL, PWR_3V3_LOCAL); the GND return of the pad is the regulator’s heat path as well.

INTERFACES

+5V — +5V
Input rail; also drives EN, so the regulator is on whenever it is present.

GND — GND
Common return; regulator ground pin and thermal pad.

+3.3V — +3.3V
Regulated output, 3.3 V fixed.

OPERATION

Signal path: +5V → U1001 (IN, pin 8) → +3.3V (OUT, pin 1). EN (pin 5) is tied to IN, so the regulator is on whenever +5V is present; there is no enable control inside this block.
NR (pin 3) is left open: no noise–reduction capacitor is fitted. GND (pin 4) and the thermal pad (pin 9) return to GND.
C1001 (1 uF) bypasses the input, C1002 (1 uF) is the output capacitor; both are the catalog 0402 1 uF part. The rail is rated by the TPS73733 (fixed 3.3 V, 1 A class per the catalog description); derate for the board’s actual load and dropout.

DESIGN CONTRACT

Clean 3.3 V linear regulator from a 5 V input rail using the TI TPS73733 fixed 3.3 V 1 A LDO. Intended for MCU, RP2040, TMC logic, encoder interface, and other low–voltage digital circuitry.

Circuit and PCB layout guidance
Migrated from the saved library sheet; circuit and PCB unchanged
Orb Weaver

Sheet: /power/5v_to_3v3_tps73733/
File: 5v_to_3v3_tps73733.kicad_sch

Title: 5 V to 3.3 V regulator

Size: A4	Date: 2026–10–04	Rev: Source migration 1
KiCad E.D.A. 10.0.6		Id: 10/11

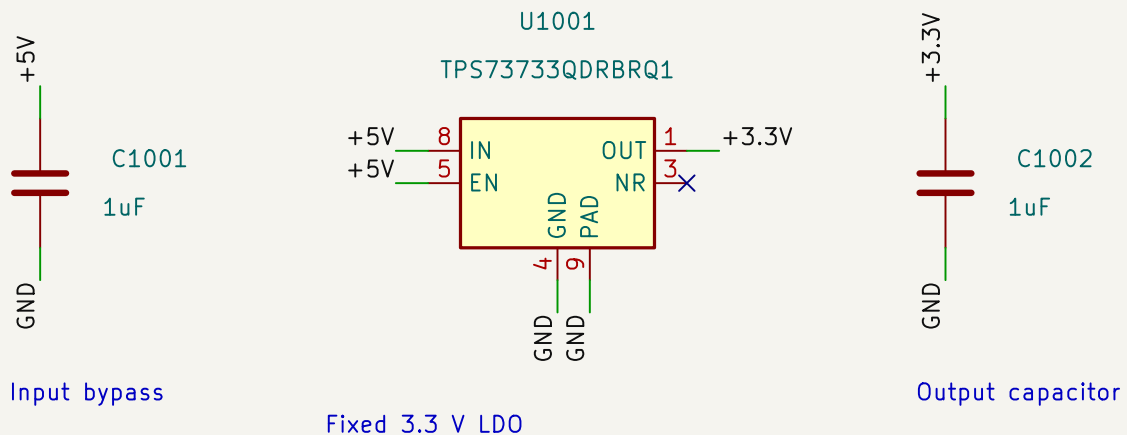
5 V to 3.3 V regulator | TPS73733 fixed 3.3 V LDO

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1. Regulator and bypass

U1001 regulates +5V to +3.3V with EN tied to IN. C1001 bypasses IN to GND, C1002 holds OUT to GND; NR is open.



PLACE: Place C1001 at pins 8 and 4 and C1002 at pins 1 and 4 with short local ground returns; tie the thermal pad to GND copper.

ROUTE: +5V and +3.3V carry the rail classes (PWR_5V_LOCAL, PWR_3V3_LOCAL); the GND return of the pad is the regulator's heat path as well.

INTERFACES

+5V □ — +5V

Input rail; also drives EN, so the regulator is on whenever it is present.

GND □ — GND

Common return; regulator ground pin and thermal pad.

+3.3V □ — +3.3V

Regulated output, 3.3 V fixed.

OPERATION

Signal path: +5V → U1001 (IN, pin 8) → +3.3V (OUT, pin 1). EN (pin 5) is tied to IN, so the regulator is on whenever +5V is present; there is no enable control inside this block.

NR (pin 3) is left open: no noise-reduction capacitor is fitted. GND (pin 4) and the thermal pad (pin 9) return to GND.

C1001 (1 uF) bypasses the input, C1002 (1 uF) is the output capacitor; both are the catalog 0402 1 uF part. The rail is rated by the TPS73733 (fixed 3.3 V, 1 A class per the catalog description); derate for the board's actual load and dropout.

DESIGN CONTRACT

Clean 3.3 V linear regulator from a 5 V input rail using the TI TPS73733 fixed 3.3 V 1 A LDO. Intended for MCU, RP2040, TMC logic, encoder interface, and other low-voltage digital circuitry.

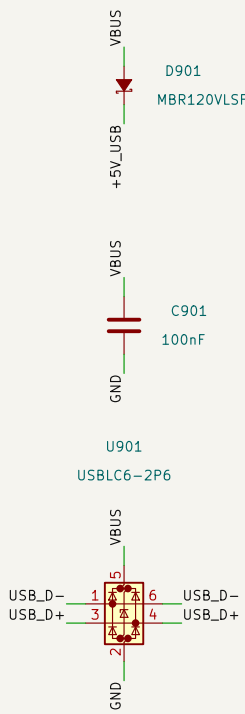
USB-C USB2 device port, vertical receptacle | USB4145, USBLC6 clamp, Rd 5.1 k, 5 V diode-OR

USB-C USB2 device-port front end on a VERTICAL, top-entry receptacle: GCT USB4145-03-0070-C, OW-CONN-USB-C-USB2-SMD-VERT, 16P USB2-only, SMT contacts plus four through-hole shell legs, 7.46 mm tall.

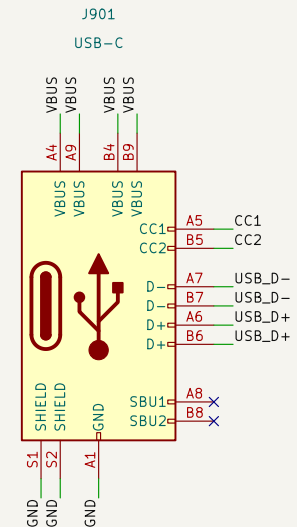
Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Receptacle and ESD clamp

J901 brings VBUS, GND, D+/D-, CC1/CC2 and the shell onto the board; U901 clamps USB_D+, USB_D- and VBUS to GND right at the receptacle. C901 holds the raw VBUS node at the clamp; D901 passes VBUS to +5V_USB and blocks the other 5 V source from feeding back into the host.



ESD clamp on D+, D- and VBUS
C901: VBUS bypass at the clamp
D901: Diode-OR Schottky



usb-connector

PLACE: Place U901 hard against J901 with a ground via at its pin 2; route each data line in one I/O pad and out the other.

PLACE: Place J901's four shell-leg holes and two locator pegs before pouring GND or routing the port; the part does not seat without them.

PLACE: Place C901 between U901 pin 5 and the GND via; D901 sits where +5V_USB leaves the block at its port via.

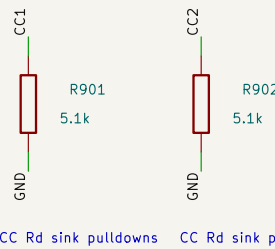
ROUTE: USB_D+ and USB_D- are the USB_HS pair; equal length, coupled at the class gap, brought to the block boundary already coupled.

ROUTE: Jump one leg of each pair once at the body centre for the A/B tie; the 0.3 mm gap at the outer contacts is unroutable.

ROUTE: VBUS and +5V_USB are Default-class rails for the port's 5 V budget; +5V_USB is picked up at the port via by the placing board.

2. CC sink declaration

R901 and R902 (5.1 k) pull CC1 and CC2 to GND; the port presents itself as a sink; nothing reads the source's advertisement.



CC Rd sink pulldowns CC Rd sink pulldowns

PLACE: Keep R901 at A5 and R902 at B5 with short returns; no other load on CC1 or CC2.

ROUTE: CC1 and CC2 are Default-class local nets that end at the resistors.

3. Power drive declarations

These nets have an explicit ERC power source declaration.



Power driven: VBUS

INTERFACES

VBUS

Raw bus 5 V, J901 A4, A9, B4, B9; bypassed by C901, the clamp's reference.

+5V_USB

VBUS through D901 (Schottky, about 0.3 V drop) for diode-ORing with +5V_PYC.

GND

USB ground: J901 A1, B1, A12, B12 and shell S1 to S4; clamp and Rd return.

USB_D+

USB 2.0 D+, J901 A6 and B6, after the U901 clamp; USB_HS pair with USB_D-.

USB_D-

USB 2.0 D-, J901 A7 and B7, after the U901 clamp; USB_HS pair with USB_D+.

INTERNAL NETS

CC1: Configuration channel for one plug orientation, J901 A5 to R901 (Rd, 5.1 k to GND); nothing reads it.

CC2: Configuration channel for the other orientation, J901 B5 to R902 (Rd, 5.1 k to GND); nothing reads it.

OPERATION

Signal path: J901 D+ (A6, B6) and D- (A7, B7) pass U901's I/O pads to USB_D+ and USB_D-; both receptacle rows are tied so either plug orientation works. SBU1 and SBU2 (A8, B8) are no-connect; USB2 only, for an RP2040-class device controller.

CC: R901 on CC1 (A5) and R902 on CC2 (B5), 5.1 k to GND, declare a UFP (sink). Nothing reads the CC level, so budget the load against a default-power source unless the host is known to advertise 1.5 A or 3 A.

ESD: U901 (USBLC6-2P6) clamps D+, D- and VBUS; 3.5 pF max per line, 1.7 pF max line to line, 6 V minimum VBUS breakdown, 12 V typical clamp at 1 A 8/20 us, IEC 61000-4-2 level 4 (15 kV air and contact). Clamp performance is set by connection inductance; pin 2 to a ground via, each data line in one I/O pad and out the other.

VBUS: C901 (100 nF) bypasses the raw bus; D901 (MBR120VLSFT1G, 20 V 1 A Schottky, 0.34 V max at 1 A, 0.6 mA leakage at 25 C) makes +5V_USB for diode-ORing with the pyControl block's +5V_PYC. The shell pads S1 to S4 are tied to GND here; isolate them through a pad/cap network instead if the shield must float.

Land pattern (from the block's own record): contacts in two rows on opposite sides of the body at 0.5 mm pitch, every pad 0.3 mm wide; the A/B ties for D+ and D- cross at the body centre with one via jump per pair leg and equal lengths; VBUS and GND each land on four pads to be used in parallel for the 3 A rating. Four plated shell legs and two 0.71 mm locator pegs are mandatory for seating. The cable leaves perpendicular to the board (7.46 mm connector height), so the enclosure needs an aperture above it.

DESIGN CONTRACT

USB-C USB2 device-port front end on a VERTICAL, top-entry receptacle: GCT USB4145-03-0070-C, OW-CONN-USB-C-USB2-SMD-VERT, 16P USB2-only, SMT contacts plus four through-hole shell legs, 7.46 mm tall. Electrically identical to the horizontal usb2 block; USBLC6-2P6 ESD clamp on D+/D- and VBUS, 5.1k Rd pulldowns on CC1 (A5) and CC2 (B5) declaring a sink, 100nF on VBUS, a MBR120VLSFT1G series Schottky from VBUS to +5V_USB for diode-ORing with other 5 V sources (pair it with pycontrol_behavior.port_lj45's +5V_PYC), PWR_FLAG on VBUS, SBU1/SBU2 deliberately unconnected, all four shell pads S1-S4 tied to GND. Ports are VBUS, +5V_USB, GND, USB_D+, USB_D-. Nothing reads the CC advertisement, so budget the load against a default-power source unless the host is known to advertise 1.5 A or 3 A. Only the land pattern differs from usb2, and it differs completely, which is why this is a separate block and not a footprint swap: contacts sit in two rows on OPPOSITE sides of the body at y = +/-4.485, 0.5 mm pitch across the six inner contacts and 1.5 mm out to the outer pads, and EVERY pad is 0.3 mm wide, where the horizontal GT-USB-7047C merges A and B into one row and gives VBUS and GND 0.6 mm pads. Three consequences follow for the layout. The A/B ties are the layout's work: D+ (A6/B6) and D- (A7/B7) cross at the body centre and cannot be taken around the ends, because the 0.3 mm gap between the outer contact and the shell-leg pad is unroutable at 0.2/0.2 and the plated leg blocks every layer there, so budget one via jump for one leg of the pair and keep both legs equal length. VBUS lands on four 0.3 mm pads (A4/A9/B4/B9) and GND on four (A1/A12/B1/B12); use all four of each in parallel for the 3 A rating and drop their ties to an inner layer rather than crowding the 1.8 mm corridor between the rows, which the two data joins need. The four shell legs are plated ovals on a 1.1 x 0.6 drill at x = +/-4 and punch every layer, and the two 0.71 mm NPTH locator pegs at (x/-4, 0) are mandatory for seating; place all six before pouring GND or routing the port. Mechanically the courtyard shrinks to x +/-5.05, y +/-2.31 from the horizontal part's x +/-6.00, y -1.25 to +6.75, so the connector stops needing about 6.75 mm of board past the contacts and can move inboard, but the cable now leaves perpendicular to the board; the enclosure needs an aperture above it plus clearance for the plug body and its wire loop, well beyond the 7.46 mm connector height. Keep the USBLC6 hard against the receptacle with a ground via at its pin 2 and route each data line in one I/O pad and out the other (clamp performance is dominated by connection inductance), and bring USB_D+/USB_D- to the block boundary already coupled at the USB_HS netclass gap. +5V_USB leaves D901 pad 1 into a port via, where a placing board picks the rail up.

Circuit and PCB layout guidance
Migrated from the saved library sheet; circuit and PCB unchanged

Orb Weaver

Sheet: /power/usb2_vertical/
File: usb2_vertical.kicad_sch

Title: USB-C USB2 device port, vertical

Size: A2 Date: 2026-10-04 Rev: Source migration 1
KiCad E.D.A. 10.0.6 Id: 9/11

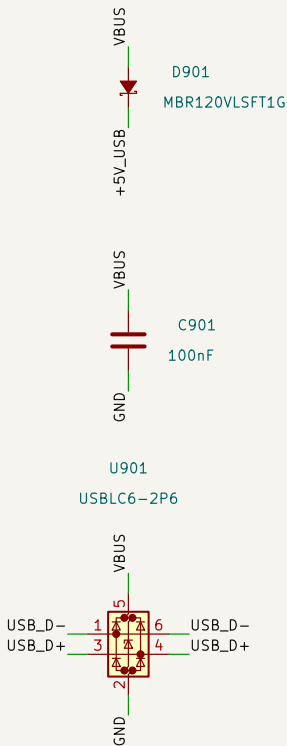
USB–C USB2 device port, vertical receptacle | USB4145, USBLC6 clamp, Rd 5.1 k, 5 V diode–OR

USB–C USB2 device–port front end on a VERTICAL, top–entry receptacle: GCT USB4145–03–0070–C, OW–CONN–USB–C–USB2–SMD–VERT, 16P USB2–only, SMT contacts

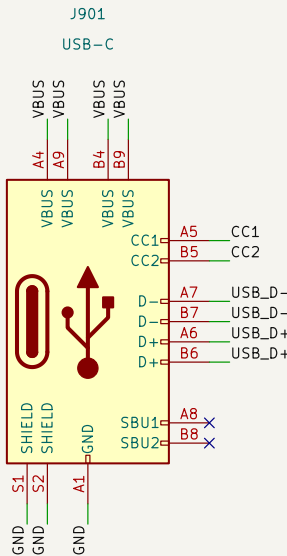
Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Receptacle and ESD clamp

J901 brings VBUS, GND, D+/D–, CC1/CC2 and the shell onto the board; U901 clamps USB_D+, USB_D– and VBUS to GND right at the receptacle. C901 holds the raw VBUS node at the clamp; D901 passes VBUS to +5V_USB and blocks the other 5 V source from feeding back into the host.



ESD clamp on D+, D– and VBUS
C901: VBUS bypass at the clamp
D901: Diode–OR Schottky



usb–connector

PLACE: Place U901 hard against J901 with a ground via at its pin 2; route each data line in one I/O pad and out the other.

PLACE: Place J901's four shell–leg holes and two locator pegs before pouring GND or routing the port; the part does not seat without them.

PLACE: Place C901 between U901 pin 5 and the GND via; D901 sits where +5V_USB leaves the block at its port via.

ROUTE: USB_D+ and USB_D– are the USB_HS pair: equal length, coupled at the class gap, brought to the block boundary already coupled.

ROUTE: Jump one leg of each pair once at the body centre for the A/B tie; the 0.3 mm gap at the outer contacts is unroutable.

ROUTE: VBUS and +5V_USB are Default–class rails for the port's 5 V budget; +5V_USB is picked up at the port via by the placing board.

5

6

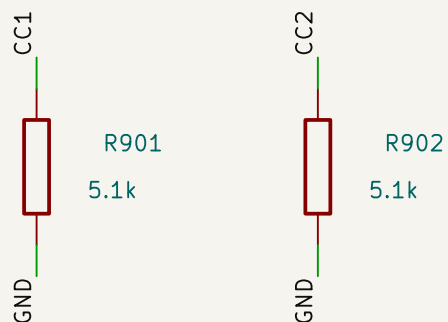
7

8

s four through-hole shell legs, 7.46 mm tall.

2. CC sink declaration

R901 and R902 (5.1 k) pull CC1 and CC2 to GND: the port presents itself as a sink; nothing reads the source's advertisement.



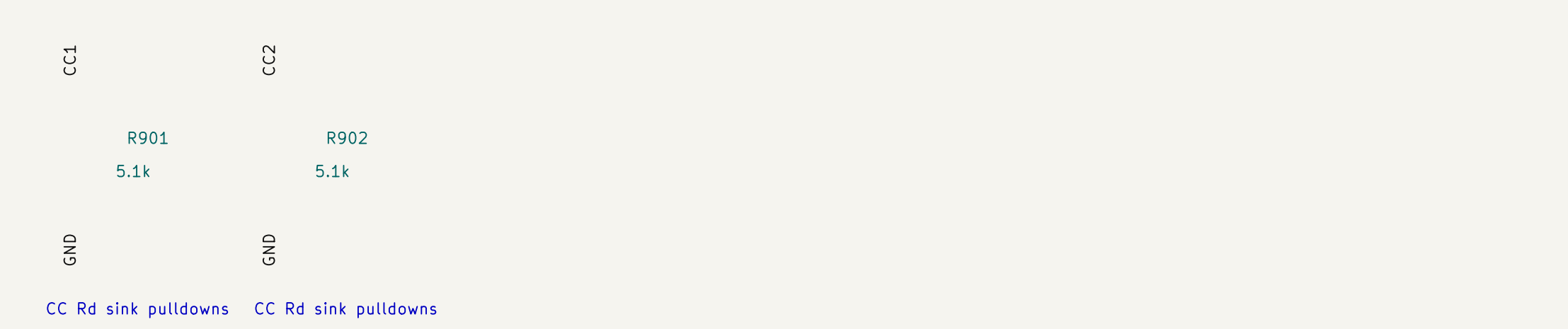
CC Rd sink pulldowns CC Rd sink pulldowns

PLACE: Keep R901 at A5 and R902 at B5 with short returns; no other load on CC1 or CC2.

ROUTE: CC1 and CC2 are Default-class local nets that end at the resistors.

2. CC sink declaration

R901 and R902 (5.1 k) pull CC1 and CC2 to GND; the port presents itself as a sink; nothing reads the source’s advertisement.

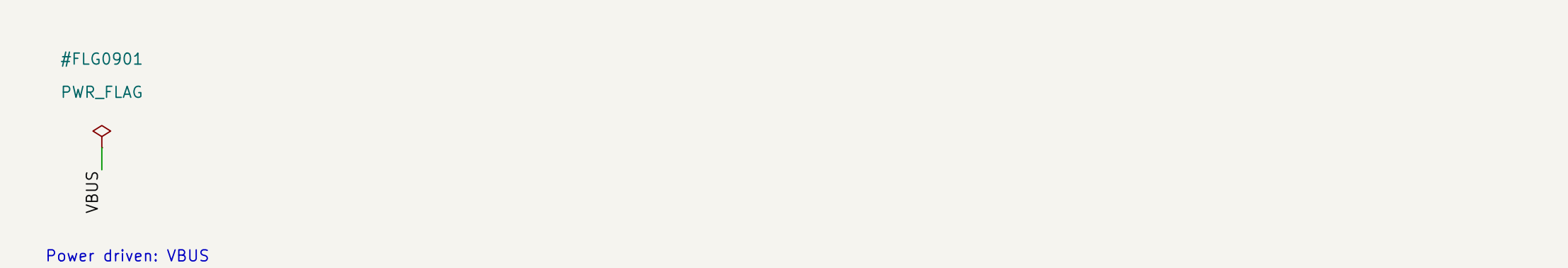


PLACE: Keep R901 at A5 and R902 at B5 with short returns; no other load on CC1 or CC2.

ROUTE: CC1 and CC2 are Default–class local nets that end at the resistors.

3. Power drive declarations

These nets have an explicit ERC power source declaration.



INTERFACES

VBUS □ — VBUS

Raw bus 5 V, J901 A4, A9, B4, B9; bypassed by C901, the clamp's reference.

+5V_USB □ — +5V_USB

VBUS through D901 (Schottky, about 0.3 V drop) for diode-ORing with +5V_PYC.

GND □ — GND

USB ground: J901 A1, B1, A12, B12 and shell S1 to S4; clamp and Rd return.

USB_D+ ◇ — USB_D+

USB 2.0 D+, J901 A6 and B6, after the U901 clamp; USB_HS pair with USB_D-.

USB_D- ◇ — USB_D-

USB 2.0 D-, J901 A7 and B7, after the U901 clamp; USB_HS pair with USB_D+.

INTERNAL NETS

CC1: Configuration channel for one plug orientation, J901 A5 to R901 (Rd, 5.1 k to GND); nothing reads it.

CC2: Configuration channel for the other orientation, J901 B5 to R902 (Rd, 5.1 k to GND); nothing reads it.

OPERATION

Signal path: J901 D+ (A6, B6) and D− (A7, B7) pass U901’s I/O pads to USB_D+ and USB_D−; both receptacle rows are tied so either plug orientation works. SBU1 and SBU2 (A8, B8) are no-connect: USB2 only, for an RP2040-class device controller.

CC: R901 on CC1 (A5) and R902 on CC2 (B5), 5.1 k to GND, declare a UFP (sink). Nothing reads the CC level, so budget the load against a default-power source unless the host is known to advertise 1.5 A or 3 A.

ESD: U901 (USBLC6-2P6) clamps D+, D− and VBUS: 3.5 pF max per line, 1.7 pF max line to line, 6 V minimum VBUS breakdown, 12 V typical clamp at 1 A 8/20 us, IEC 61000-4-2 level 4 (15 kV air and contact). Clamp performance is set by connection inductance: pin 2 to a ground via, each data line in one I/O pad and out the other.

VBUS: C901 (100 nF) bypasses the raw bus; D901 (MBR120VLSFT1G, 20 V 1 A Schottky, 0.34 V max at 1 A, 0.6 mA leakage at 25 C) makes +5V_USB for diode-ORing with the pyControl block’s +5V_PYC. The shell pads S1 to S4 are tied to GND here; isolate them through a pad/cap network instead if the shield must float.

Land pattern (from the block’s own record): contacts in two rows on opposite sides of the body at 0.5 mm pitch, every pad 0.3 mm wide; the A/B ties for D+ and D− cross at the body centre with one via jump per pair leg and equal lengths; VBUS and GND each land on four pads to be used in parallel for the 3 A rating. Four plated shell legs and two 0.71 mm locator pegs are mandatory for seating. The cable leaves perpendicular to the board (7.46 mm connector height), so the enclosure needs an aperture above it.

DESIGN CONTRACT

USB-C USB2 device-port front end on a VERTICAL, top-entry receptacle: GCT USB4145-03-0070-C, 0W-CONN-USB-C-USB2-SMD-VERT, 16P USB2-only, SMT contacts plus four through-hole shell legs, 7.46 mm tall. Electrically identical to the horizontal usb2 block: USBLC6-2P6 ESD clamp on D+/D− and VBUS, 5.1k Rd pulldowns on CC1 (A5) and CC2 (B5) declaring a sink, 100nF on VBUS, a MBR120VLSFT1G series Schottky from VBUS to +5V_USB for diode-ORing with other 5 V sources (pair it with pycontrol_behavior_port_rj45’s +5V_PYC), PWR_FLAG on VBUS, SBU1/SBU2 deliberately unconnected, all four shell pads S1-S4 tied to GND. Ports are VBUS, +5V_USB, GND, USB_D+, USB_D−.

Nothing reads the CC advertisement, so budget the load against a default-power source unless the host is known to advertise 1.5 A or 3 A. Only the land pattern differs from usb2, and it differs completely, which is why this is a separate block and not a footprint swap: contacts sit in two rows on OPPOSITE sides of the body at y = +/-1.485, 0.5 mm pitch across the six inner contacts and 1.5 mm out to the outer pads, and EVERY pad is 0.3 mm wide, where the horizontal GT-USB-7047C merges A and B into one row and gives VBUS and GND 0.6 mm pads. Three consequences follow for the layout. The A/B ties are the layout’s work: D+ (A6/B6) and D− (A7/B7) cross at the body centre and cannot be taken around the ends, because the 0.3 mm gap between the outer contact and the shell-leg pad is unroutable at 0.2/0.2 and the plated leg blocks every layer there, so budget one via jump for one leg of the pair and keep both legs equal length. VBUS lands on four 0.3 mm pads (A4/A9/B4/B9) and GND on four (A1/A12/B1/B12): use all four of each in parallel for the 3 A rating and drop their ties to an inner layer rather than crowding the 1.8 mm corridor between the rows, which the two data joins need. The four shell legs are plated ovals on a 1.1 x 0.6 drill at x = +/-4 and punch every layer, and the two 0.71 mm NPTH locator pegs at (+/-4, 0) are mandatory for seating: place all six before pouring GND or routing the port. Mechanically the courtyard shrinks to x +/-5.05, y +/-2.31 from the horizontal part’s x +/-6.00, y -1.25 to +6.75, so the connector stops needing about 6.75 mm of board past the contacts and can move inboard, but the cable now leaves perpendicular to the board: the enclosure needs an aperture above it plus clearance for the plug body and its wire loop, well beyond the 7.46 mm connector height.

Keep the USBLC6 hard against the receptacle with a ground via at its pin 2 and route each data line in one I/O pad and out the other (clamp performance is dominated by connection inductance), and bring USB_D+/USB_D− to the block boundary already coupled at the USB_HS netclass gap. +5V_USB leaves D901 pad 1 into a port via, where a placing board picks the rail up.

C

D

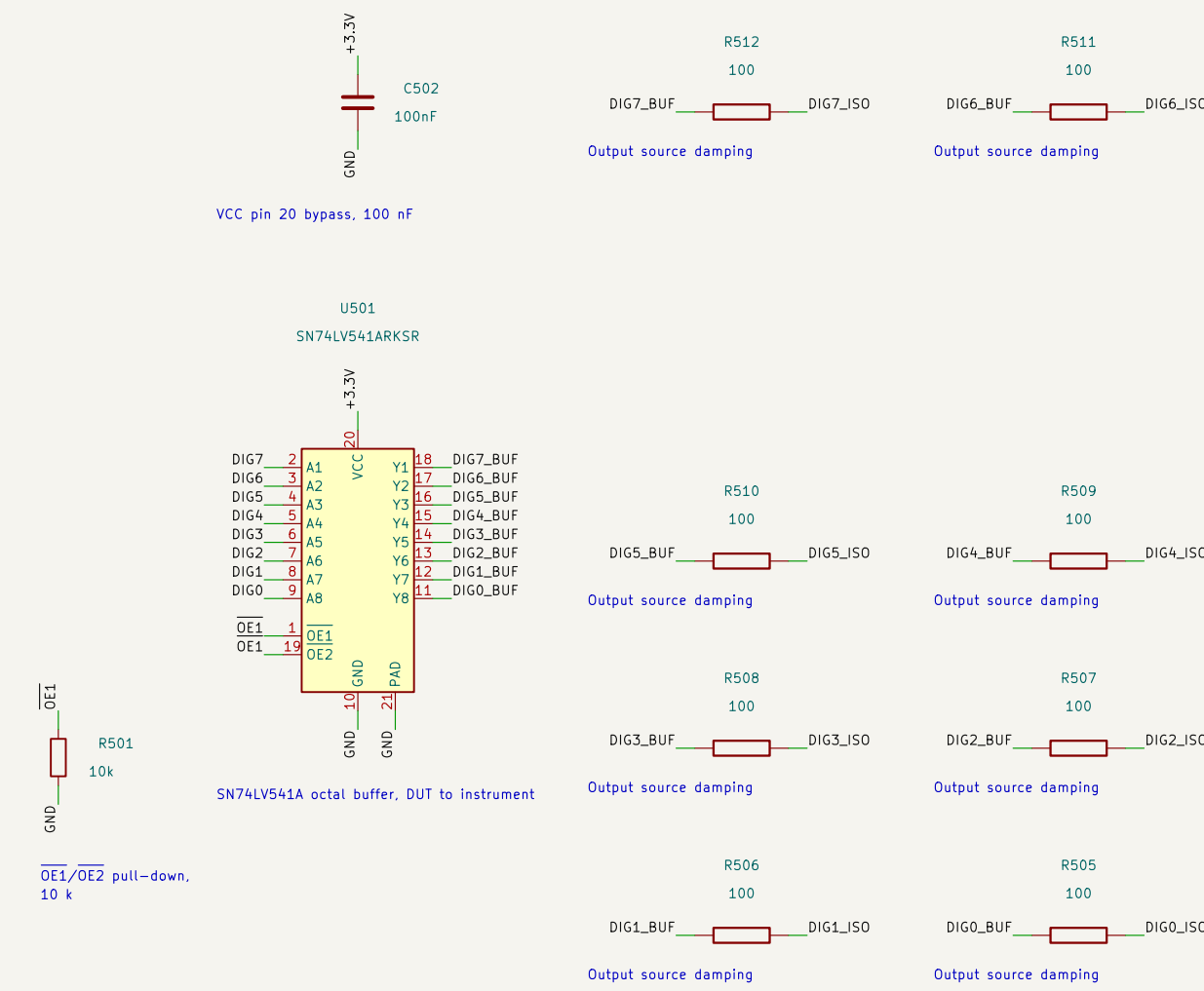
E

InstrumentPort-Digital-50 DUT Boundary | four SN74LV541A octets, 100 ohm damping, enabled by hardware

DUT-side InstrumentPort-Digital-50 with integrated read-only buffering, on a VERTICAL, top-entry 50-contact ZIF connector: Hirose FH12-50S-0-55VA(54). DW-CONN-FH12-50S-0-55VA-54, LCSC C597991, 0.5mm pitch, symbol Conn_01x50, footprint orb_weaver_connectors:Hirose_FH12-50S-0.55VA_1x50-4MP_P0.5mm_Vertical; the four mechanical lands are unnumbered pads and carry no net. Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Octet DIG0 to DIG7: U501

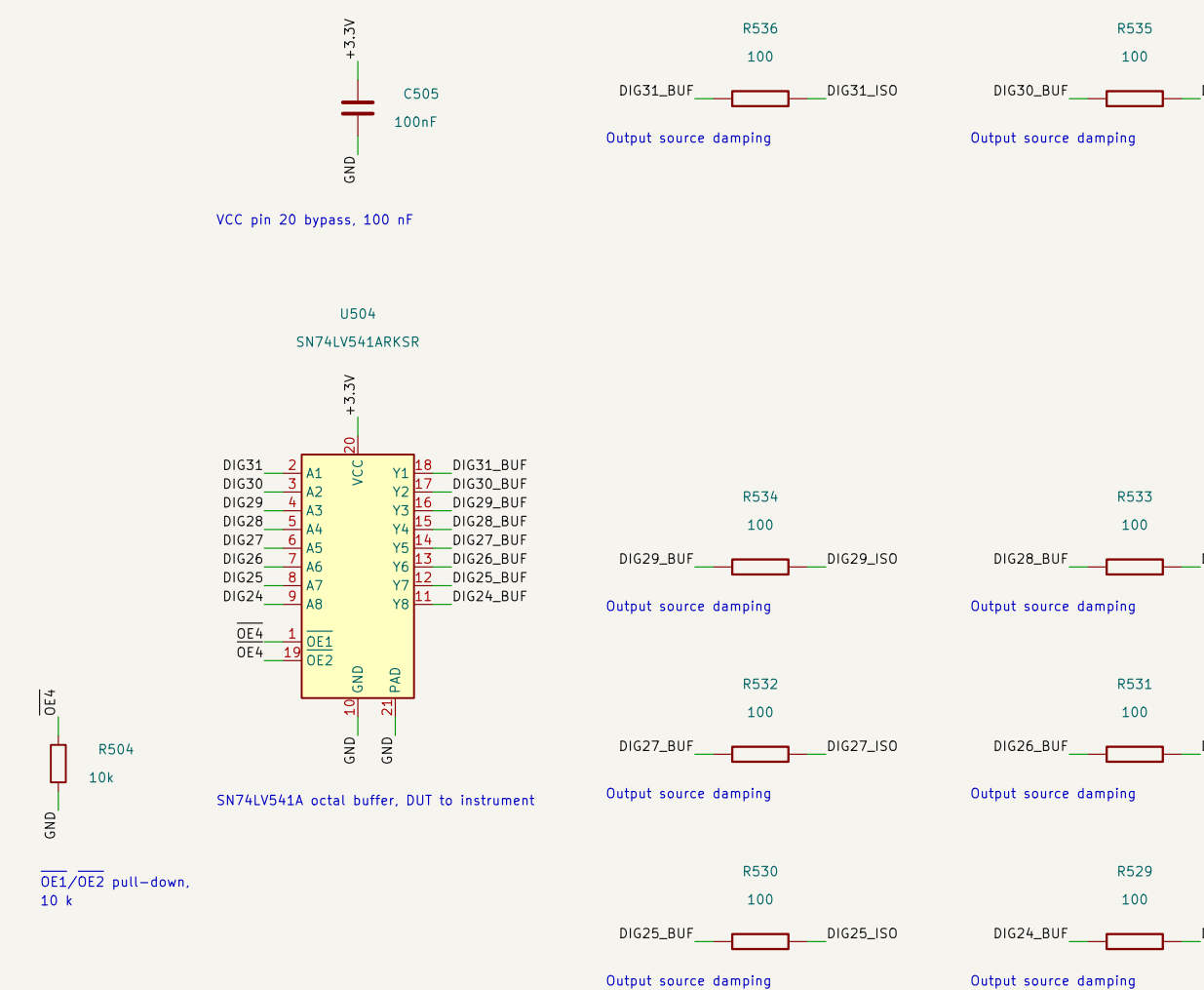
U501 buffers DIG0 to DIG7 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18); R505 to R512 (100 ohm) damp each output into its connector contact. C502 bypasses VCC (pin 20); R501 holds both enables (pins 1 and 19) low.



PLACE: Place C502 hard against pin 20 of U501 with a short return to pin 10 and the exposed pad 21; R501 near pins 1 and 19; the eight damping resistors between the Y pins and J501, outputs toward the connector.
ROUTE: The DIG0 to DIG7 inputs use this block's ports and escape toward the board on vias; keep the Y runs short to the resistors and the resistor-to-contact runs paired with the connector's ground contacts.

4. Octet DIG24 to DIG31: U504

U504 buffers DIG24 to DIG31 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18); R529 to R536 (100 ohm) damp each output into its connector contact. C505 bypasses VCC (pin 20); R504 holds both enables (pins 1 and 19) low.



PLACE: Place C505 hard against pin 20 of U504 with a short return to pin 10 and the exposed pad 21; R504 near pins 1 and 19; the eight damping resistors between the Y pins and J501, outputs toward the connector.
ROUTE: The DIG24 to DIG31 inputs use this block's ports and escape toward the board on vias; keep the Y runs short to the resistors and the resistor-to-contact runs paired with the connector's ground contacts.

OPERATION

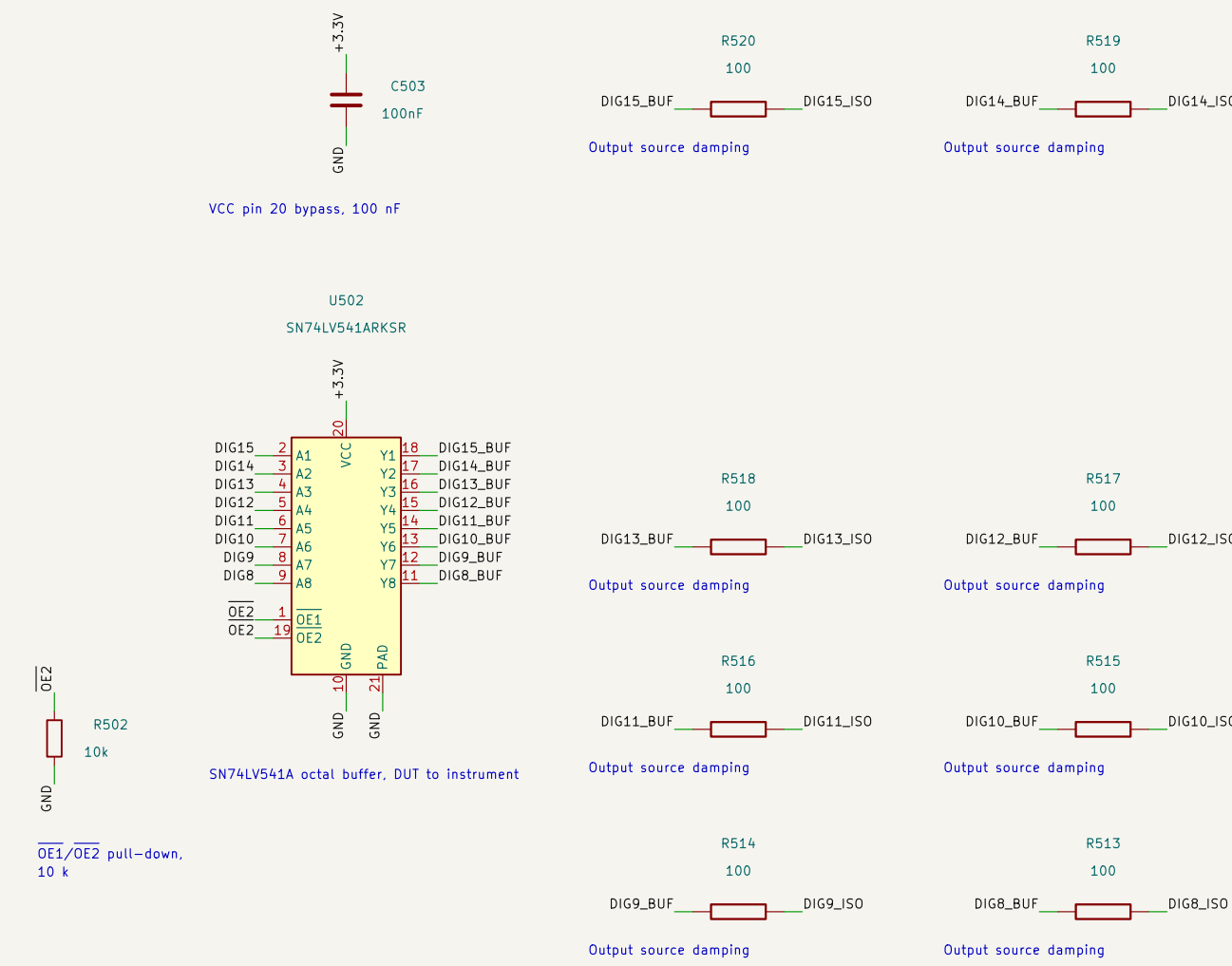
DUT side of the InstrumentPort-Digital-50 profile (board-interfaces/docs/instrument-port-digital.md, draft v0.1). Direction is a hardware property, DUT to Instrument only; DIGn enters U501 to U504 (DIG0 to 7, 9 to 15, 16 to 23, 24 to 31, each octet one package, A8 down to A1), leaves on Y8 to Y1 through 100 ohm damping (R505 to R536) onto J501. The cable carries no supply reference, enable or stimulus.
Pin mapping is the contract's DUT table and is not mirrored; channel n lands on contact 2 + n * floor((n/2)) + floor((n/16)). DIG0 on contact 2, DIG31 on contact 49; the 18 grounds on 1, 4, 7, ... 47, 50 with the 25/28 double ground at the bank boundary. The mirror lines on InstrumentPort_Digital_50_adapter.fxc_boundary.vertical: mirroring both ends cancels, and ERC and DRC cannot see it.
Enabled by hardware default, no disable at all; both active-low enables of each package share one net held low by its 10 k pull-down (R501 to R504; at most about 0.1 V from the two inputs' leakage against the 0.99 VIL, so observation works with the MCU in reset or unprogrammed. The contract permits this since 2026-09-15; do not re-add a control as a fix.
Supply the always-on 3.3 V rail to VCC (pin 20): SN74LV541A has 2 to 3.5 V drives +/-8 mA at 3.3 V; inputs tolerate 0 to 3.5 V with Ioff <= 1 uA unpowered. VIN 2.25 V, VIN 0.99 V, edges <= 100 ns/V, not a Schmitt input, C502 (100 fF) bypass each pin 20; C501 (4.7 uF, XSR 0402, well below nameplate at 3.3 V bias) is the one rail-entry bulk, not a fifth per-package bypass.
The 100 ohm damping bounds a hard short of one output to GND at 33 mA inside the +/-35 mA per-output absolute maximum, and damps edges into the cable; it is not short-circuit protection. Input bias is board-specific and not in this block; never must be tied at the board. Attach and remove the FFC with target power off; J501 is rated 20 mating cycles, so break the link at the instrument end.

DESIGN CONTRACT

DUT-side InstrumentPort-Digital-50 with integrated read-only buffering, on a VERTICAL, top-entry 50-contact ZIF connector: Hirose FH12-50S-0.55VA(54A), DW-CONN-FH12-50S-0-55VA-54, LCSC C597991, 0.5mm pitch, symbol Conn_01x50, footprint orb_weaver_connectors:Hirose_FH12-50S-0.55VA_1x50-4MP_P0.5mm_Vertical; the four mechanical lands are unnumbered pads and carry no net. Thirty-two channels through four SN74LV541A octet buffers (DW-HSC-SN74LV541A8RSR, C7384605, symbol orb_weaver_mhic:SN74LV541A8RSR, footprint orb_weaver_and:Keelec_KX50020A_V01N-20-1EP_2.5x5.5mm_P0.5mm_P1x3mm, exposed pad 21 to GND), grouped DIG0-7 / DIG8-15 / DIG16-23 / DIG24-31 to match the 13-contact octet windows. The 541 is flow-through input pin pairs with output pins 20 to 3, A1C1 to 1C1D through A8D1 to Y811. DIRECTION IS A HARDWARE PROPERTY; DUT to Instrument only. The cable carries no supply, no voltage reference, no enable and no stimulus, and nothing in this block may be driven by the instrument; PIN MAPPING IS THE CONTRACT'S DUT TABLE and IS NOT MIRRORRED; channel n lands on pin 2 + n * floor((n/2)) + floor((n/16)), so DIG0 to pin 2 and DIG31 to pin 49, with all 18 grounds on pins 1, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31, 34, 37, 40, 43, 46, 49 and 50. THE MIRROR LINES ON THE ADAPTER, NOT HERE, InstrumentPort_Digital_50_adapter.fxc_boundary.vertical is pre-mirrored to S1-- so that the expected reversing assembly -- same-side Type A FFC with a vertical FH12 at both ends, connectors rotated 180 degrees -- delivers DIGn to DRC. Mirroring both ends cancels and channels arrive as DIG2--. The ground pattern is palindromic, under S1-- so a mirrored map links every ground identically and every net stays direct and terminated; ERC, DRC and desktop_black-body check are ALL BLIND to this error, and only a pin-to-pin netlist comparison or continuity on the real cable catches it. Per-output source damping is 100 ohm, DW-PASS-0402W0100TCE. That value is chosen as the smallest standard one that bounds a hard short to ground inside the LV541A +/-35mA output absolute maximum even crediting the driver with zero impedance (3.3V/100k = 33mA); 68R gives 40mA, 47R gives 70mA, and the legacy 33R gives 100mA. It is NOT short-circuit protection and does not cover every fault; DEFAULT=ENABLED BY HARDWARE, AND THERE IS NO DISABLE AT ALL; both active-low DE inputs of each package share one net held low by a single 10k pull-down -- R501 through R504, one per package -- so observation works with the MCU held in reset, unprogrammed or unable to boot, and the port cannot be muted without desoldering. There is no manual jumper, no firmware flip and no OE port. The switching contract was relaxed on 2026-09-15 from requiring manual disabling to permitting none, so this conforms; the reasoning and the related future options are in Kicad/dns/docs/digital-instrument-port-design-block-and-net; No disable control, and why; DO NOT re-add a control as an oversight fix. Shared 10k is verified against aggregate leakage: 2 x 5uA max gives 0.1V at 0.99V VIL. If a noise investigation ever needs a mute, detaching the FFC bounds the cable's contribution but NOT the buffers', which keep switching into their board-side traces and damping resistors; OFF the 100R resistors on the suspect channels instead. SUPPLY FROM THE BOARD'S ALWAYS-ON 3.3V RAIL, independent of firmware, HVLIN and every switched domain; a buffer on a switched rail cannot observe the domain it is powering down with. DECOUPLING is one 100nF per package, C502 through C505, hard against each pin 20 with a short return, plus one 4.7uF rail-entry bulk, C501 / DW-CAP-047-0402-XSR-16V, at the supply entry, C501 is NOT a fifth per-IC bypass -- do not fix its distance to any package. Simultaneous-switching budget: 32 x 50pF x 3.3V = 5.2nC per all-channel edge, about 1mV of droop against the combined local reservoir. Expect meaningfully less than 4.7uF at 3.3V bias -- a 4.7uF XSR in an 0402 derates hard -- so treat the nameplate value as nominal, not measured. INPUT BIAS IS BOARD-SPECIFIC AND IS NOT IN THIS BLOCK; there is no universal pull-down, because SPI selects, open-drain buses and switched-domain paths each need different bias, and pulls that must hold HIGH on a switched net reference the switched rail, never the always-on net. Every unused input must be explicitly tied at the board, LV541A at 3.3V needs VIH = 2.31V and VIL <= 0.99V with transients <= 100 ns/V; it is 0-0.5V input tolerant with 20pF typical input capacitance and Ioff <= 5uA at VCC=0. It is NOT Schmitt-triggered and NOT a comparator; do not route a raw analog node through it for a timing wheress, and do not treat a clean legacy LVCMOS25 capture as LV541A qualification. OE would disable outputs only -- it never removes input loading or makes a floating input acceptable, which is part of why no mute was fitted. Requires straight-ended 0.25 +/-0.05mm PFC with gold contacts, at least 2mm exposed contact and 3mm reinforcement; retest-on-rear cable is NOT qualified for this connector. Rated 20 mating cycles, so prefer breaking the link at the instrument end, and attach or remove the cable with target power off unless the actual assembly is hot-swap qualified. Profile is InstrumentPort-Digital-50 draft v0.1, UNQUALIFIED; no measured rate, delay, skew, loading or power-side limit has been established. Marker/beacon channel indices are NOT frozen, with DIG0/DIG1 the current recommendation over the earlier DIGA/DIG15. Pairs with InstrumentPort_Digital_50_adapter.fxc_boundary.vertical; the analyzer-specific channel map belongs to LV5022 connector boundary, not here. GROUNDING: INPUTS AND THE BOARD'S COPPER: the inputs are the block's ports, so a board that grounds unused Dig channels draws one 0.20 mm track per grounded LV541A pad column straight into that package's thermal pad on F.Cu, before autorouting; freerouting will not run a track along a row of same-net 0.5 mm-pitch pads and left those groups ungrounded on every copper board run (layout convention 11a). Since 2026-09-29 every Dig also enters its own escape via above the pad row, so a board may instead tie an unused channel to ground at the other way the grounding copper is the better, never the worse; the 0.10 mm gaps between the 1.00 mm gaps between the 32 damping resistors and the LV541A pins (2026-09-29) and between each Dig escape stub and the escape via beside it (2026-09-29) are wrapped in BLOCK/LOOK rule areas, so a consuming board sees no clearance findings from this block under the shared rules: a board wasting 0.20 mm inside the block re-routes the block, not the rule layout convention 12).

2. Octet DIG8 to DIG15: U502

U502 buffers DIG8 to DIG15 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18); R513 to R520 (100 ohm) damp each output into its connector contact. C503 bypasses VCC (pin 20); R502 holds both enables (pins 1 and 19) low.



PLACE: Place C503 hard against pin 20 of U502 with a short return to pin 10 and the exposed pad 21; R502 near pins 1 and 19; the eight damping resistors between the Y pins and J501, outputs toward the connector.
ROUTE: The DIG8 to DIG15 inputs use this block's ports and escape toward the board on vias; keep the Y runs short to the resistors and the resistor-to-contact runs paired with the connector's ground contacts.

5. Rail-entry bulk bypass

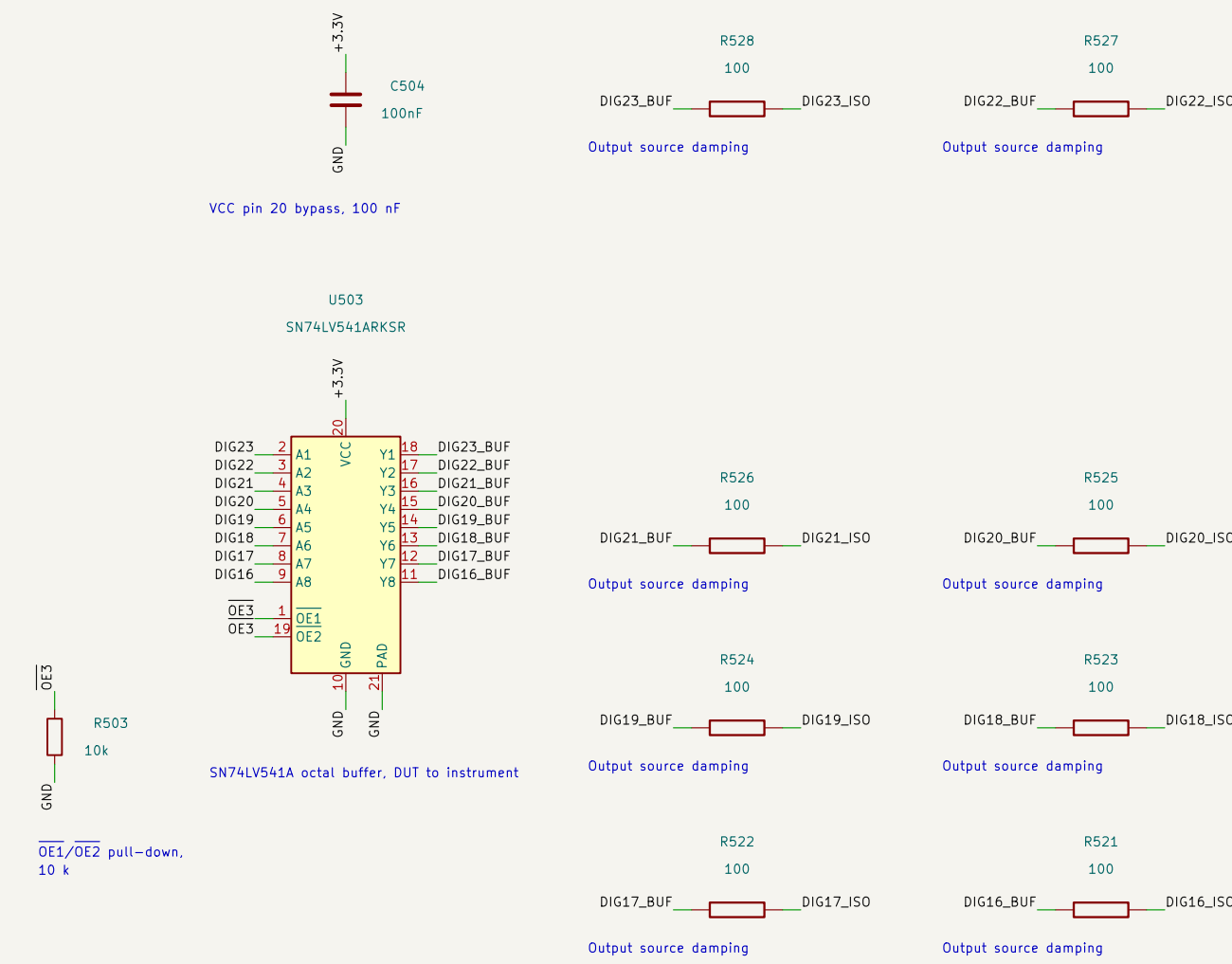
C501 (4.7 uF) holds the +3.3V rail where it enters the block; the per-package 100 nF bypasses are in the octet groups.



PLACE: Place C501 at the supply entry of the block, not at any one package.
ROUTE: +3.3V carries PWR_3V3_LOCAL from the entry to the four VCC pins; GND is PWR_RETURN_LOCAL.

3. Octet DIG16 to DIG23: U503

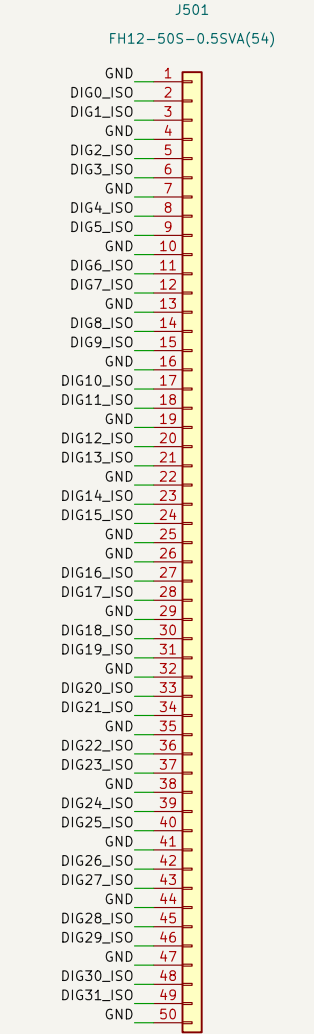
U503 buffers DIG16 to DIG23 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18); R521 to R528 (100 ohm) damp each output into its connector contact. C504 bypasses VCC (pin 20); R503 holds both enables (pins 1 and 19) low.



PLACE: Place C504 hard against pin 20 of U503 with a short return to pin 10 and the exposed pad 21; R503 near pins 1 and 19; the eight damping resistors between the Y pins and J501, outputs toward the connector.
ROUTE: The DIG16 to DIG23 inputs use this block's ports and escape toward the board on vias; keep the Y runs short to the resistors and the resistor-to-contact runs paired with the connector's ground contacts.

6. FFC receptacle

J501 carries the 32 damped outputs (DIGn_J50) on the contract's DUT contacts and the 18 grounds on one GND; the four mechanical lands carry no net.



50-contact FFC receptacle, top entry
PLACE: Vertical, top-entry receptacle at the board edge, latch away from the buffers; verify pin 1 and the contact face on the real part.
ROUTE: Pair each DIGn_J50 with its neighbouring ground contact and tie all 18 grounds into one GND copper under the connector; land pattern dual-row staggered at 1.0 mm within each row.

INTERFACES

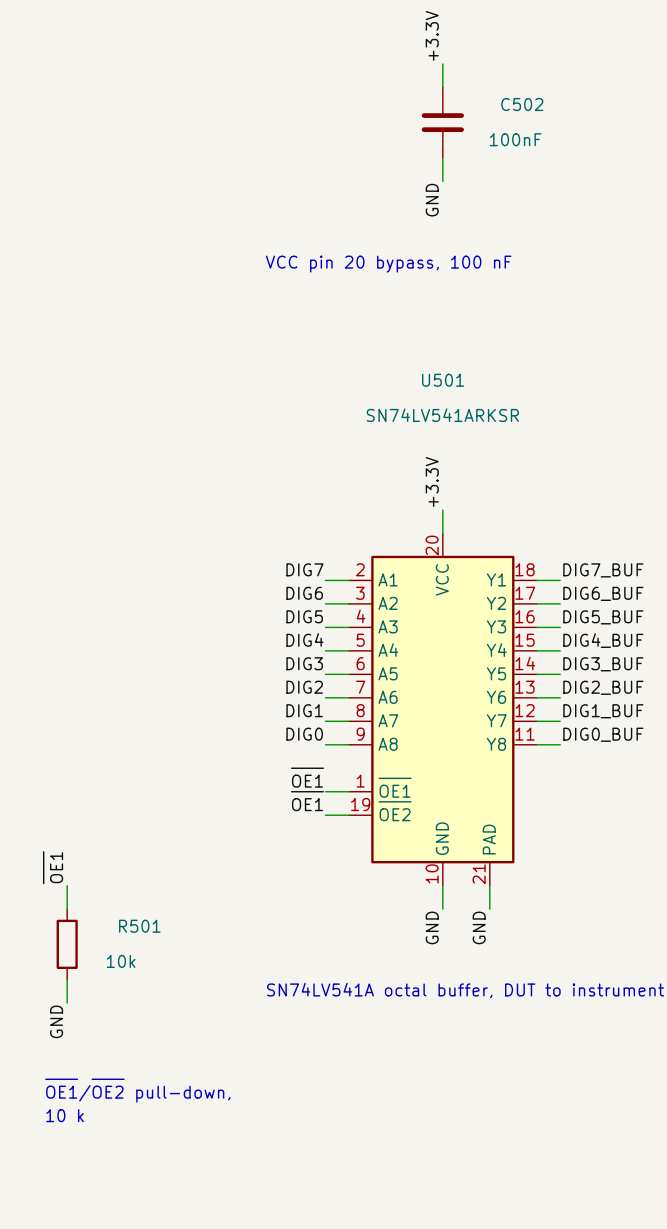
+3.3VDC--+3.3V
Always-on 3.3 V buffer supply (VCC pins 20); never reaches the cable.

18 connector grounds, buffer GND pins and pads, bypass and OE pull-down return.

DIG0--DIG0
Observation Input 0 into U501 A8 (pin 9); leaves on contact 2.
DIG1--DIG1
Observation Input 1 into U501 A7 (pin 8); leaves on contact 3.
DIG2--DIG2
Observation Input 2 into U501 A6 (pin 7); leaves on contact 5.
DIG3--DIG3
Observation Input 3 into U501 A5 (pin 6); leaves on contact 6.
DIG4--DIG4
Observation Input 4 into U501 A4 (pin 5); leaves on contact 8.
DIG5--DIG5
Observation Input 5 into U501 A3 (pin 4); leaves on contact 9.
DIG6--DIG6
Observation Input 6 into U501 A2 (pin 3); leaves on contact 11.
DIG7--DIG7
Observation Input 7 into U501 A1 (pin 2); leaves on contact 12.
DIG8--DIG8
Observation Input 8 into U502 A8 (pin 9); leaves on contact 14.
DIG9--DIG9
Observation Input 9 into U502 A7 (pin 8); leaves on contact 15.
DIG10--DIG10
Observation Input 10 into U502 A6 (pin 7); leaves on contact 17.
DIG11--DIG11
Observation Input 11 into U502 A5 (pin 6); leaves on contact 18.
DIG12--DIG12
Observation Input 12 into U502 A4 (pin 5); leaves on contact 20.
DIG13--DIG13
Observation Input 13 into U502 A3 (pin 4); leaves on contact 21.
DIG14--DIG14
Observation Input 14 into U502 A2 (pin 3); leaves on contact 23.
DIG15--DIG15
Observation Input 15 into U502 A1 (pin 2); leaves on contact 24.
DIG16--DIG16
Observation Input 16 into U503 A8 (pin 9); leaves on contact 27.
DIG17--DIG17
Observation Input 17 into U503 A7 (pin 8); leaves on contact 28.
DIG18--DIG18
Observation Input 18 into U503 A6 (pin 7); leaves on contact 30.
DIG19--DIG19
Observation Input 19 into U503 A5 (pin 6); leaves on contact 31.
DIG20--DIG20
Observation Input 20 into U503 A4 (pin 5); leaves on contact 33.
DIG21--DIG21
Observation Input 21 into U503 A3 (pin 4); leaves on contact 34.
DIG22--DIG22
Observation Input 22 into U503 A2 (pin 3); leaves on contact 36.
DIG23--DIG23
Observation Input 23 into U503 A1 (pin 2); leaves on contact 37.
DIG24--DIG24
Observation Input 24 into U504 A8 (pin 9); leaves on contact 39.
DIG25--DIG25
Observation Input 25 into U504 A7 (pin 8); leaves on contact 40.
DIG26--DIG26
Observation Input 26 into U504 A6 (pin 7); leaves on contact 42.
DIG27--DIG27
Observation Input 27 into U504 A5 (pin 6); leaves on contact 43.
DIG28--DIG28
Observation Input 28 into U504 A4 (pin 5); leaves on contact 45.
DIG29--DIG29
Observation Input 29 into U504 A3 (pin 4); leaves on contact 46.
DIG30--DIG30
Observation Input 30 into U504 A2 (pin 3); leaves on contact 48.
DIG31--DIG31
Observation Input 31 into U504 A1 (pin 2); leaves on contact 49.

1. Octet DIG0 to DIG7: U501

U501 buffers DIG0 to DIG7 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18); R505 to R512 (100 ohm) damp each output into its connector contact. C502 bypasses VCC (pin 20); R501 holds both enables (pins 1 and 19) low.

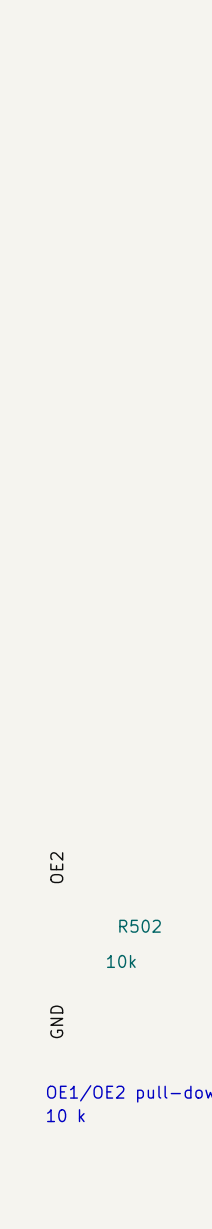


PLACE: Place C502 hard against pin 20 of U501 with a short return to pin 10 and the exposed pad 21; R501 near pins 1 and 19; the eight damping resistors between the Y pins and J501, outputs toward the connector.

ROUTE: The DIG0 to DIG7 inputs are this block's ports and escape toward the board on vias; keep the Y runs short to the resistors and the resistor-to-contact runs paired with the connector's ground contacts.

2. Octet DIG8 to DIG15: U502

U502 buffers DIG8 to DIG15 (inputs B8 to B1, pins 29 to 22) onto Y15 to Y8 (pins 31 to 24); R503 to R510 (100 ohm) damp each output into its connector contact. C503 bypasses VCC (pin 30); R501 holds both enables (pins 25 and 27) low.

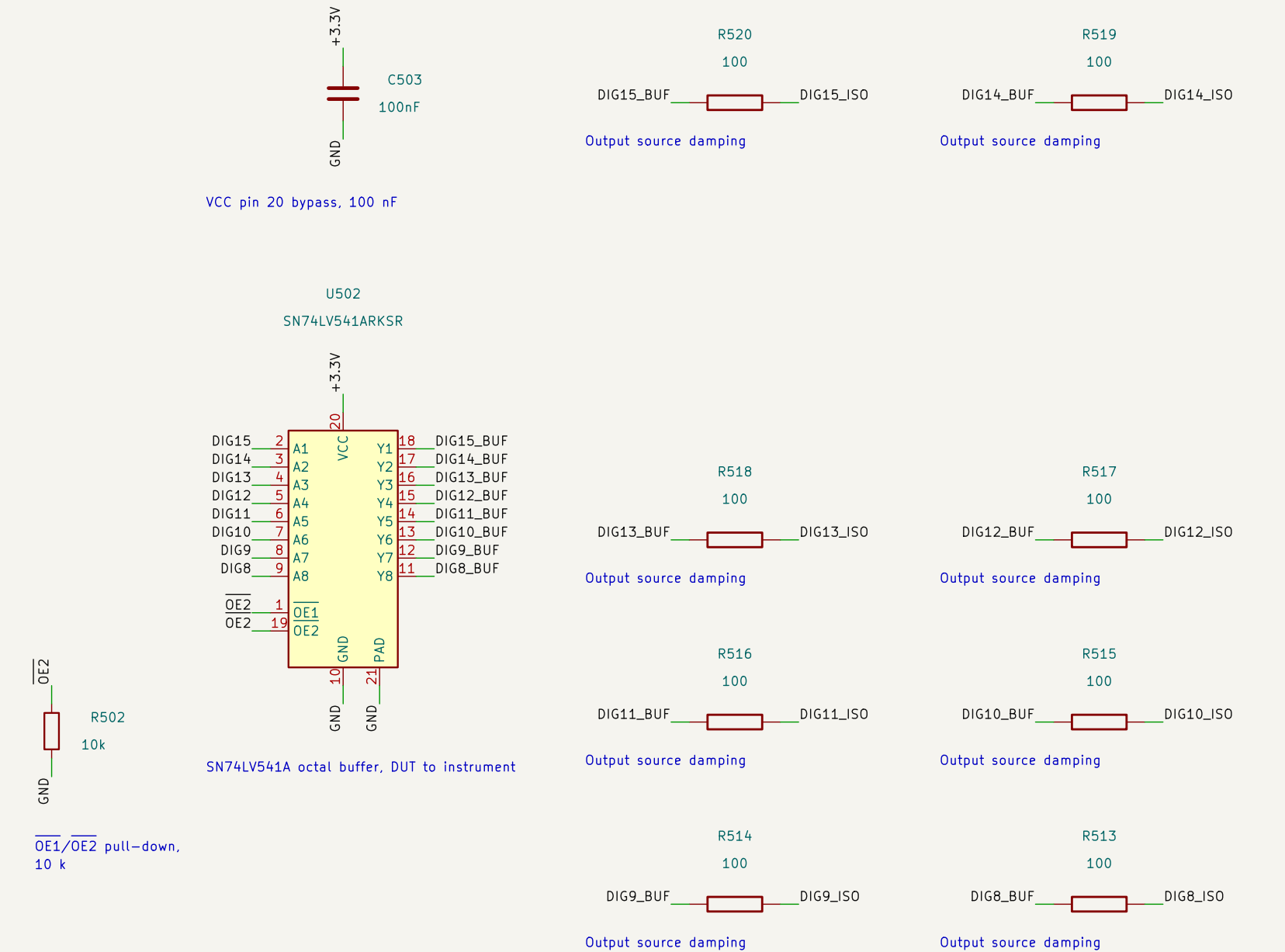


PLACE: Place C503 hard against pin 30 of U502 with a short return to pin 28 and the exposed pad 29; R501 near pins 25 and 27; the eight damping resistors between the Y pins and J501, outputs toward the connector.

ROUTE: The DIG8 to DIG15 inputs are this block's ports and escape toward the board on vias; keep the Y runs short to the resistors and the resistor-to-contact runs paired with the connector's ground contacts.

2. Octet DIG8 to DIG15: U502

U502 buffers DIG8 to DIG15 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18); R513 to R520 (100 ohm) damp each output into its connector contact. C503 bypasses VCC (pin 20); R502 bypasses VCC (pin 20); R502 holds both enables (pins 1 and 19) low.

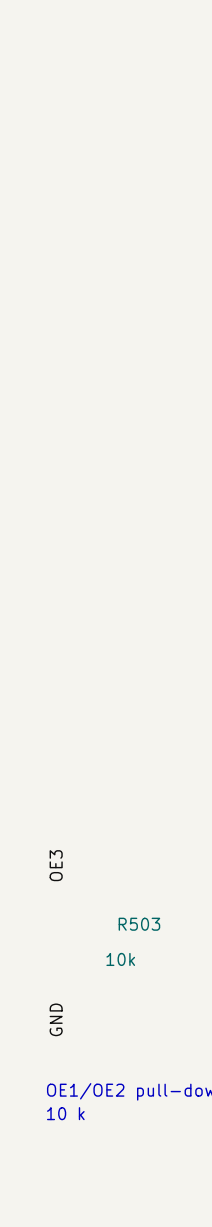


PLACE: Place C503 hard against pin 20 of U502 with a short return to pin 10 and the exposed pad 21; R502 near pins 1 and 19; the eight damping resistors between the Y pins and J501, outputs toward the connector.

ROUTE: The DIG8 to DIG15 inputs are this block's ports and escape toward the board on vias; keep the Y runs short to the resistors and the resistor-to-contact runs paired with the connector's ground contacts.

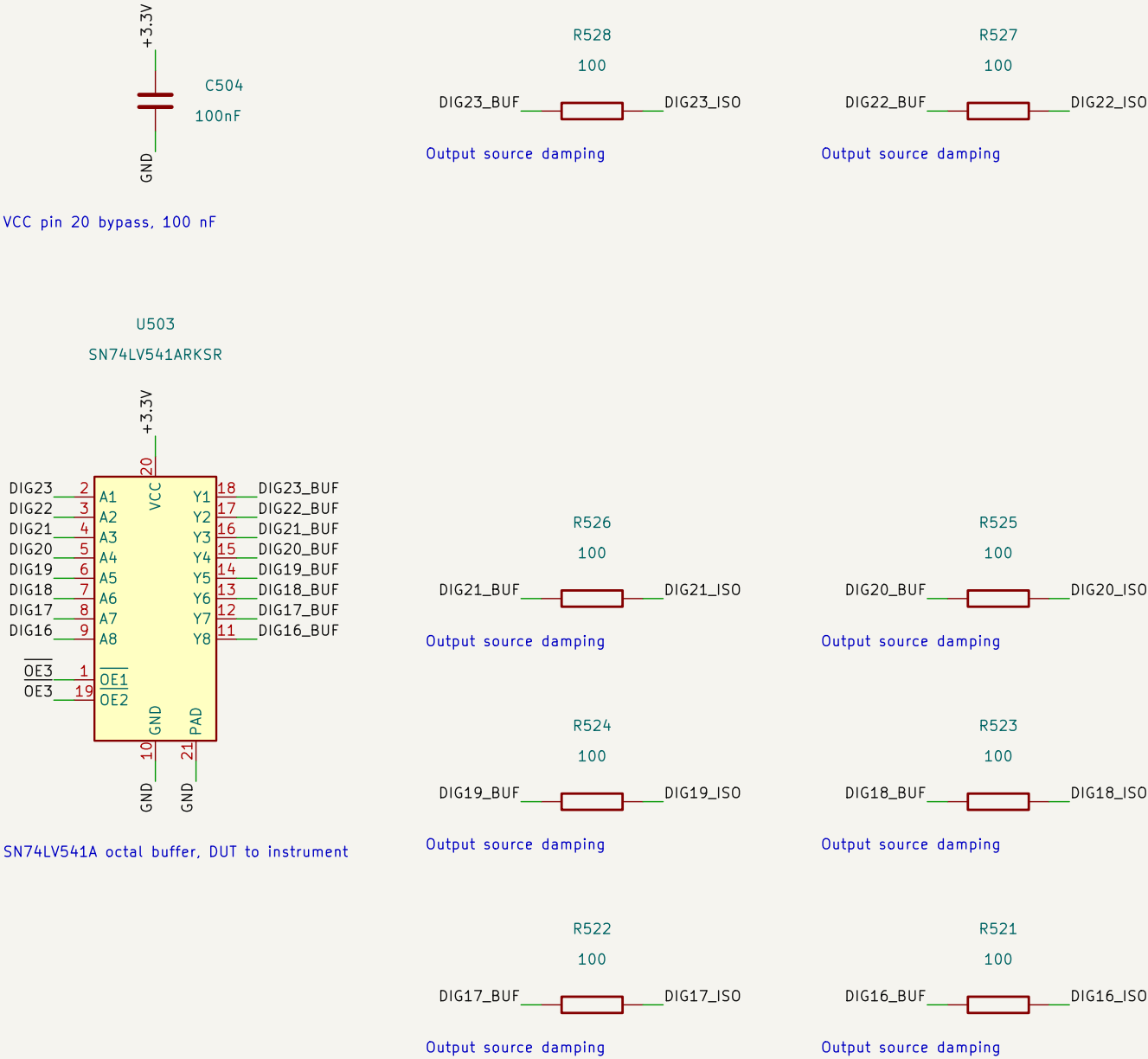
3. Octet DIG16 to

U503 buffers DIG16 to
C504 bypasses VCC (pin



3. Octet DIG16 to DIG23: U503

U503 buffers DIG16 to DIG23 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18); R521 to R528 (100 ohm) damp each output into its connector contact. C504 bypasses VCC (pin 20); R503 holds both enables (pins 1 and 19) low.

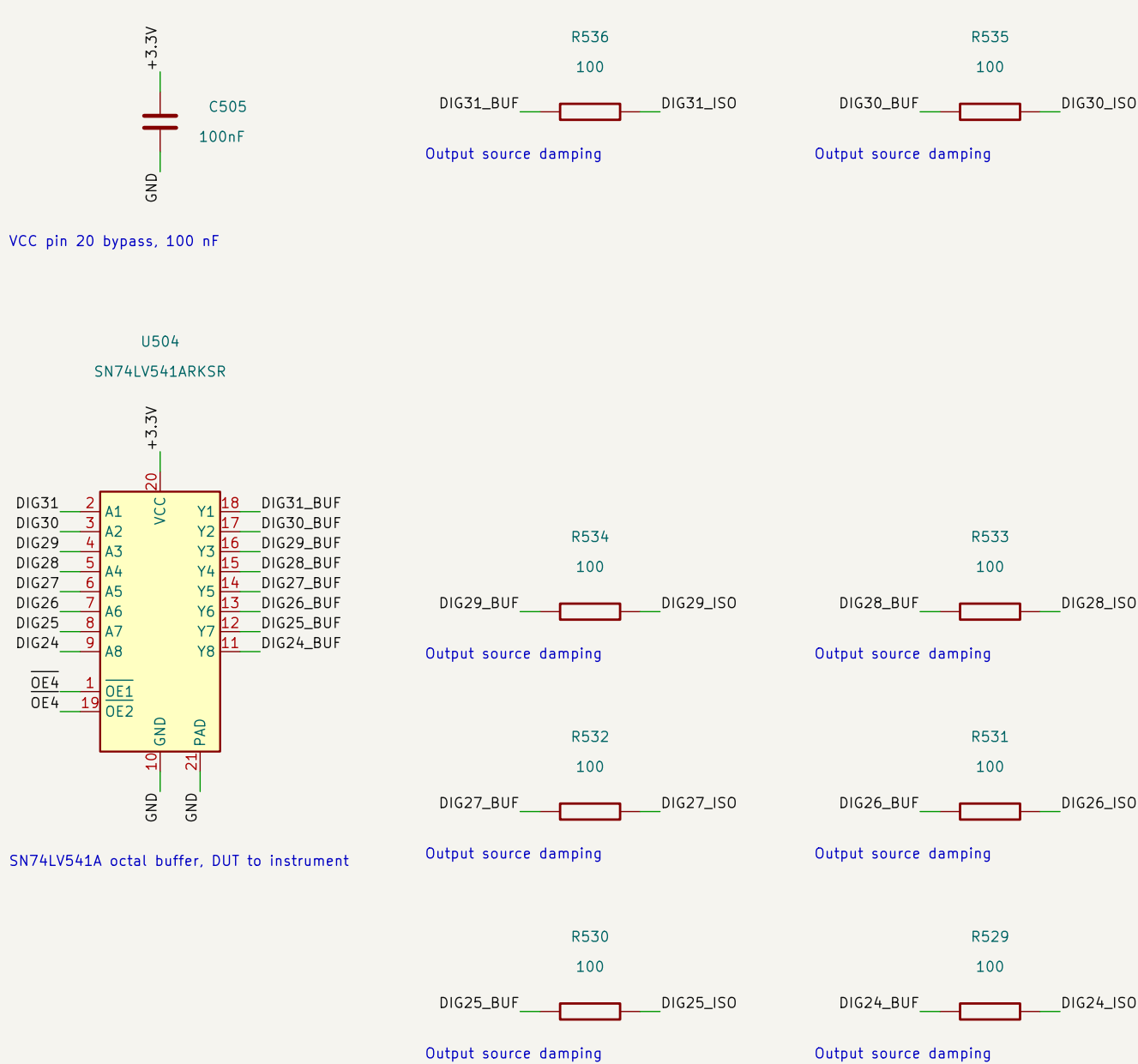


PLACE: Place C504 hard against pin 20 of U503 with a short return to pin 10 and the exposed pad 21; R503 near pins 1 and 19; the eight damping resistors between the Y pins and J501, outputs toward the connector.

ROUTE: The DIG16 to DIG23 inputs are this block's ports and escape toward the board on vias; keep the Y runs short to the resistors and the resistor-to-contact runs paired with the connector's ground contacts.

4. Octet DIG24 to DIG31: U504

U504 buffers DIG24 to DIG31 (inputs A8 to A1, pins 9 to 2) onto Y8 to Y1 (pins 11 to 18); R529 to R536 (100 ohm) damp each output into its connector contact. C505 bypasses VCC (pin 20); R504 holds both enables (pins 1 and 19) low.



PLACE: Place C505 hard against pin 20 of U504 with a short return to pin 10 and the exposed pad 21; R504 near pins 1 and 19; the eight damping resistors between the Y pins and J501, outputs toward the connector.

ROUTE: The DIG24 to DIG31 inputs are this block's ports and escape toward the board on vias; keep the Y runs short to the resistors and the resistor-to-contact runs paired with the connector's ground contacts.

5. Rail-entry bulk b

C501 (4.7 uF) holds the



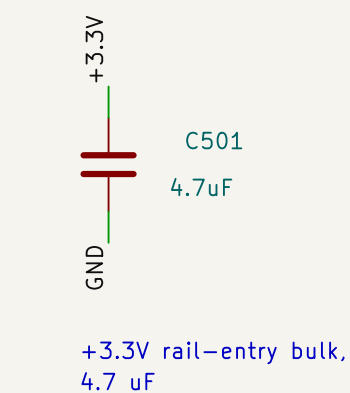
PLACE: Place C501 at the

ROUTE: +3.3V carries PW



5. Rail-entry bulk bypass

C501 (4.7 uF) holds the +3.3V rail where it enters the block; the per-package 100 nF bypasses are in the octet groups.

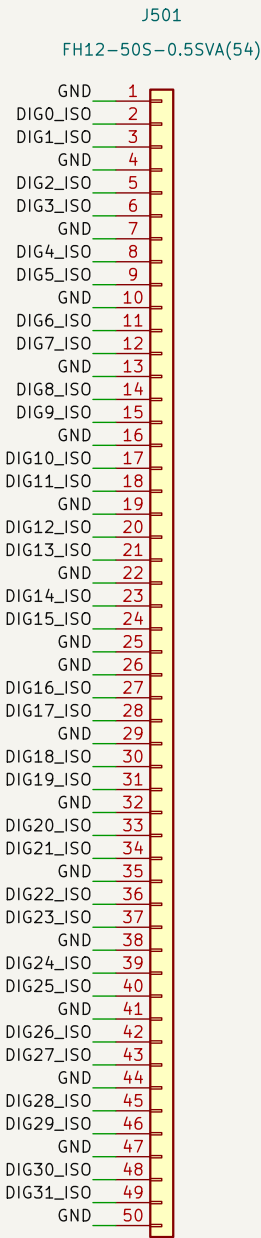


PLACE: Place C501 at the supply entry of the block, not at any one package.

ROUTE: +3.3V carries PWR_3V3_LOCAL from the entry to the four VCC pins; GND is PWR_RETURN_LOCAL.

6. FFC receptacle

J501 carries the 32 damped outputs (DIGn_ISO) on the contract’s DUT contacts and the 18 grounds on one GND; the four mechanical lands carry no net.



50–contact FFC receptacle, top entry

PLACE: Vertical, top–entry receptacle at the board edge, latch away from the buffers; verify pin 1 and the contact face on the real part.

ROUTE: Pair each DIGn_ISO with its neighbouring ground contact and tie all 18 grounds into one GND copper under the connector; land pattern dual–row staggered at 1.0 mm within each row.

Observation input 13 into U50

DIG14 DIG14

Observation input 14 into U50

DIG15 DIG15

Observation input 15 into U50

DIG16 DIG16

Observation input 16 into U50

DIG17 DIG17

Observation input 17 into U50

DIG18 DIG18

Observation input 18 into U50

DIG19 DIG19

Observation input 19 into U50

DIG20 DIG20

Observation input 20 into U50

DIG21 DIG21

Observation input 21 into U50

DIG22 DIG22

Observation input 22 into U50

DIG23 DIG23

Observation input 23 into U50

DIG24 DIG24

Observation input 24 into U50

DIG25 DIG25

Observation input 25 into U50

DIG26 DIG26

Observation input 26 into U50

DIG27 DIG27

Observation input 27 into U50

INTERFACES

+3.3V  +3.3V

Always-on 3.3 V buffer supply (VCC pins 20); never reaches the cable.

GND  GND

18 connector grounds, buffer GND pins and pads, bypass and OE pull-down return.

DIG0  DIG0

Observation input 0 into U501 A8 (pin 9); leaves on contact 2.

DIG1  DIG1

Observation input 1 into U501 A7 (pin 8); leaves on contact 3.

DIG2  DIG2

Observation input 2 into U501 A6 (pin 7); leaves on contact 5.

DIG3  DIG3

Observation input 3 into U501 A5 (pin 6); leaves on contact 6.

DIG4  DIG4

Observation input 4 into U501 A4 (pin 5); leaves on contact 8.

DIG5  DIG5

Observation input 5 into U501 A3 (pin 4); leaves on contact 9.

DIG6  DIG6

Observation input 6 into U501 A2 (pin 3); leaves on contact 11.

DIG7  DIG7

Observation input 7 into U501 A1 (pin 2); leaves on contact 12.

DIG8  DIG8

Observation input 8 into U502 A8 (pin 9); leaves on contact 14.

DIG9  DIG9

Observation input 9 into U502 A7 (pin 8); leaves on contact 15.

DIG10  DIG10

Observation input 10 into U502 A6 (pin 7); leaves on contact 17.

DIG11  DIG11

Observation input 11 into U502 A5 (pin 6); leaves on contact 18.

DIG12  DIG12

Observation input 12 into U502 A4 (pin 5); leaves on contact 20.

DIG13  DIG13

Observation input 13 into U502 A3 (pin 4); leaves on contact 21.

DIG14  DIG14

Observation input 14 into U502 A2 (pin 3); leaves on contact 23.

DIG15  DIG15

Observation input 15 into U502 A1 (pin 2); leaves on contact 24.

DIG16  DIG16

Observation input 16 into U503 A8 (pin 9); leaves on contact 27.

DIG17  DIG17

Observation input 17 into U503 A7 (pin 8); leaves on contact 28.

DIG18  DIG18

Observation input 18 into U503 A6 (pin 7); leaves on contact 30.

DIG19  DIG19

Observation input 19 into U503 A5 (pin 6); leaves on contact 31.

DIG20  DIG20

Observation input 20 into U503 A4 (pin 5); leaves on contact 33.

DIG21  DIG21

Observation input 21 into U503 A3 (pin 4); leaves on contact 34.

DIG22  DIG22

Observation input 22 into U503 A2 (pin 3); leaves on contact 36.

DIG23  DIG23

Observation input 23 into U503 A1 (pin 2); leaves on contact 37.

DIG24  DIG24

Observation input 24 into U504 A8 (pin 9); leaves on contact 39.

DIG25  DIG25

Observation input 25 into U504 A7 (pin 8); leaves on contact 40.

DIG26  DIG26

Observation input 26 into U504 A6 (pin 7); leaves on contact 42.

DIG27  DIG27

Observation input 27 into U504 A5 (pin 6); leaves on contact 43.

DIG28  DIG28

Observation input 28 into U504 A4 (pin 5); leaves on contact 45.

DIG29  DIG29

Observation input 29 into U504 A3 (pin 4); leaves on contact 46.

DIG30  DIG30

Observation input 30 into U504 A2 (pin 3); leaves on contact 48.

DIG31  DIG31

Observation input 31 into U504 A1 (pin 2); leaves on contact 49.

OPERATION

DUT side of the InstrumentPort-Digital-50 profile (board-interfaces docs/instrument-port-digital.md, draft v0.1). Direction is a hardware property, DUT to instrument only: DIGn enters U501 to U504 (DIG0 to 7, 8 to 15, 16 to 23, 24 to 31, each octet one package, A8 down to A1), leaves on Y8 to Y1 through 100 ohm damping (R505 to R536) onto J501. The cable carries no supply, reference, enable or stimulus.

Pin mapping is the contract's DUT table and is not mirrored: channel n lands on contact 2 + n + floor(n/2) + floor(n/16), DIG0 on contact 2, DIG31 on contact 49, the 18 grounds on 1, 4, 7, ... 47, 50 with the 25/26 double ground at the bank boundary. The mirror lives on instrument_port_digital_50_adapter_ffc_boundary_vertical; mirroring both ends cancels, and ERC and DRC cannot see it.

Enabled by hardware default, no disable at all: both active-low enables of each package share one net held low by its 10 k pull-down (R501 to R504; at most about 0.1 V from the two inputs' leakage against the 0.99 V VIL), so observation works with the MCU in reset or unprogrammed. The contract permits this since 2026-09-15; do not re-add a control as a fix.

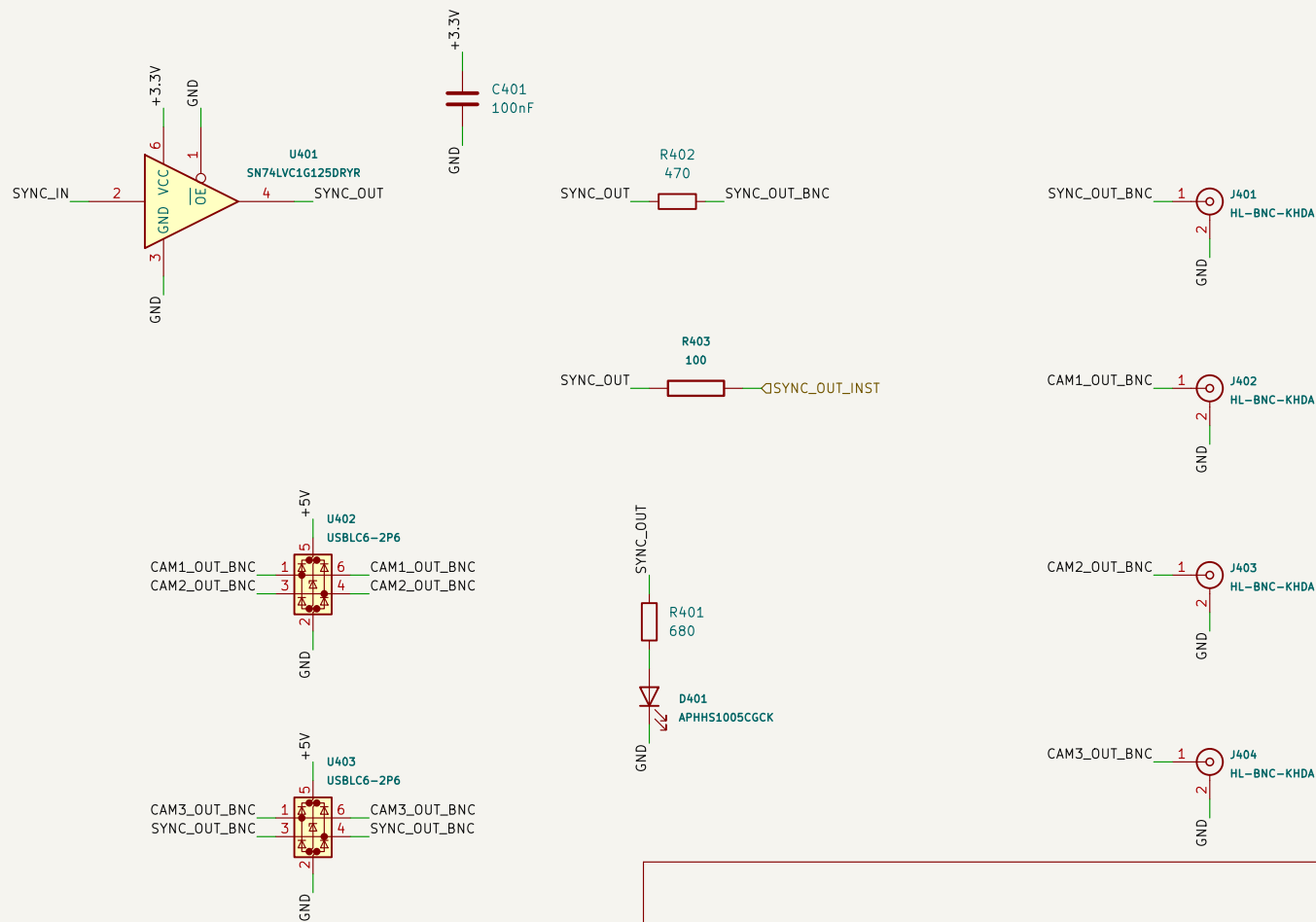
Supply: the always-on 3.3 V rail on VCC (pins 20); SN74LV541A runs 2 to 5.5 V, drives +/-8 mA at 3.3 V, inputs tolerate 0 to 5.5 V with Ioff <= 5 uA unpowered, VIH 2.31 V, VIL 0.99 V, edges <= 100 ns/V, not a Schmitt input. C502 to C505 (100 nF) bypass each pin 20; C501 (4.7 uF, X5R 0402, well below nameplate at 3.3 V bias) is the one rail-entry bulk, not a fifth per-package bypass.

The 100 ohm damping bounds a hard short of one output to GND at 33 mA, inside the +/-35 mA per-output absolute maximum, and damps edges into the cable; it is not short-circuit protection. Input bias is board-specific and not in this block: every unused DIGn must be tied at the board. Attach and remove the FFC with target power off; J501 is rated 20 mating cycles, so break the link at the instrument end.

DESIGN CONTRACT

DUT-side InstrumentPort-Digital-50 with integrated read-only buffering, on a VERTICAL, top-entry 50-contact ZIF connector: Hirose FH12-50S-0.5SVA(54), OW-CONN-FH12-50S-0-5SVA-54, LCSC C597991, 0.5mm pitch, symbol Conn_01x50, footprint orb_weaver_connectors:Hirose_FH12-50S-0.5SVA_1x50-4MP_P0.5mm_Vertical; the four mechanical lands are unnumbered pads and carry no net. Thirty-two channels through four SN74LV541ARKSR octal buffers (OW-MISC-SN74LV541ARKSR, C7364695, symbol orb_weaver_misc:SN74LV541ARKSR, footprint orb_weaver_smd:Texas_RKS0020A_VQFN-20-1EP_2.5x4.5mm_P0.5mm_EP1x3mm, exposed pad 21 to GND), grouped DIG0-7 / DIG8-15 / DIG16-23 / DIG24-31 to match the 13-contact octet windows. The 541 is flow-through: input pin p pairs with output pin 20-p, A1(2) to Y1(18) through A8(9) to Y8(11). DIRECTION IS A HARDWARE PROPERTY: DUT to instrument only. The cable carries no supply, no voltage reference, no enable and no stimulus, and nothing in this block may be driven by the instrument. PIN MAPPING IS THE CONTRACT'S DUT TABLE AND IS NOT MIRRORRED: channel n lands on pin 2 + n + floor(n/2) + floor(n/16), so DIG0 is pin 2 and DIG31 is pin 49, with all 18 grounds on pins 1, 4, 7, 10, 13, 16, 19, 22, 25, 26, 29, 32, 35, 38, 41, 44, 47 and 50. THE MIRROR LIVES ON THE ADAPTER, NOT HERE. instrument_port_digital_50_adapter_ffc_boundary_vertical is pre-mirrored to 51-n so that the expected reversing assembly - same-side Type A FFC with a vertical FH12 at both ends, connectors rotated 180 degrees - delivers DIGn to DIGn. Mirroring both ends cancels and channels arrive as DIG31-n. The ground pattern is palindromic under 51-n, so a mirrored map lands every ground identically and every net stays driven and terminated: ERC, DRC and design_block_tools.py check are ALL BLIND to this error, and only a pin-by-pin netlist comparison or continuity on the real cable catches it. Per-output source damping is 100 ohms, OW-PASS-0402WGF1000TCE. That value is chosen as the smallest standard one that bounds a hard short to ground inside the LV541A's +/-35mA output absolute maximum even crediting the driver with zero impedance (3.3V/100R = 33mA); 68R gives 49mA, 47R gives 70mA, and the legacy 33R gives 100mA. It is NOT short-circuit protection and does not cover every fault. DEFAULT-ENABLED BY HARDWARE, AND THERE IS NO DISABLE AT ALL: both active-low OE inputs of each package share one net held low by a single 10k pull-down - R501 through R504, one per package - so observation works with the MCU held in reset, unprogrammed or unable to boot, and the port cannot be muted without desoldering. There is no manual jumper, no firmware link and no OE port. The owning contract was relaxed on 2026-09-15 from requiring manual disabling to permitting none, so this conforms; the reasoning and the retained future option are in kicad-libs/docs/digital-instrument-port-design-blocks.md under 'No disable control, and why'. DO NOT re-add a control as an oversight fix. Shared 10k is verified against aggregate leakage: 2 x 5uA max gives 0.1V against a 0.99V VIL. If a noise investigation ever needs a mute, detaching the FFC bounds the cable's contribution but NOT the buffers', which keep switching into their board-side traces and damping resistors; lift the 100R resistors on the suspect channels instead. SUPPLY FROM THE BOARD'S ALWAYS-ON 3.3V RAIL, independent of firmware, HV_EN and every switched domain; a buffer on a switched rail cannot observe the domain it is powering down with. DECOUPLING is one 100nF per package, C502 through C505, hard against each pin 20 with a short return, plus one 4.7uF rail-entry bulk, C501 / OW-CAP-4U7-0402-X5R-16V, at the supply entry. C501 is NOT a fifth per-IC bypass - do not 'fix' its distance to any package. Simultaneous-switching budget: 32 x 50pF x 3.3V = 5.3nC per all-channel edge, about 1mV of droop against the combined local reservoir. Expect meaningfully less than 4.7uF at 3.3V bias - a 4.7uF X5R in an 0402 derates hard - so treat the nameplate value as nominal, not measured. INPUT BIAS IS BOARD-SPECIFIC AND IS NOT IN THIS BLOCK: there is no universal pull-down, because SPI selects, open-drain buses and switched-domain taps each need different bias, and pulls that must read HIGH on a switched net reference the switched rail, never the always-on one. Every unused input must be explicitly tied at the board. LV541A at 3.3V needs VIH >= 2.31V and VIL <= 0.99V with transitions <= 100 ns/V; it is 0-5.5V input tolerant with 2pF typical input capacitance and Ioff <= 5uA at VCC=0. It is NOT Schmitt-triggered and NOT a comparator: do not route a raw analog node through it for a timing witness, and do not treat a clean legacy LVC125A capture as LV541A qualification. OE would disable outputs only - it never removes input loading or makes a floating input acceptable, which is part of why no mute was fitted. Requires straight-ended 0.30 +/-0.05mm FFC with gold contacts, at least 2mm exposed contact and 3mm reinforcement; retention-eared cable is NOT qualified for this connector. Rated 20 mating cycles, so prefer breaking the link at the instrument end, and attach or remove the cable with target power off unless the actual assembly is hot-plug qualified. Profile is InstrumentPort-Digital-50 draft v0.1, UNQUALIFIED: no measured rate, delay, skew, loading or power-state limit has been established. Marker/beacon channel indices are NOT frozen, with DIG0/DIG1 the current recommendation over the earlier DIG14/DIG15. Pairs with instrument_port_digital_50_adapter_ffc_boundary_vertical; the analyzer-specific channel map belongs to la5032_connector_boundary, not here. GROUNDED INPUTS ARE THE BOARD'S COPPER: the inputs are this block's ports, so a board that grounds unused DIGn channels draws one 0.20 mm track per grounded LV541A pad column straight into that package's thermal pad on F.Cu, before autorouting; Freerouting will not run a track along a row of same-net 0.5 mm-pitch pads and left those groups unrouted on every camera-board run (layout conventions 11a). Since 2026-09-29 every DIGn also ends at its own escape via above the pad row, so a board may instead tie an unused channel to ground at that via; either way the grounding copper is the board's, never the block's. FLOOR COPPER IS DECLARED: the 0.10 mm gaps between the 32 damping resistors and the LV541A pins (2026-09-26) and between each DIGn escape stub and the escape via beside it (2026-09-29) are wrapped in BLOCK_FLOOR rule areas, so a consuming board sees no clearance findings from this block under the shared rules; a board wanting 0.20 mm inside the block re-routes the block, not the rule (layout conventions 12).

+5V □ +5V
+3.3V □ +3.3V
GND □ GND
SYNC_IN □ SYNC_IN
CAM1_OUT_BNC □ CAM1_OUT_BNC
CAM2_OUT_BNC □ CAM2_OUT_BNC
CAM3_OUT_BNC □ CAM3_OUT_BNC



Janelia Research Campus

Sheet: /outputs/

File: outputs.kicad_sch

Title: camera-gpio-interface-pcb

Size: A4

Date: 2026-09-26

Rev: 1.0

KiCad E.D.A. 10.0.6

Id: 4/11

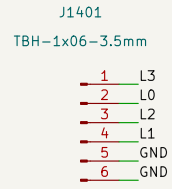
Blackfly S GPIO channel | trigger in, sync in, exposure out, five taps; vertical or horizontal header

One FLIR Blackfly S camera GPIO channel (trigger, sync, exposure output, instrument taps) on a 6-position 3.5 mm Phoenix header; the connector family pilot: the vertical MCV and the horizontal MC header are pad-identical, so one source publishes both orientations

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Camera header

J701, the 6-position 3.5 mm Phoenix header; pins 1 to 4 are Lines 3, 0, 2 and 1, pins 5 and 6 are the camera's two grounds.

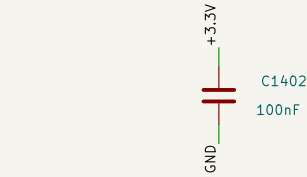


Camera GPIO header, 6-pos
3.5 mm

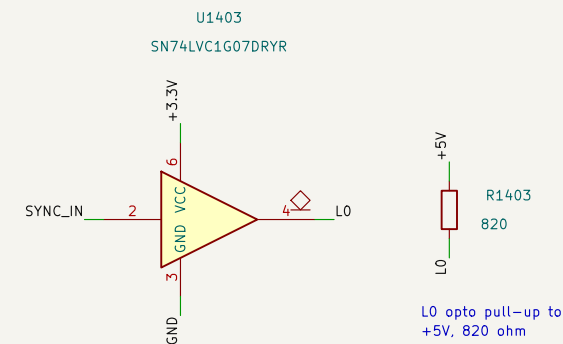
PLACE: Place J701 at the board edge the plug needs; the vertical body takes the plug from above, the horizontal from its +Y side; the anchor is the pad-array centre for both.
ROUTE: L3, L0, L2 and L1 run straight from the pads to their clamps and parts; GND from pins 5 and 6 into the block's return.

3. Line 0 sync drive

U703's open-drain Y pulls L0 low; R703 (820 ohm) returns it to +5V, the opto input's drive level; C702 bypasses U703's VCC.



VCC pin 6 bypass, U703

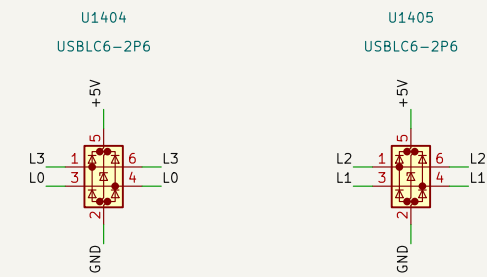


Line 0 sync driver, open drain

PLACE: Place U703 near J701 pin 2 with C702 at its pin 6; R703 from L0 to the +5V entry.
ROUTE: L0 carries about 6 mA pulses into the camera's opto input; keep its return with the trigger line.

5. ESD clamps

U704 clamps L3 and L0, U705 clamps L2 and L1, both referenced to +5V and GND; each pair's two I/O pins are tied to the node.



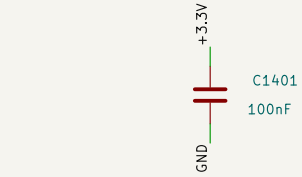
ESD array for L3/L0

ESD array for L2/L1

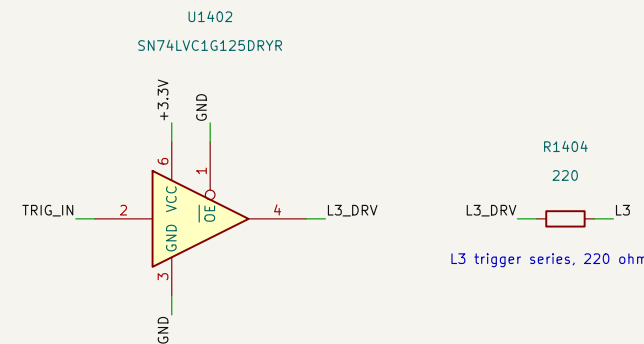
PLACE: Place both arrays right at J701's pads, before any series part, with the shortest GND return.
ROUTE: Wire the paired I/O pads together on the node itself; no separate track between them.

2. Line 3 trigger drive

U702 (always enabled) drives L3_DRV; R704 (220 ohm) in series feeds camera Line 3 on L3; C701 bypasses U702's VCC.



VCC pin 6 bypass, U702

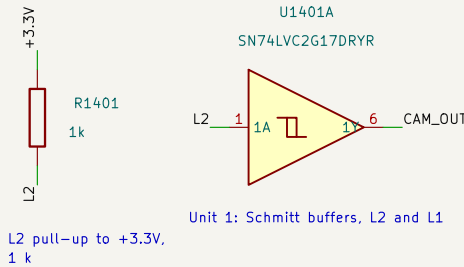


Line 3 trigger driver, always enabled

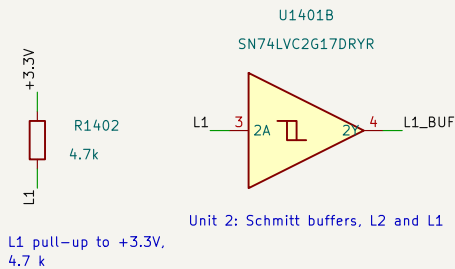
PLACE: Place U702 near J701 pin 1 with C701 at its pin 6 and a short return to pin 3; R704 between the driver and the connector.
ROUTE: L3 is a 3.3 V edge-triggered line; short, over ground, away from the switching parts of the board.

4. Exposure output, BNC drive and LED

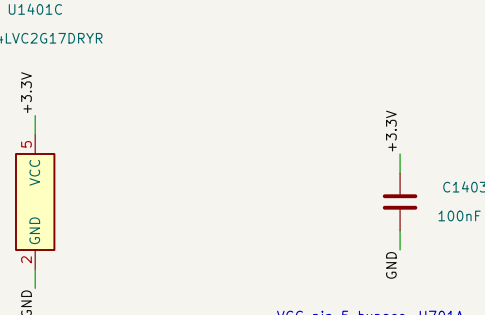
R701 pulls Line 2 up, U701A gate 1 squares it into CAM_OUT; R705 drives the BNC, R706 lights D701; R702 pulls Line 1 up and gate 2 buffers it into L1_BUF; C703 bypasses U701A.



L2 pull-up to +3.3V,
1 k



L1 pull-up to +3.3V,
4.7 k



Power unit

PLACE: Place U701A between the connector and the BNC side with C703 at its pin 5; R701 and R702 at the connector pads; D701 where it is visible.
ROUTE: CAM_OUT is the board's exposure reference; route R705's far end to the BNC with a ground return beside it.

INTERFACES

+5V — +5V
Must be a 5 V rail; the Line 0 opto drive level (R703) and both ESD clamps' VBUS reference.

+3.3V — +3.3V
Logic rail for U701A, U702, U703 and the L2/L1 pull-ups; always-on if the taps must read before firmware.

GND — GND
Camera pins 5 (opto ground) and 6 (ground) both land here, with the logic and ESD returns.

TRIG_IN — TRIG_IN
Conditioned 3.3 V frame trigger from the board's input Schmitt into U702 (pin 2).

SYNC_IN — SYNC_IN
Conditioned 3.3 V Rsync from the board's input Schmitt into U703 (pin 2).

CAM_OUT_BNC — CAM_OUT_BNC
Exposure-active output; CAM_OUT through R705 (470 ohm); the BNC itself is the board's.

L0_INST — L0_INST
100 ohm tap (R707) on L0, camera Line 0 OPTOIN; the sync drive.

L1_INST — L1_INST
100 ohm tap (R708) on L1_BUF, camera Line 1 OPTOOUT after the Schmitt buffer.

L2_INST — L2_INST
100 ohm tap (R709) on L2, camera Line 2, the open-drain exposure output.

L3_INST — L3_INST
100 ohm tap (R710) on L3, camera Line 3, the frame trigger.

OUT_INST — OUT_INST
100 ohm tap (R711) on CAM_OUT, the buffered exposure signal.

INTERNAL NETS

CAM_OUT: Buffered Line 2 (exposure active) from U701A 1Y; drives the BNC resistor, the LED resistor and the OUT tap.

L0: Camera pin 2, Line 0 OPTOIN; open-drain U703 Y, pulled to +5V by R703 (820 ohm), clamped by U704.

L1: Camera pin 4, Line 1 OPTOOUT, pulled up to +3.3V by R702 (4.7 k), into Schmitt 2A, clamped by U705.

L1_BUF: Schmitt 2Y; buffered Line 1 for the L1_INST tap.

L2: Camera pin 3, Line 2 as open-drain exposure output, pulled up by R701 (1 k), into Schmitt 1A, clamped by U705.

L3: Camera pin 1, Line 3 GPI trigger, driven by U702 through R704 (220 ohm), clamped by U704.

L3_DRV: U702 Y, the trigger drive before the 220 ohm series resistor.

LED_A: LED anode; R706 (680 ohm) from CAM_OUT, so D701 lights while exposure is active.

OPERATION

Camera side: J701's terminal numbers are the camera's Hirose HR10A-7R-6PB pin numbers, wired with the FLIR 1 m flying-lead GPIO cable into a Phoenix MC 1.5/6-ST-3.5 plug; pin 1 green Line 3 (GPI, trigger), pin 2 black Line 0 (OPTOIN, sync), pin 3 red Line 2 (GPIO, exposure output), pin 4 white Line 1 (OPTOOUT), pin 5 blue opto ground and pin 6 brown ground, both on GND (common-ground wiring).

Trigger path: TRIG_IN -> U702 (SN74LVC1G125, OE pin 1 grounded, so always enabled) -> L3_DRV -> R704 (220 ohm) -> L3 -> camera Line 3; camera settings TriggerSelector FrameStart, TriggerSource Line3 RisingEdge. Sync path: SYNC_IN -> U703 (SN74LVC1G07 open drain) -> L0, pulled to +5V by R703 (820 ohm); 5 V across 820 ohm is about 6 mA, less by the opto input's forward drop. Both drivers run from +3.3V with 5.5 V-tolerant I/O.

Exposure output: camera Line 2 (LineMode Output, LineSource ExposureActive, V3.3Enable false, so open drain) is pulled up by R701 (1 k) to +3.3V and squared by Schmitt U701A 1A -> 1Y = CAM_OUT, which drives the BNC through R705 (470 ohm), the green LED D701 through R706 (680 ohm; about (3.3 - 2.1) / 680 = 1.8 mA, LED on while exposure is active) and the OUT_INST tap. Line 1 (OPTOOUT, LineSource Off) is pulled up by R702 (4.7 k) and buffered 2A -> 2Y into L1_BUF for its tap.

ESD: two USBLC6-2P6 arrays with VBUS on +5V clamp L3 and L0 (U704) and L2 and L1 (U705), 15 kV IEC 61000-4-2 level 4, at most 3.5 pF per line; both I/O pins of each pair are wired to the node, so the footprint's paired pads need no track between them. +5V must therefore be a 5 V rail: it is the clamp reference and the opto drive level, and feeds nothing else.

Variants (family.json): mcv6_vertical fits J701 = OW-CONN-TBH-1X06-3P5-VERT (Phoenix MCV 1.5/6-G-3.5, top entry); mc6_horizontal fits OW-CONN-1844252 (Phoenix MC 1.5/6-G-3.5, side entry toward the footprint's +Y). The two footprints are pad-identical (six 1.8 x 3.6 mm ovals on 3.5 mm, origin at the pad-array centre), so the variant swaps only the connector's body, courtyard and 3D model; every pad, track and via stays, and the anchor connector_center is the same point for both.

The placing board provides +3.3V (bind it to the always-on rail when the taps must be observable before firmware runs), a 5 V rail on +5V, the BNC on CAM_OUT_BNC, the conditioned 3.3 V TRIG_IN and SYNC_IN, and the instrument port behind the five 100 ohm taps; the three pull-ups are inside because the block owns L0, L1 and L2 (layout convention 10). Place one block per camera; the horizontal variant's plug needs the board edge its wire exit faces.

DESIGN CONTRACT

One FLIR Blackfly S camera GPIO channel (trigger, sync, exposure output, instrument taps) on a 6-position 3.5 mm Phoenix header; the connector family pilot: the vertical MCV and the horizontal MC header are pad-identical, so one source publishes both orientations

Circuit and PCB layout guidance
Migrated from the saved family core; circuit, variants and PCB unchanged

Orb Weaver

Sheet: /blackfly_s_gpio_channel_mcv6_vertical2/
File: blackfly_s_gpio_channel_mcv6_vertical.kicad_sch

Title: **Blackfly S GPIO channel family**

Size: A2	Date: 2026-10-04	Rev: Source migration 1
KiCad E.D.A. 10.0.6		Id: 14/11

1

2

3

4

Blackfly S GPIO channel | trigger in, sync in, exposure out, five taps; vertical or horizontal header

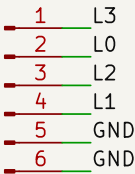
One FLIR Blackfly S camera GPIO channel (trigger, sync, exposure output, instrument taps) on a 6–position 3.5 mm Phoenix header; the connector family pilot: the vertical body. Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Camera header

J701, the 6–position 3.5 mm Phoenix header; pins 1 to 4 are Lines 3, 0, 2 and 1, pins 5 and 6 are the camera’s two grounds.

J1401

TBH–1x06–3.5mm



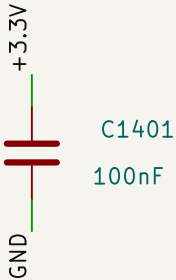
Camera GPIO header, 6–pos
3.5 mm

PLACE: Place J701 at the board edge the plug needs: the vertical body takes the plug from above, the horizontal from its +Y side; the anchor is the pad–array centre for both.

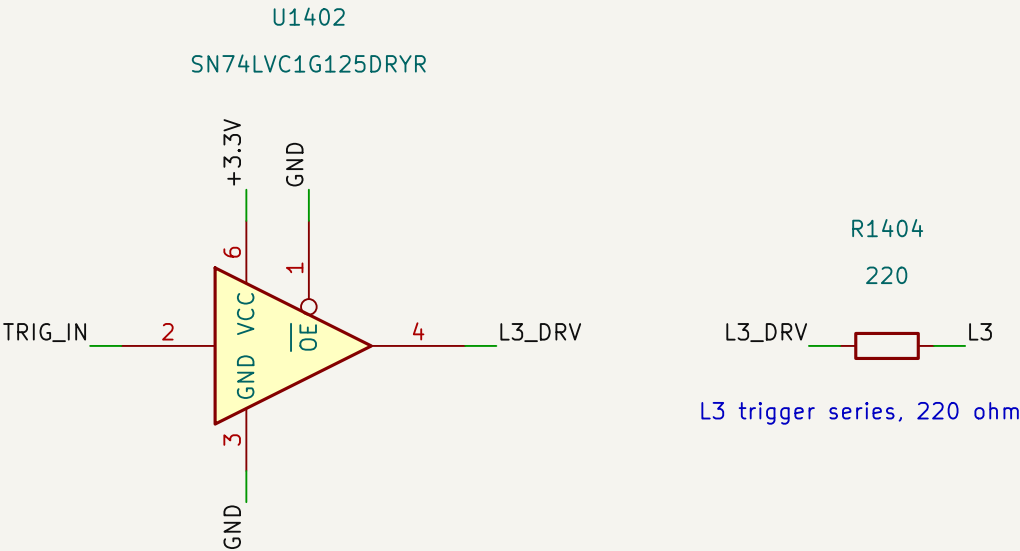
ROUTE: L3, L0, L2 and L1 run straight from the pads to their clamps and parts; GND from pins 5 and 6 into the block’s return.

2. Line 3 trigger drive

U702 (always enabled) drives L3_DRV; R704 (220 ohm) in series feeds camera Line 3 on L3; C701 bypasses U702's VCC.



VCC pin 6 bypass, U702



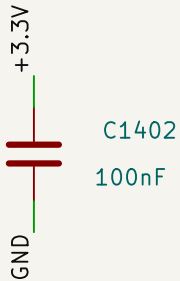
Line 3 trigger driver, always enabled

PLACE: Place U702 near J701 pin 1 with C701 at its pin 6 and a short return to pin 3; R704 between the driver and the connector.

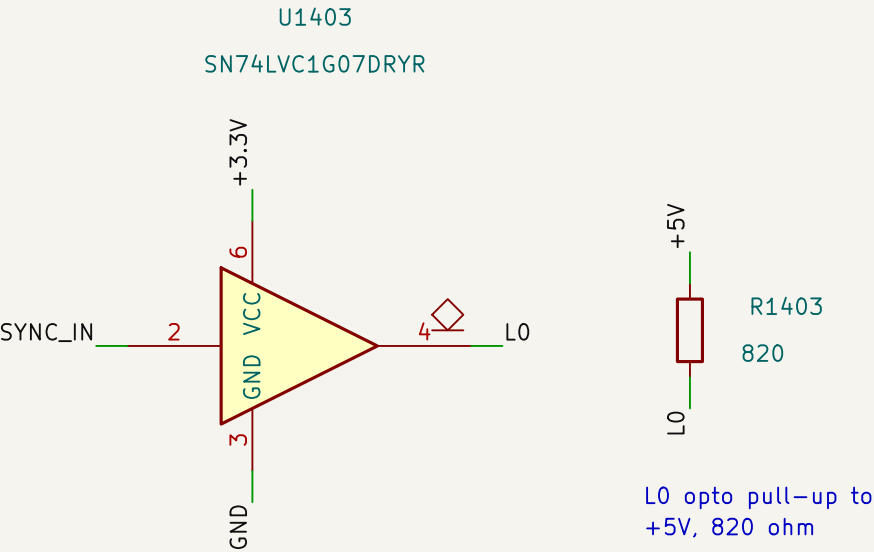
ROUTE: L3 is a 3.3 V edge-triggered line: short, over ground, away from the switching parts of the board.

3. Line 0 sync drive

U703's open-drain Y pulls L0 low; R703 (820 ohm) returns it to +5V, the opto input's drive level; C702 bypasses U703's VCC.



VCC pin 6 bypass, U703



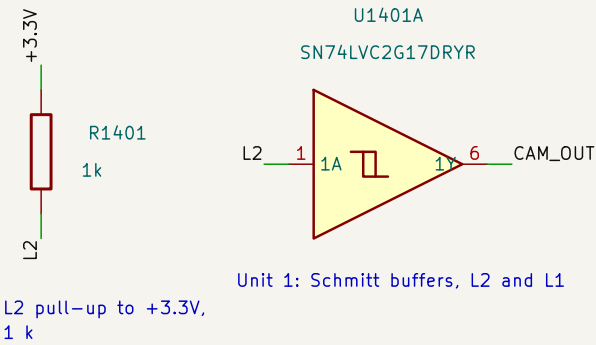
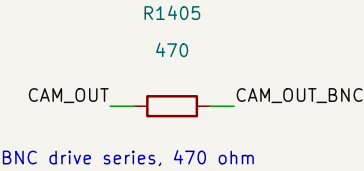
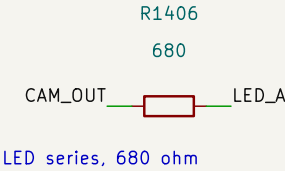
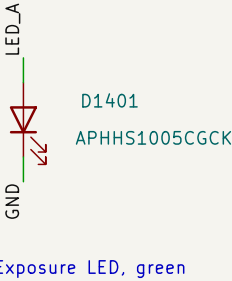
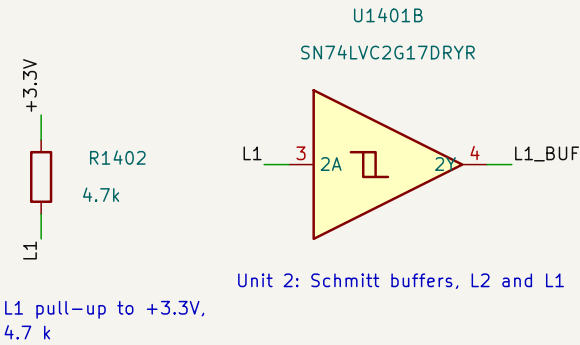
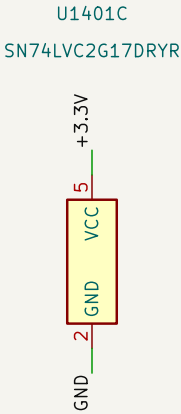
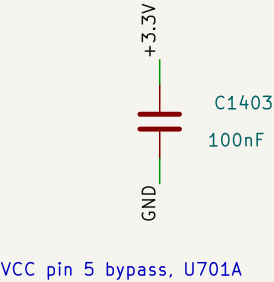
Line 0 sync driver, open drain

PLACE: Place U703 near J701 pin 2 with C702 at its pin 6; R703 from L0 to the +5V entry.

ROUTE: L0 carries about 6 mA pulses into the camera's opto input; keep its return with the trigger line.

4. Exposure output, BNC drive and LED

R701 pulls Line 2 up, U701A gate 1 squares it into CAM_OUT; R705 drives the BNC, R706 lights D701; R702 pulls Line 1 up and gate 2 buffers it into L1_BUF; C703 bypasses U701A.



100 ohm tap (R711) on

INTERNAL NETS

CAM_OUT: Buffered Line 2
L0: Camera pin 2, Line 0
L1: Camera pin 4, Line 1
L1_BUF: Schmitt 2Y: buffered
L2: Camera pin 3, Line 2
L3: Camera pin 1, Line 3
L3_DRV: U702 Y, the trigger
LED_A: LED anode: R706

OPERATION

Camera side: J701's terminals are a Phoenix MC 1,5/6-ST-4 white Line 1 (OPTOOUT).

Trigger path: TRIG_IN -> Line 3; camera settings TRIG_L0, pulled to +5V by R704 5.5 V-tolerant I/O.

Exposure output: camera +3.3V and squared by Schmitt buffer R706 (680 ohm: about (3.3V/680) = 4.8 mA) pulled up by R702 (4.7 k).

ESD: two USBLC6-2P6 are 100 pF per line; both I/O pins are 100 pF to the 3.3V rail: it is the clamp resistor.

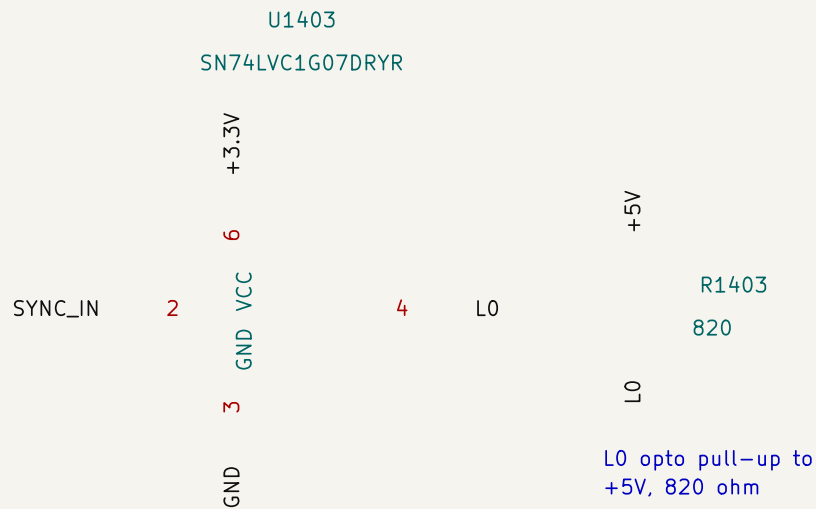
Variants (family.json): model OW-CONN-1844252 (Phoenix 3.5 mm, origin at the package the anchor connector_center).

The placing board provides CAM_OUT_BNC, the connector because the block owns the exit faces.

DESIGN CONTRACT

One FLIR Blackfly S camera family pilot: the vertical

PLACE: Place U701A between the connector and the BNC side with C703 at its pin 5; R701 and R702 at the connector pads; D701 where it is visible.
ROUTE: CAM_OUT is the board's exposure reference: route R705's far end to the BNC with a ground return beside it.



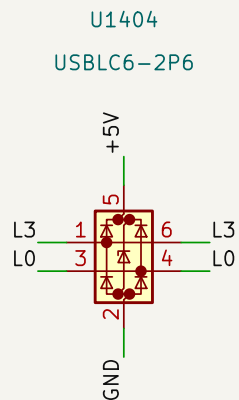
Line 0 sync driver, open drain

PLACE: Place U703 near J701 pin 2 with C702 at its pin 6; R703 from L0 to the +5V entry.

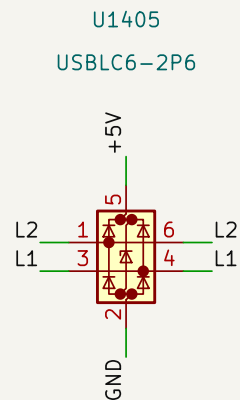
ROUTE: L0 carries about 6 mA pulses into the camera's opto input; keep its return with the trigger line.

5. ESD clamps

U704 clamps L3 and L0, U705 clamps L2 and L1, both referenced to +5V and GND; each pair's two I/O pins are tied to the node.



ESD array for L3/L0



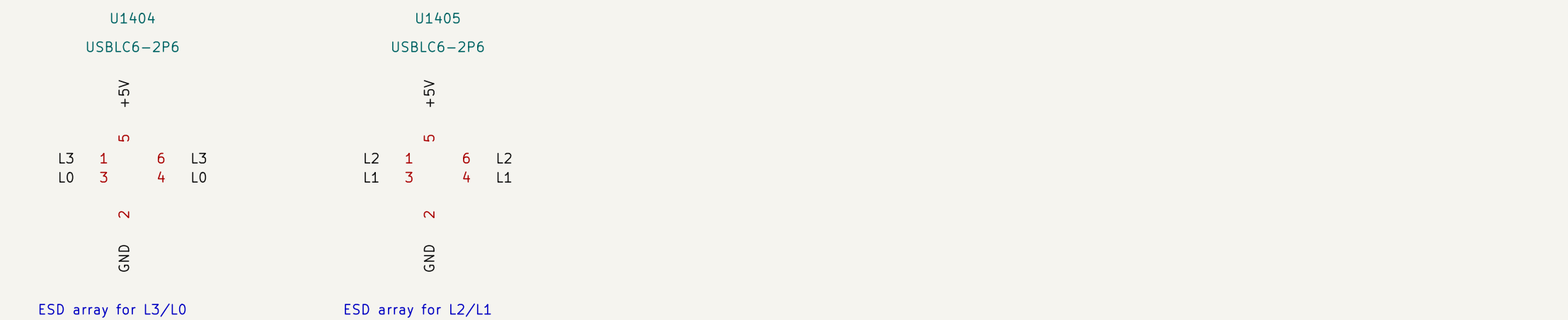
ESD array for L2/L1

PLACE: Place both arrays right at J701's pads, before any series part, with the shortest GND return.

ROUTE: Wire the paired I/O pads together on the node itself; no separate track between them.

5. ESD clamps

U704 clamps L3 and L0, U705 clamps L2 and L1, both referenced to +5V and GND; each pair’s two I/O pins are tied to the node.

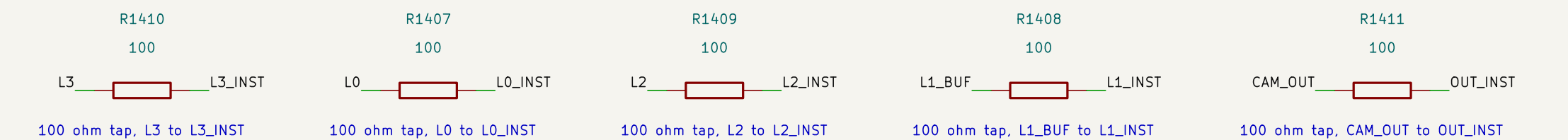


PLACE: Place both arrays right at J701’s pads, before any series part, with the shortest GND return.

ROUTE: Wire the paired I/O pads together on the node itself; no separate track between them.

6. Instrument taps

100 ohm series taps: R710 on L3, R707 on L0, R709 on L2, R708 on L1_BUF, R711 on CAM_OUT, each to its _INST port.



PLACE: Place the five taps as a row toward the instrument–port side of the block.

ROUTE: INSTRUMENT class to the instrument port; every tapped node has a DC definition (driven or pulled up).

INTERFACES

+5V  +5V

Must be a 5 V rail: the Line 0 opto drive level (R703) and both ESD clamps' VBUS reference.

+3.3V  +3.3V

Logic rail for U701A, U702, U703 and the L2/L1 pull-ups; always-on if the taps must read before firmware.

GND  GND

Camera pins 5 (opto ground) and 6 (ground) both land here, with the logic and ESD returns.

TRIG_IN  TRIG_IN

Conditioned 3.3 V frame trigger from the board's input Schmitt into U702 (pin 2).

SYNC_IN  SYNC_IN

Conditioned 3.3 V Rsync from the board's input Schmitt into U703 (pin 2).

CAM_OUT_BNC  CAM_OUT_BNC

Exposure-active output: CAM_OUT through R705 (470 ohm); the BNC itself is the board's.

L0_INST  L0_INST

100 ohm tap (R707) on L0, camera Line 0 OPTOIN: the sync drive.

L1_INST  L1_INST

100 ohm tap (R708) on L1_BUF, camera Line 1 OPTOOUT after the Schmitt buffer.

L2_INST  L2_INST

100 ohm tap (R709) on L2, camera Line 2, the open-drain exposure output.

L3_INST  L3_INST

100 ohm tap (R710) on L3, camera Line 3, the frame trigger.

OUT_INST  OUT_INST

100 ohm tap (R711) on CAM_OUT, the buffered exposure signal.

INTERNAL NETS

CAM_OUT: Buffered Line 2 (exposure active) from U701A 1Y; drives the BNC resistor, the LED resistor and the OUT tap.

L0: Camera pin 2, Line 0 OPTOIN: open–drain U703 Y, pulled to +5V by R703 (820 ohm), clamped by U704.

L1: Camera pin 4, Line 1 OPTOOUT, pulled up to +3.3V by R702 (4.7 k), into Schmitt 2A, clamped by U705.

L1_BUF: Schmitt 2Y: buffered Line 1 for the L1_INST tap.

L2: Camera pin 3, Line 2 as open–drain exposure output, pulled up by R701 (1 k), into Schmitt 1A, clamped by U705.

L3: Camera pin 1, Line 3 GPI trigger, driven by U702 through R704 (220 ohm), clamped by U704.

L3_DRV: U702 Y, the trigger drive before the 220 ohm series resistor.

LED_A: LED anode: R706 (680 ohm) from CAM_OUT, so D701 lights while exposure is active.

OPERATION

Camera side: J701’s terminal numbers are the camera’s Hirose HR10A–7R–6PB pin numbers, wired with the FLIR 1 m flying–lead GPIO cable into a Phoenix MC 1,5/6–ST–3,5 plug: pin 1 green Line 3 (GPI, trigger), pin 2 black Line 0 (OPTOIN, sync), pin 3 red Line 2 (GPIO, exposure output), pin 4 white Line 1 (OPTOOUT), pin 5 blue opto ground and pin 6 brown ground, both on GND (common–ground wiring).

Trigger path: TRIG_IN → U702 (SN74LVC1G125, $\overline{OE}$ pin 1 grounded, so always enabled) → L3_DRV → R704 (220 ohm) → L3 → camera Line 3; camera settings TriggerSelector FrameStart, TriggerSource Line3 RisingEdge. Sync path: SYNC_IN → U703 (SN74LVC1G07 open drain) → L0, pulled to +5V by R703 (820 ohm): 5 V across 820 ohm is about 6 mA, less by the opto input’s forward drop. Both drivers run from +3.3V with 5.5 V–tolerant I/O.

Exposure output: camera Line 2 (LineMode Output, LineSource ExposureActive, V3_3Enable false, so open drain) is pulled up by R701 (1 k) to +3.3V and squared by Schmitt U701A 1A → 1Y = CAM_OUT, which drives the BNC through R705 (470 ohm), the green LED D701 through R706 (680 ohm: about $(3.3 - 2.1) / 680 = 1.8$ mA, LED on while exposure is active) and the OUT_INST tap. Line 1 (OPTOOUT, LineSource Off) is pulled up by R702 (4.7 k) and buffered 2A → 2Y into L1_BUF for its tap.

ESD: two USBLC6–2P6 arrays with VBUS on +5V clamp L3 and L0 (U704) and L2 and L1 (U705), 15 kV IEC 61000–4–2 level 4, at most 3.5 pF per line; both I/O pins of each pair are wired to the node, so the footprint’s paired pads need no track between them. +5V must therefore be a 5 V rail: it is the clamp reference and the opto drive level, and feeds nothing else.

Variants (family.json): mcv6_vertical fits J701 = OW–CONN–TBH–1X06–3P5–VERT (Phoenix MCV 1,5/6–G–3,5, top entry); mc6_horizontal fits OW–CONN–1844252 (Phoenix MC 1,5/6–G–3,5, side entry toward the footprint’s +Y). The two footprints are pad–identical (six 1.8 x 3.6 mm ovals on 3.5 mm, origin at the pad–array centre), so the variant swaps only the connector’s body, courtyard and 3D model; every pad, track and via stays, and the anchor connector_center is the same point for both.

The placing board provides +3.3V (bind it to the always–on rail when the taps must be observable before firmware runs), a 5 V rail on +5V, the BNC on CAM_OUT_BNC, the conditioned 3.3 V TRIG_IN and SYNC_IN, and the instrument port behind the five 100 ohm taps; the three pull–ups are inside because the block owns L0, L1 and L2 (layout convention 10). Place one block per camera; the horizontal variant’s plug needs the board edge its wire exit faces.

DESIGN CONTRACT

One FLIR Blackfly S camera GPIO channel (trigger, sync, exposure output, instrument taps) on a 6–position 3.5 mm Phoenix header; the connector family pilot: the vertical MCV and the horizontal MC header are pad–identical, so one source publishes both orientations

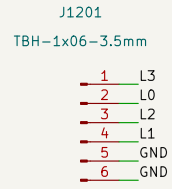
Blackfly S GPIO channel | trigger in, sync in, exposure out, five taps; vertical or horizontal header

One FLIR Blackfly S camera GPIO channel (trigger, sync, exposure output, instrument taps) on a 6-position 3.5 mm Phoenix header; the connector family pilot: the vertical MCV and the horizontal MC header are pad-identical, so one source publishes both orientations

Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Camera header

J701, the 6-position 3.5 mm Phoenix header; pins 1 to 4 are Lines 3, 0, 2 and 1, pins 5 and 6 are the camera's two grounds.

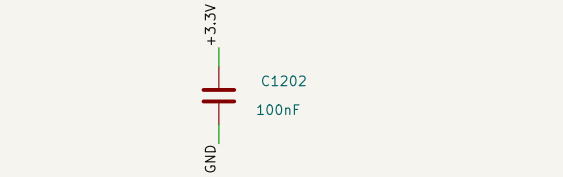


Camera GPIO header, 6-pos
3.5 mm

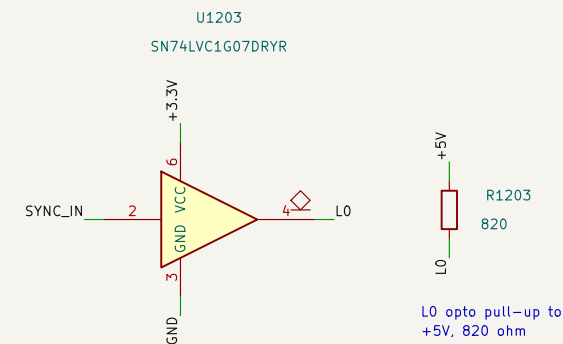
PLACE: Place J701 at the board edge the plug needs: the vertical body takes the plug from above, the horizontal from its +Y side; the anchor is the pad-array centre for both.
ROUTE: L3, L0, L2 and L1 run straight from the pads to their clamps and parts; GND from pins 5 and 6 into the block's return.

3. Line 0 sync drive

U703's open-drain Y pulls L0 low; R703 (820 ohm) returns it to +5V, the opto input's drive level; C702 bypasses U703's VCC.



VCC pin 6 bypass, U703

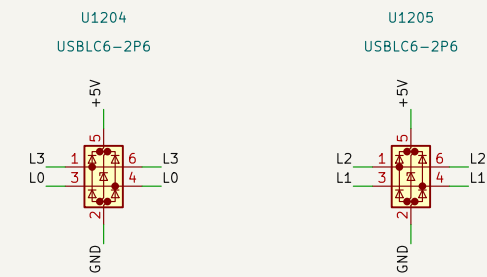


Line 0 sync driver, open drain

PLACE: Place U703 near J701 pin 2 with C702 at its pin 6; R703 from L0 to the +5V entry.
ROUTE: L0 carries about 6 mA pulses into the camera's opto input; keep its return with the trigger line.

5. ESD clamps

U704 clamps L3 and L0, U705 clamps L2 and L1, both referenced to +5V and GND; each pair's two I/O pins are tied to the node.



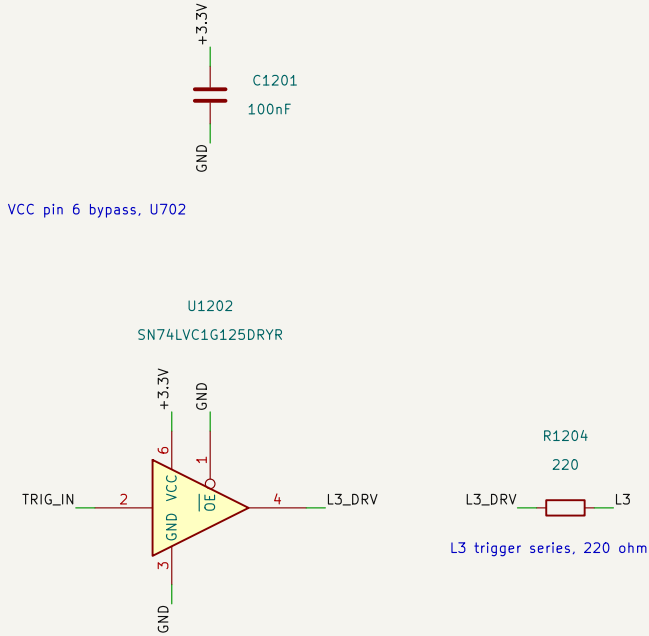
ESD array for L3/L0

ESD array for L2/L1

PLACE: Place both arrays right at J701's pads, before any series part, with the shortest GND return.
ROUTE: Wire the paired I/O pads together on the node itself; no separate track between them.

2. Line 3 trigger drive

U702 (always enabled) drives L3_DRV; R704 (220 ohm) in series feeds camera Line 3 on L3; C701 bypasses U702's VCC.

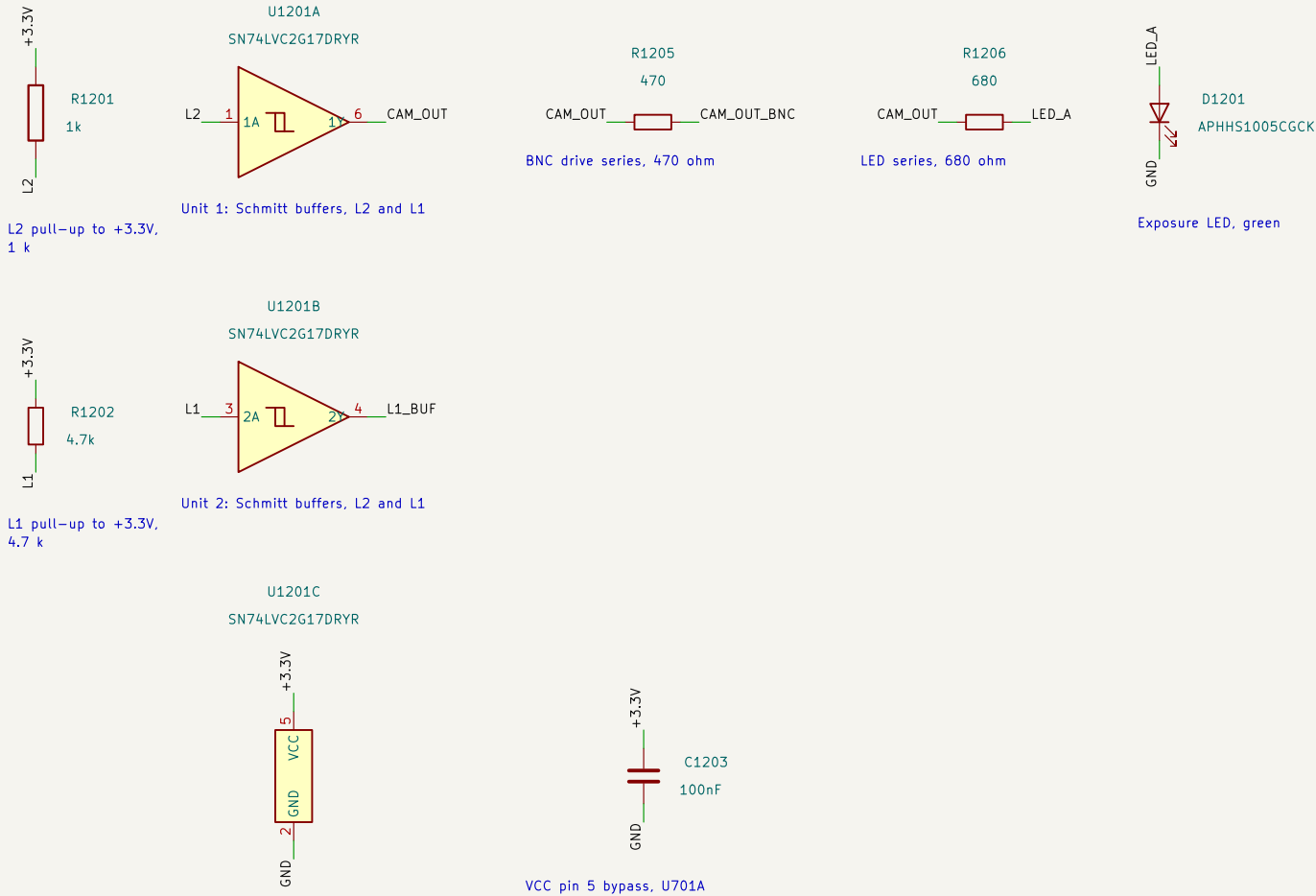


Line 3 trigger driver, always enabled

PLACE: Place U702 near J701 pin 1 with C701 at its pin 6 and a short return to pin 3; R704 between the driver and the connector.
ROUTE: L3 is a 3.3 V edge-triggered line; short, over ground, away from the switching parts of the board.

4. Exposure output, BNC drive and LED

R701 pulls Line 2 up, U701A gate 1 squares it into CAM_OUT; R705 drives the BNC, R706 lights D701; R702 pulls Line 1 up and gate 2 buffers it into L1_BUF; C703 bypasses U701A.



Power unit

PLACE: Place U701A between the connector and the BNC side with C703 at its pin 5; R701 and R702 at the connector pads; D701 where it is visible.
ROUTE: CAM_OUT is the board's exposure reference; route R705's far end to the BNC with a ground return beside it.

INTERFACES

+5V — +5V
Must be a 5 V rail; the Line 0 opto drive level (R703) and both ESD clamps' VBUS reference.

+3.3V — +3.3V
Logic rail for U701A, U702, U703 and the L2/L1 pull-ups; always-on if the taps must read before firmware.

GND — GND
Camera pins 5 (opto ground) and 6 (ground) both land here, with the logic and ESD returns.

TRIG_IN — TRIG_IN
Conditioned 3.3 V frame trigger from the board's input Schmitt into U702 (pin 2).

SYNC_IN — SYNC_IN
Conditioned 3.3 V Rsync from the board's input Schmitt into U703 (pin 2).

CAM_OUT_BNC — CAM_OUT_BNC
Exposure-active output; CAM_OUT through R705 (470 ohm); the BNC itself is the board's.

L0_INST — L0_INST
100 ohm tap (R707) on L0, camera Line 0 OPTOIN; the sync drive.

L1_INST — L1_INST
100 ohm tap (R708) on L1_BUF, camera Line 1 OPTOOUT after the Schmitt buffer.

L2_INST — L2_INST
100 ohm tap (R709) on L2, camera Line 2, the open-drain exposure output.

L3_INST — L3_INST
100 ohm tap (R710) on L3, camera Line 3, the frame trigger.

OUT_INST — OUT_INST
100 ohm tap (R711) on CAM_OUT, the buffered exposure signal.

INTERNAL NETS

CAM_OUT: Buffered Line 2 (exposure active) from U701A 1Y; drives the BNC resistor, the LED resistor and the OUT tap.

L0: Camera pin 2, Line 0 OPTOIN; open-drain U703 Y, pulled to +5V by R703 (820 ohm), clamped by U704.

L1: Camera pin 4, Line 1 OPTOOUT, pulled up to +3.3V by R702 (4.7 k), into Schmitt 2A, clamped by U705.

L1_BUF: Schmitt 2Y; buffered Line 1 for the L1_INST tap.

L2: Camera pin 3, Line 2 as open-drain exposure output, pulled up by R701 (1 k), into Schmitt 1A, clamped by U705.

L3: Camera pin 1, Line 3 GPI trigger, driven by U702 through R704 (220 ohm), clamped by U704.

L3_DRV: U702 Y, the trigger drive before the 220 ohm series resistor.

LED_A: LED anode; R706 (680 ohm) from CAM_OUT, so D701 lights while exposure is active.

OPERATION

Camera side: J701's terminal numbers are the camera's Hirose HR10A-7R-6PB pin numbers, wired with the FLIR 1 m flying-lead GPIO cable into a Phoenix MC 1.5/6-ST-3.5 plug; pin 1 green Line 3 (GPI, trigger), pin 2 black Line 0 (OPTOIN, sync), pin 3 red Line 2 (GPIO, exposure output), pin 4 white Line 1 (OPTOOUT), pin 5 blue opto ground and pin 6 brown ground, both on GND (common-ground wiring).

Trigger path: TRIG_IN -> U702 (SN74LVC1G125, OE pin 1 grounded, so always enabled) -> L3_DRV -> R704 (220 ohm) -> L3 -> camera Line 3; camera settings TriggerSelector FrameStart, TriggerSource Line3 RisingEdge. Sync path: SYNC_IN -> U703 (SN74LVC1G07 open drain) -> L0, pulled to +5V by R703 (820 ohm); 5 V across 820 ohm is about 6 mA, less by the opto input's forward drop. Both drivers run from +3.3V with 5.5 V-tolerant I/O.

Exposure output: camera Line 2 (LineMode Output, LineSource ExposureActive, V3.3Enable false, so open drain) is pulled up by R701 (1 k) to +3.3V and squared by Schmitt U701A 1A -> 1Y = CAM_OUT, which drives the BNC through R705 (470 ohm), the green LED D701 through R706 (680 ohm; about (3.3 - 2.1) / 680 = 1.8 mA, LED on while exposure is active) and the OUT_INST tap. Line 1 (OPTOOUT, LineSource Off) is pulled up by R702 (4.7 k) and buffered 2A -> 2Y into L1_BUF for its tap.

ESD: two USBLC6-2P6 arrays with VBUS on +5V clamp L3 and L0 (U704) and L2 and L1 (U705), 15 kV IEC 61000-4-2 level 4, at most 3.5 pF per line; both I/O pins of each pair are wired to the node, so the footprint's paired pads need no track between them. +5V must therefore be a 5 V rail: it is the clamp reference and the opto drive level, and feeds nothing else.

Variants (family.json): mcv6_vertical fits J701 = OW-CONN-TBH-1X06-3P5-VERT (Phoenix MCV 1.5/6-G-3.5, top entry); mc6_horizontal fits OW-CONN-1844252 (Phoenix MC 1.5/6-G-3.5, side entry toward the footprint's +Y). The two footprints are pad-identical (six 1.8 x 3.6 mm ovals on 3.5 mm, origin at the pad-array centre), so the variant swaps only the connector's body, courtyard and 3D model; every pad, track and via stays, and the anchor connector_center is the same point for both.

The placing board provides +3.3V (bind it to the always-on rail when the taps must be observable before firmware runs), a 5 V rail on +5V, the BNC on CAM_OUT_BNC, the conditioned 3.3 V TRIG_IN and SYNC_IN, and the instrument port behind the five 100 ohm taps; the three pull-ups are inside because the block owns L0, L1 and L2 (layout convention 10). Place one block per camera; the horizontal variant's plug needs the board edge its wire exit faces.

DESIGN CONTRACT

One FLIR Blackfly S camera GPIO channel (trigger, sync, exposure output, instrument taps) on a 6-position 3.5 mm Phoenix header; the connector family pilot: the vertical MCV and the horizontal MC header are pad-identical, so one source publishes both orientations

Circuit and PCB layout guidance
Migrated from the saved family core; circuit, variants and PCB unchanged

Orb Weaver

Sheet: /blackfly_s_gpio_channel_mcv6_vertical1/
File: blackfly_s_gpio_channel_mcv6_vertical.kicad_sch

Title: **Blackfly S GPIO channel family**

Size: A2

Date: 2026-10-04

Rev: Source migration 1

KiCad E.D.A. 10.0.6

Id: 12/11

1

2

3

4

Blackfly S GPIO channel | trigger in, sync in, exposure out, five taps; vertical or horizontal header

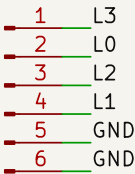
One FLIR Blackfly S camera GPIO channel (trigger, sync, exposure output, instrument taps) on a 6-position 3.5 mm Phoenix header; the connector family pilot: the vertical body takes the plug from above, the horizontal from its +Y side; the anchor is the pad-array centre for both. Matching net labels are connected. Group order explains function; PCB placement priorities are stated below.

1. Camera header

J701, the 6-position 3.5 mm Phoenix header; pins 1 to 4 are Lines 3, 0, 2 and 1, pins 5 and 6 are the camera's two grounds.

J1201

TBH-1x06-3.5mm



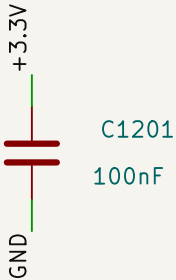
Camera GPIO header, 6-pos
3.5 mm

PLACE: Place J701 at the board edge the plug needs: the vertical body takes the plug from above, the horizontal from its +Y side; the anchor is the pad-array centre for both.

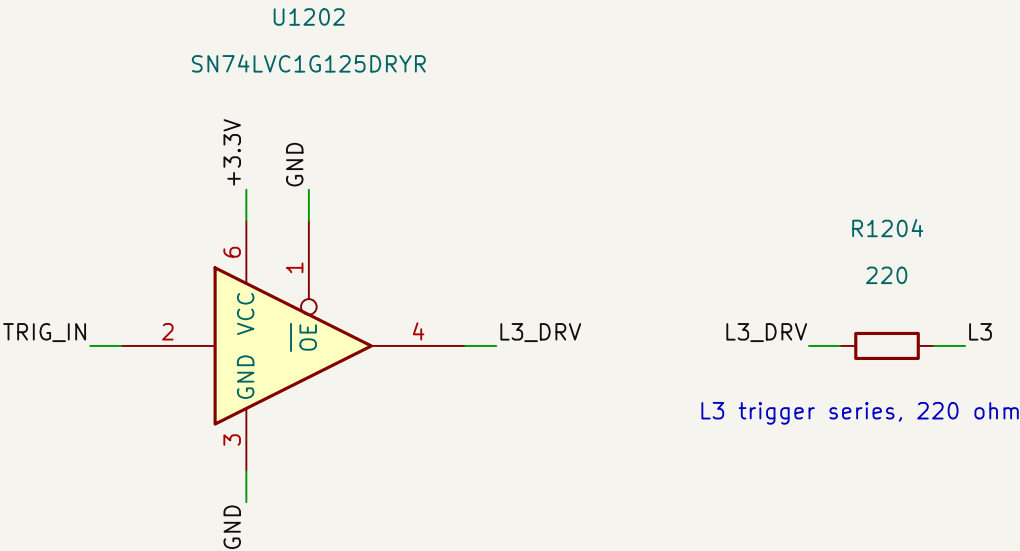
ROUTE: L3, L0, L2 and L1 run straight from the pads to their clamps and parts; GND from pins 5 and 6 into the block's return.

2. Line 3 trigger drive

U702 (always enabled) drives L3_DRV; R704 (220 ohm) in series feeds camera Line 3 on L3; C701 bypasses U702's VCC.



VCC pin 6 bypass, U702



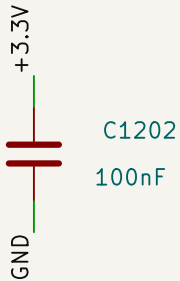
Line 3 trigger driver, always enabled

PLACE: Place U702 near J701 pin 1 with C701 at its pin 6 and a short return to pin 3; R704 between the driver and the connector.

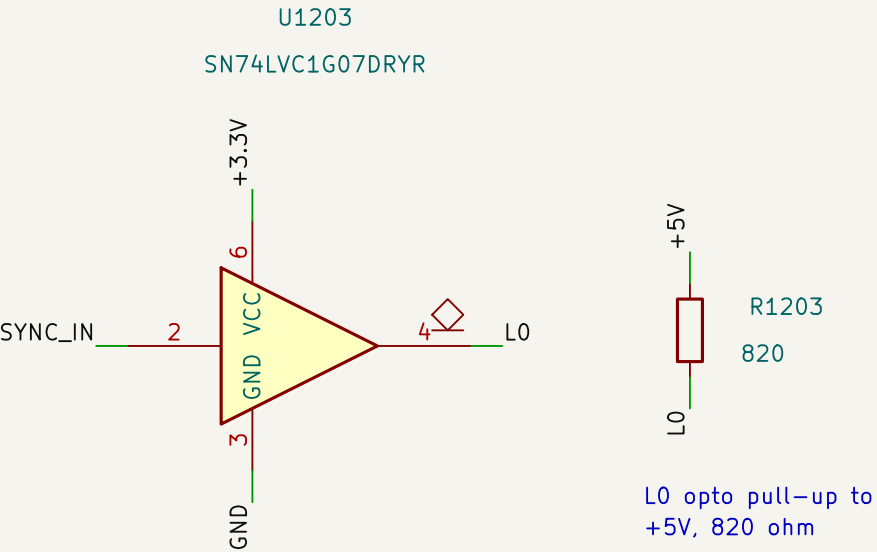
ROUTE: L3 is a 3.3 V edge-triggered line: short, over ground, away from the switching parts of the board.

3. Line 0 sync drive

U703's open-drain Y pulls L0 low; R703 (820 ohm) returns it to +5V, the opto input's drive level; C702 bypasses U703's VCC.



VCC pin 6 bypass, U703



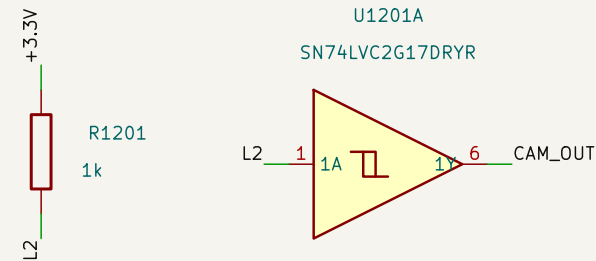
Line 0 sync driver, open drain

PLACE: Place U703 near J701 pin 2 with C702 at its pin 6; R703 from L0 to the +5V entry.

ROUTE: L0 carries about 6 mA pulses into the camera's opto input; keep its return with the trigger line.

4. Exposure output, BNC drive and LED

R701 pulls Line 2 up, U701A gate 1 squares it into CAM_OUT; R705 drives the BNC, R706 lights D701; R702 pulls Line 1 up and gate 2 buffers it into L1_BUF; C703 bypasses U701A.

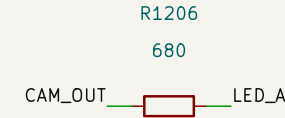


Unit 1: Schmitt buffers, L2 and L1

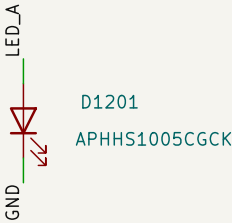
L2 pull-up to +3.3V, 1 k



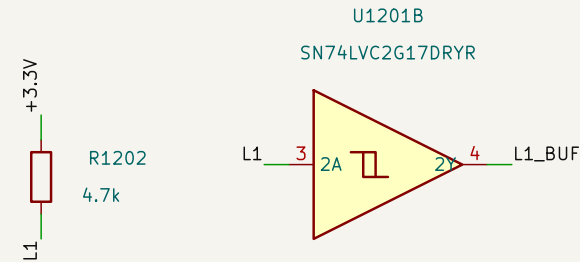
BNC drive series, 470 ohm



LED series, 680 ohm

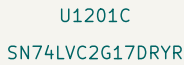


Exposure LED, green

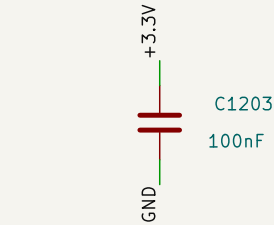


Unit 2: Schmitt buffers, L2 and L1

L1 pull-up to +3.3V, 4.7 k



Power unit



VCC pin 5 bypass, U701A

INTERNAL NETS

CAM_OUT: Buffered Line 2

L0: Camera pin 2, Line 0

L1: Camera pin 4, Line 1

L1_BUF: Schmitt 2Y: buffered

L2: Camera pin 3, Line 2

L3: Camera pin 1, Line 3

L3_DRV: U702 Y, the trigger

LED_A: LED anode: R706

OPERATION

Camera side: J701's terminals are a Phoenix MC 1,5/6-ST-4 white Line 1 (OPTOOUT),

Trigger path: TRIG_IN -> Line 3; camera settings T L0, pulled to +5V by R705 5.5 V-tolerant I/O.

Exposure output: camera +3.3V and squared by Schmitt R706 (680 ohm: about (3 pulled up by R702 (4.7 k

ESD: two USBLC6-2P6 and 10 pF per line; both I/O pins 5 V rail: it is the clamp ret

Variants (family.json): model OW-CONN-1844252 (Phoenix 3.5 mm, origin at the pad the anchor connector_cen

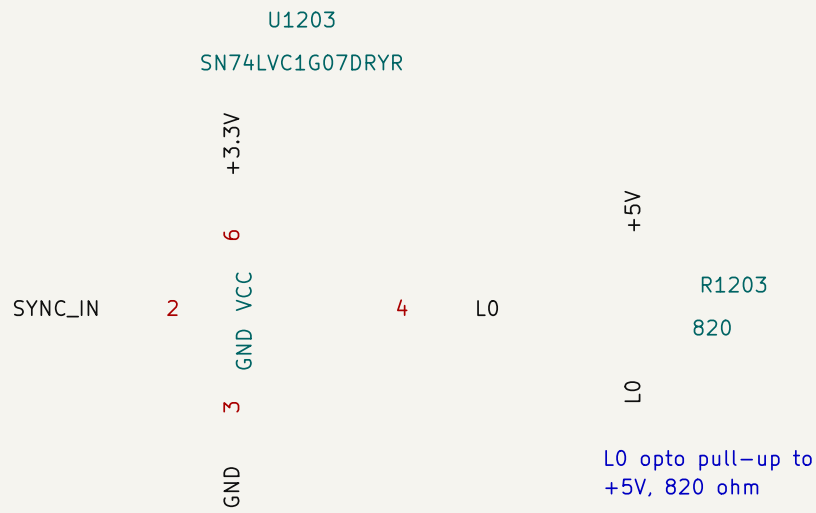
The placing board provides on CAM_OUT_BNC, the connector because the block owns 1 exit faces.

DESIGN CONTRACT

One FLIR Blackfly S camera family pilot: the vertical

PLACE: Place U701A between the connector and the BNC side with C703 at its pin 5; R701 and R702 at the connector pads; D701 where it is visible.

ROUTE: CAM_OUT is the board's exposure reference: route R705's far end to the BNC with a ground return beside it.



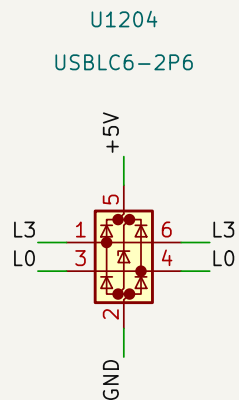
Line 0 sync driver, open drain

PLACE: Place U703 near J701 pin 2 with C702 at its pin 6; R703 from L0 to the +5V entry.

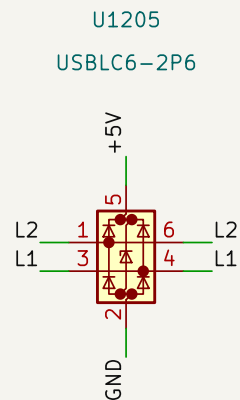
ROUTE: L0 carries about 6 mA pulses into the camera's opto input; keep its return with the trigger line.

5. ESD clamps

U704 clamps L3 and L0, U705 clamps L2 and L1, both referenced to +5V and GND; each pair's two I/O pins are tied to the node.



ESD array for L3/L0



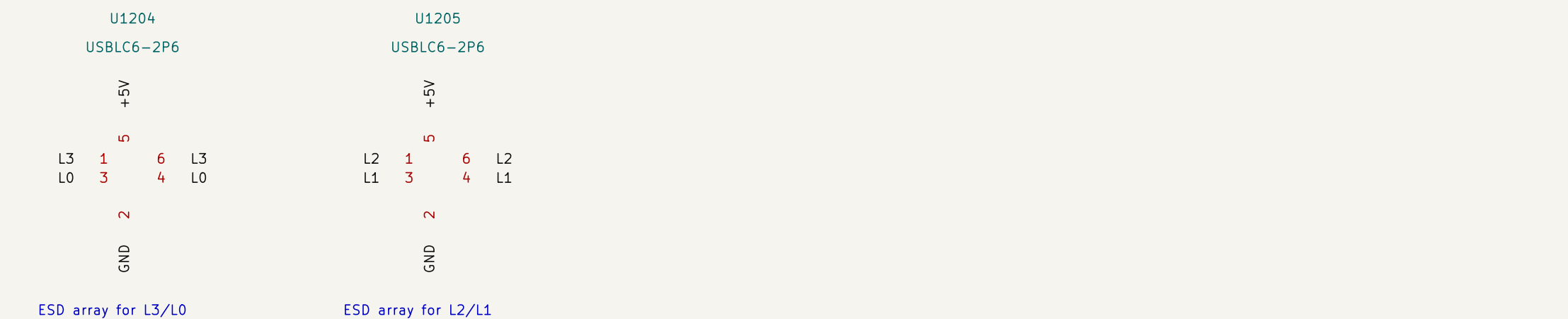
ESD array for L2/L1

PLACE: Place both arrays right at J701's pads, before any series part, with the shortest GND return.

ROUTE: Wire the paired I/O pads together on the node itself; no separate track between them.

5. ESD clamps

U704 clamps L3 and L0, U705 clamps L2 and L1, both referenced to +5V and GND; each pair’s two I/O pins are tied to the node.

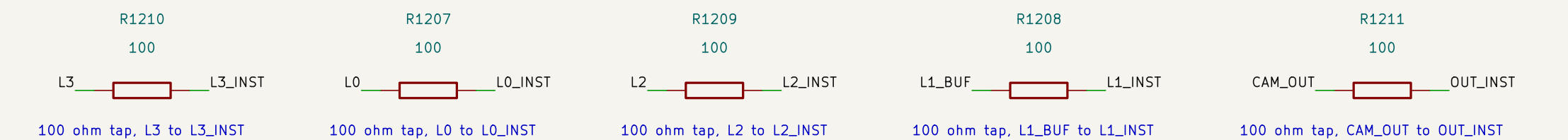


PLACE: Place both arrays right at J701’s pads, before any series part, with the shortest GND return.

ROUTE: Wire the paired I/O pads together on the node itself; no separate track between them.

6. Instrument taps

100 ohm series taps: R710 on L3, R707 on L0, R709 on L2, R708 on L1_BUF, R711 on CAM_OUT, each to its _INST port.



PLACE: Place the five taps as a row toward the instrument–port side of the block.

ROUTE: INSTRUMENT class to the instrument port; every tapped node has a DC definition (driven or pulled up).

INTERFACES

+5V  +5V

Must be a 5 V rail: the Line 0 opto drive level (R703) and both ESD clamps' VBUS reference.

+3.3V  +3.3V

Logic rail for U701A, U702, U703 and the L2/L1 pull-ups; always-on if the taps must read before firmware.

GND  GND

Camera pins 5 (opto ground) and 6 (ground) both land here, with the logic and ESD returns.

TRIG_IN  TRIG_IN

Conditioned 3.3 V frame trigger from the board's input Schmitt into U702 (pin 2).

SYNC_IN  SYNC_IN

Conditioned 3.3 V Rsync from the board's input Schmitt into U703 (pin 2).

CAM_OUT_BNC  CAM_OUT_BNC

Exposure-active output: CAM_OUT through R705 (470 ohm); the BNC itself is the board's.

L0_INST  L0_INST

100 ohm tap (R707) on L0, camera Line 0 OPTOIN: the sync drive.

L1_INST  L1_INST

100 ohm tap (R708) on L1_BUF, camera Line 1 OPTOOUT after the Schmitt buffer.

L2_INST  L2_INST

100 ohm tap (R709) on L2, camera Line 2, the open-drain exposure output.

L3_INST  L3_INST

100 ohm tap (R710) on L3, camera Line 3, the frame trigger.

OUT_INST  OUT_INST

100 ohm tap (R711) on CAM_OUT, the buffered exposure signal.

INTERNAL NETS

CAM_OUT: Buffered Line 2 (exposure active) from U701A 1Y; drives the BNC resistor, the LED resistor and the OUT tap.

L0: Camera pin 2, Line 0 OPTOIN: open–drain U703 Y, pulled to +5V by R703 (820 ohm), clamped by U704.

L1: Camera pin 4, Line 1 OPTOOUT, pulled up to +3.3V by R702 (4.7 k), into Schmitt 2A, clamped by U705.

L1_BUF: Schmitt 2Y: buffered Line 1 for the L1_INST tap.

L2: Camera pin 3, Line 2 as open–drain exposure output, pulled up by R701 (1 k), into Schmitt 1A, clamped by U705.

L3: Camera pin 1, Line 3 GPI trigger, driven by U702 through R704 (220 ohm), clamped by U704.

L3_DRV: U702 Y, the trigger drive before the 220 ohm series resistor.

LED_A: LED anode: R706 (680 ohm) from CAM_OUT, so D701 lights while exposure is active.

OPERATION

Camera side: J701’s terminal numbers are the camera’s Hirose HR10A–7R–6PB pin numbers, wired with the FLIR 1 m flying–lead GPIO cable into a Phoenix MC 1,5/6–ST–3,5 plug: pin 1 green Line 3 (GPI, trigger), pin 2 black Line 0 (OPTOIN, sync), pin 3 red Line 2 (GPIO, exposure output), pin 4 white Line 1 (OPTOOUT), pin 5 blue opto ground and pin 6 brown ground, both on GND (common–ground wiring).

Trigger path: TRIG_IN → U702 (SN74LVC1G125, $\overline{OE}$ pin 1 grounded, so always enabled) → L3_DRV → R704 (220 ohm) → L3 → camera Line 3; camera settings TriggerSelector FrameStart, TriggerSource Line3 RisingEdge. Sync path: SYNC_IN → U703 (SN74LVC1G07 open drain) → L0, pulled to +5V by R703 (820 ohm): 5 V across 820 ohm is about 6 mA, less by the opto input’s forward drop. Both drivers run from +3.3V with 5.5 V–tolerant I/O.

Exposure output: camera Line 2 (LineMode Output, LineSource ExposureActive, V3_3Enable false, so open drain) is pulled up by R701 (1 k) to +3.3V and squared by Schmitt U701A 1A → 1Y = CAM_OUT, which drives the BNC through R705 (470 ohm), the green LED D701 through R706 (680 ohm: about $(3.3 - 2.1) / 680 = 1.8$ mA, LED on while exposure is active) and the OUT_INST tap. Line 1 (OPTOOUT, LineSource Off) is pulled up by R702 (4.7 k) and buffered 2A → 2Y into L1_BUF for its tap.

ESD: two USBLC6–2P6 arrays with VBUS on +5V clamp L3 and L0 (U704) and L2 and L1 (U705), 15 kV IEC 61000–4–2 level 4, at most 3.5 pF per line; both I/O pins of each pair are wired to the node, so the footprint’s paired pads need no track between them. +5V must therefore be a 5 V rail: it is the clamp reference and the opto drive level, and feeds nothing else.

Variants (family.json): mcv6_vertical fits J701 = OW–CONN–TBH–1X06–3P5–VERT (Phoenix MCV 1,5/6–G–3,5, top entry); mc6_horizontal fits OW–CONN–1844252 (Phoenix MC 1,5/6–G–3,5, side entry toward the footprint’s +Y). The two footprints are pad–identical (six 1.8 x 3.6 mm ovals on 3.5 mm, origin at the pad–array centre), so the variant swaps only the connector’s body, courtyard and 3D model; every pad, track and via stays, and the anchor connector_center is the same point for both.

The placing board provides +3.3V (bind it to the always–on rail when the taps must be observable before firmware runs), a 5 V rail on +5V, the BNC on CAM_OUT_BNC, the conditioned 3.3 V TRIG_IN and SYNC_IN, and the instrument port behind the five 100 ohm taps; the three pull–ups are inside because the block owns L0, L1 and L2 (layout convention 10). Place one block per camera; the horizontal variant’s plug needs the board edge its wire exit faces.

DESIGN CONTRACT

One FLIR Blackfly S camera GPIO channel (trigger, sync, exposure output, instrument taps) on a 6–position 3.5 mm Phoenix header; the connector family pilot: the vertical MCV and the horizontal MC header are pad–identical, so one source publishes both orientations